

DESCRIPTION

This document describes the specification for the F1300 **D**igital **P**re-**D**istortion Demodulator for PA linearization. This device is one of 2 variants to cover common UTRA bands. See the Part# Matrix below for details.

COMPETITIVE ADVANTAGE

In typical basestation transmitters a digital pre-distortion loop is employed to improve the Transmitter performance. The signal coming out of the PA is sampled so that the I&Q data at Baseband can be pre-distorted before being sent to the Tx DAC to counteract the distortion inherent in the downstream PA. The signal coupled from the PA is adjusted via a digital step attenuator to a lower level and then sub-sampled at an IF frequency of ~200 MHz which necessitates the need for a highly linear demodulator to downmix to quadrature IF from the Transmit frequency. By sampling IF_I and IF_Q independently and then digitally combining these signals, an effective doubling of the sample rate can be achieved. Any distortion in this path will degrade the performance of the DPD algorithm. By utilizing an ultra-linear demodulator w/integrated DSA such as the F1300, the ACLR and/or power consumption of the full Tx system can be improved significantly.

- ✓ DPD full path ACLR: ↓ 1 dB
- ✓ I_{cc}: DPD function Power Consumption ↓ 40%
- ✓ Zero-Distortion™ Demod eliminates 2 IF amps
- ✓ Integrates 2 BPFs, 2 Baluns, 2 SP2Ts
- ✓ Glitch-Free™ gain control



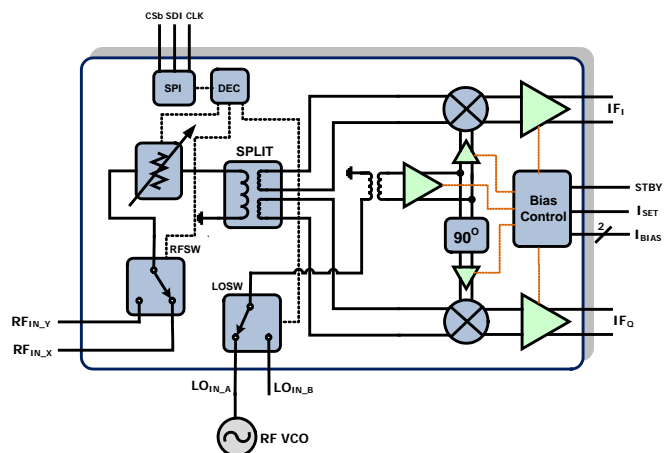
PART# MATRIX

| Part# | RF range | UTRA bands | IF freq range | Typ. Gain | Injection |
|-------|-------------|---------------------------|---------------|-----------|-----------------------|
| F1300 | 550 - 1150 | 5,6,8,12,13,14,17 | 20 - 350 | 12.5 | High Side or Low Side |
| F1350 | 1300 - 2900 | 1,2,3,4,9,10,7,21, 24, 38 | 20 - 500 | 12.5 | High Side or Low Side |

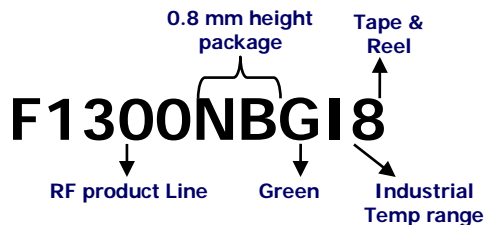
FEATURES (I OR Q PATH)

- Wide flat performance IF BW
- Wide RF and LO BWs (~ 0.8 GHz)
- Ideal for Multi-Carrier Systems
- Drives ADC directly
- Ultra linear +43 dBm IP_{3o}
- Low Noise Figure
- Excellent ACLR performance
- **200Ω** output impedance
- Fully integrated DPD demodulator
- 6 x 6 mm 36-pin package
- Standby Mode w/Fast Recovery
- I_{cc}: 262 mA

DEVICE BLOCK DIAGRAM



ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

| | |
|---|----------------------------------|
| V _{CC} to GND | -0.3V to +5.5V |
| SW_Latch, DATA, CSb, CLK | 0V to 3.6V |
| STBY | 0V to V _{CC} |
| IF_I+, IF_I-, IF_Q+, IF_Q- | 1V to (V _{CC} + 0.3V) |
| IF_BiasI, IF_BiasQ to GND | -0.3V to +1.2V |
| LO_ADJ to GND | 2.1V to 4.0V |
| RF Input Power (Into RFIN_X or RFIN_Y) | +27 dBm |
| Continuous Power Dissipation | 2.5W |
| θ _{JA} (Junction – Ambient) | +40°C/W |
| θ _{JC} (Junction – Case) The Case is defined as the exposed paddle | +3°C/W |
| Operating Temperature Range (Case Temperature) | T _C = -40°C to +105°C |
| Maximum Junction Temperature | 150°C |
| Storage Temperature Range | -65°C to +150°C |
| Moisture Sensitivity Level | 1 |
| Lead Temperature (soldering, 10s) | +260°C |

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

F1300 SPECIFICATION

Refer to Typical Application Circuit when operated with $V_{CC} = +5.0V$, $T_{CASE} = 25C$, $F_{RF} = 860\text{ MHz}$, $F_{LO} = 1060\text{ MHz}$, Gain = G_{MAX} , $P_{LO} = 0\text{ dBm}$, $T_C = +25^\circ C$, STBY = GND, unless otherwise noted. Full Lineup measured through to I or Q path. IF Transformers and RF trace losses de-embedded.

| Parameter | Comment | Symbol | Min | Typ | Max | Units |
|----------------------------|--|------------------------------|-------------|-----------------|------------------------|----------|
| Logic Input High | For STBY, DATA, CSb, CLK, SW_Latch | V_{IH} | 2.3 | | | V |
| Logic Input Low | For STBY, DATA, CSb, CLK, SW_Latch | V_{IL} | | | 0.5 | V |
| Logic Current | $V_H = 2.3V$, $V_L = 0V$ | I_{IH} , I_{IL} | -135 | | +10 | μA |
| Supply Voltage(s) | All V_{CC} (operating range) | V_{CC} | | 4.75 to 5.25 | | V |
| Temperature Range | Operating Range | T_{CASE} | -40 | | +105 | degC |
| Supply Current | Total V_{CC} | I_{SUPP} | | 262 | 290¹ | mA |
| Supply Current | Standby Mode: STBY > V_{IH} | I_{STBY} | | 22 | 27 | mA |
| RF Freq Range | Sets LO freq range | F_{RF} | 700 | | 1100 | MHz |
| IF center Freq Range | Sets LO freq range | F_{IF} | 100 | | 250 | MHz |
| Oversample Operating Range | <ul style="list-style-type: none"> ▪ Measure Gain at I&Q ▪ Gain setting = G_{MAX} ▪ $F_{LO} = 950\text{ MHz}$, 1080 MHz ▪ Gain Delta < 2.5 dB | F_{RFD} | 550 | | 1150 | MHz |
| Oversample IF Range | <ul style="list-style-type: none"> ▪ Measure Gain at I&Q ▪ Gain setting = G_{MAX} ▪ $F_{LO} = 950\text{ MHz}$, 1080 MHz ▪ Gain Delta < 2.5 dB | F_{IFD} | 20 | | 350 | MHz |
| IF Linearity BW | <ul style="list-style-type: none"> ▪ RF Freq = 860 MHz ▪ IP3O > +39 dBm ▪ From RF_INX to I+,I- & Q+,Q- ▪ Pin = -11 dBm/Tone ▪ Gain setting = G_{MAX} | IF_{LIN} | 100 | | 300 | MHz |
| RF Linearity BW | <ul style="list-style-type: none"> ▪ IF Freq = 200 MHz ▪ IP3O > +37.5 dBm ▪ From RF_INX to I+,I- & Q+,Q- ▪ Pin = -11 dBm/Tone ▪ Gain setting = G_{MAX} | RF_{LIN} | 700 | | 1100 | MHz |
| LO Freq Range1 | With R20 = 2.8K | F_{LOH1} | 650 | | 1300 | MHz |
| LO Freq Range2 | With R20 = 4.0K | F_{LOH2} | 500 | | 650 | MHz |
| LO Power | Operating Range | P_{LO} | | -3 to +3 | | dBm |
| RF Input Impedance | Single Ended (RL > 10 dB) | Z_{RF} | | 50 | | Ω |
| IF Output Impedance | Differential (RL > 10 dB) | Z_{IF} | | 200 | | Ω |
| LO port Impedance | Single Ended (RL > 10 dB) | Z_{LO} | | 50 | | Ω |
| Gain maximum | <ul style="list-style-type: none"> ▪ From RF_INX to I+,I- & Q+,Q- ▪ Gain setting = G_{MAX} ▪ Pin = -11 dBm | G_{MAX} OR $ATTN_{MIN}$ | 11 | 12.5 | 14 | dB |
| Gain minimum | <ul style="list-style-type: none"> ▪ From RF_INX to I+,I- ▪ Gain setting = G_{MIN} ▪ Pin = +14 dBm | G_{MIN} OR $ATTN_{MAX}$ | -15 | -13.5 | -12 | dB |

F1300 SPECIFICATION - CONTINUED

Refer to Typical Application Circuit when operated with $V_{CC} = +5.0V$, $T_{CASE} = 25C$, $F_{RF} = 860\text{ MHz}$, $F_{LO} = 1060\text{ MHz}$, Gain = G_{MAX} , $P_{LO} = 0\text{ dBm}$, $T_C = +25^\circ C$, STBY = GND, unless otherwise noted. Full Lineup measured through to I or Q path. IF Transformers and RF trace losses de-embedded.

| Parameter | Comment | Symbol | Min | Typ | Max | Units |
|--|---|--------------------|-----------------|------------|----------|---------|
| Noise Figure | <ul style="list-style-type: none"> From RF_INX to I+,I- out Gain setting = G_{MAX} | NF | | 18.3 | | dB |
| Output IP3 – G_{MAX} | <ul style="list-style-type: none"> Measured at I+,I- and Q+,Q- $P_{IN} = -11\text{ dBm}$ per tone 5 MHz Tone Separation Gain setting = G_{MAX} | IP3 _{MAX} | 39 | 43 | | dBm |
| Output IP3 – G_{-20} | <ul style="list-style-type: none"> Measured at I+,I- and Q+,Q- $P_{IN} = +9\text{ dBm}$ per tone 5 MHz Tone Separation Gain setting = G_{-20} | IP3 ₋₂₀ | 39 ² | 42 | | dBm |
| 2 nd Harmonic | <ul style="list-style-type: none"> Measured at I+,I- and Q+,Q- $P_{IN} = -11\text{ dBm}$ $F_{RF} = 860$, $F_{LO} = 970$ Gain setting = G_{MAX} | H2 | -70 | -76 | | dBc |
| Output IP2 | <ul style="list-style-type: none"> Measured at I+,I- and Q+,Q- $P_{IN} = -11\text{ dBm}$ per tone 5 MHz Tone Separation Gain setting = G_{MAX} | IP2 _o | 59 | 65 | | dBm |
| Output compression | <ul style="list-style-type: none"> Measured at I+,I- and Q+,Q- $P_{IN} = +4\text{ dBm}$ Gain setting = G_{MAX} | C | | 0.3 | 1 | dB |
| Gain Ripple1 | <ul style="list-style-type: none"> Fixed LO = 1020 MHz RF = 650 to 1000 MHz IF = 20 to 370 MHz | Ripple1 | | 0.8 | 1.4 | dB |
| Gain Ripple2 | <ul style="list-style-type: none"> Fixed LO = 1061.5 MHz RF = 591.5MHz to 1041.5MHz IF = 20 to 470 MHz | Ripple2 | | 1.1 | 1.5 | dB |
| Group Delay Distortion | <ul style="list-style-type: none"> Fixed LO = 1020 MHz RF = 650 to 1000 MHz IF = 20 to 350 MHz | GDD | | 2 | | nsec |
| Quadrature Amplitude Balance | <ul style="list-style-type: none"> From RF_INX to I+,I- & Q+,Q- Gain setting = G_{MAX} $P_{in} = -11\text{ dBm}$ | BAL _G | -0.2 | | 0.2 | dB |
| Quadrature Phase Balance | <ul style="list-style-type: none"> $F_{RF} = 860$, $F_{LO} = 1060$ Measure with 20 GSa/sec scope | BAL _φ | -3 | | +3 | degrees |
| Amplitude Balance over environmentals | <ul style="list-style-type: none"> $F_{RF} = 860$, $F_{LO} = 1060$ $T_C = -40C$ to $100C$ LO drive = -3 dBm to +3 dBm Measure with 20 GSa/sec scope | BAL _{GΔ} | -0.3 | | +0.3 | dB |
| Quadrature Phase Balance over environmentals | <ul style="list-style-type: none"> $F_{RF} = 860$, $F_{LO} = 1060$ $T_C = -40C$ to $100C$ LO drive = -3 dBm to +3 dBm Measure with 20 GSa/sec scope | BAL _{φΔ} | -3 | | +3 | degrees |
| LO to IF leakage | | ISO _{LI} | | -30 | -25 | dBm |
| LO to RF leakage | | ISO _{LR} | | -40 | | dBm |
| RF to IF isolation | | ISO _{RI} | | -32 | -23 | dB |
| Attenuator Range | | Range | | 25.5 | | dB |

F1300 SPECIFICATION - CONTINUED

Refer to Typical Application Circuit when operated with $V_{CC} = +5.0V$, $T_{CASE} = 25C$, , $F_{RF} = 860 \text{ MHz}$, $F_{LO} = 1060 \text{ MHz}$, Gain = G_{MAX} , $P_{LO} = 0 \text{ dBm}$, $T_C = +25^\circ C$, STBY = GND, unless otherwise noted. Full Lineup measured through to I or Q path. IF Transformers and RF trace losses de-embedded.

| Parameter | Comment | Symbol | Min | Typ | Max | Units | |
|--|---|---------------------|-----|------------|------------|-------|--|
| Attenuator Glitching | <ul style="list-style-type: none"> ▪ Step from 15.5 to 16 dB ▪ Step from 16 to 15.5 dB ▪ Measure maximum excursion | ATTN _G | | 0.5 | | dB | |
| Attenuator Step Accuracy | | DNL | | 0.2 | | dB | |
| Attenuator Abs. Accuracy | | INL | | 0.2 | 0.5 | dB | |
| Attenuator Resolution | | LSB | | 0.5 | | dB | |
| Serial Clock Speed | SPI 3 wire bus | F _{CLOCK} | | 20 | 50 | MHz | |
| Data to Clock Setup | SPI 3 wire bus | T _S | 3 | | | ns | |
| Data to Clock Hold | SPI 3 wire bus | T _H | 3 | | | ns | |
| Clock to CS Setup | SPI 3 wire bus | T _{EN} | 3 | | | ns | |
| Clock Pulse Width | SPI 3 wire bus | T _W | 5 | | | ns | |
| LO Switch Isolation | | ISO _{LOSW} | | -45 | -36 | dB | |
| RF Switch Isolation | | ISO _{RFSW} | | -45 | -43 | dB | |
| RF Switch and attenuator settling times³ | | | | | | | |
| EN bit on | <ul style="list-style-type: none"> • LO_INA: 1050MHz, +3dBm • RF_INX: 850MHz, -10dBm | EN _{ON} | | 100 | | nsec | |
| EN bit off | | EN _{OFF} | | 50 | | | |
| RF switched X to Y (no Y signal) | | RF _{SWXY} | | 130 | | | |
| RF switched Y to X (no Y signal) | | RF _{SWYX} | | 200 | | | |
| LO switched A to B (no B signal) | | LO _{SWAB} | | 40 | | | |
| LO switched B to A (no B signal) | | LO _{SWBA} | | 20 | | | |
| Attenuator switched 0dB to 25.5dB (max) | | ATT _{SETL} | | | 300 | | |
| Attenuator switched 25.5dB (max) to 0dB | | | | | 300 | | |
| Attenuator switched 15.5dB to 16dB | | | | | 250 | | |
| Attenuator switched 16dB to 15.5dB | | | | | 300 | | |

SPECIFICATION NOTES:

- 1 – Items in min/max columns in **bold italics** are Guaranteed by Test
- 2 – All other Items in min/max columns are Guaranteed by Design Characterization
- 3 – Excludes SPI write time

POWER-ON SEQUENCE

The power-on sequence ensures F1300 works in default mode once powered on. If the F1300 is programmed after applying DC power, the following power-on sequence is not needed.

The power-on sequence should be:

1. CSb & SW_LATCH must be set low at power-on
2. Once powered on, first set SW_LATCH high, then set CSb high
3. Proceed with normal programming.

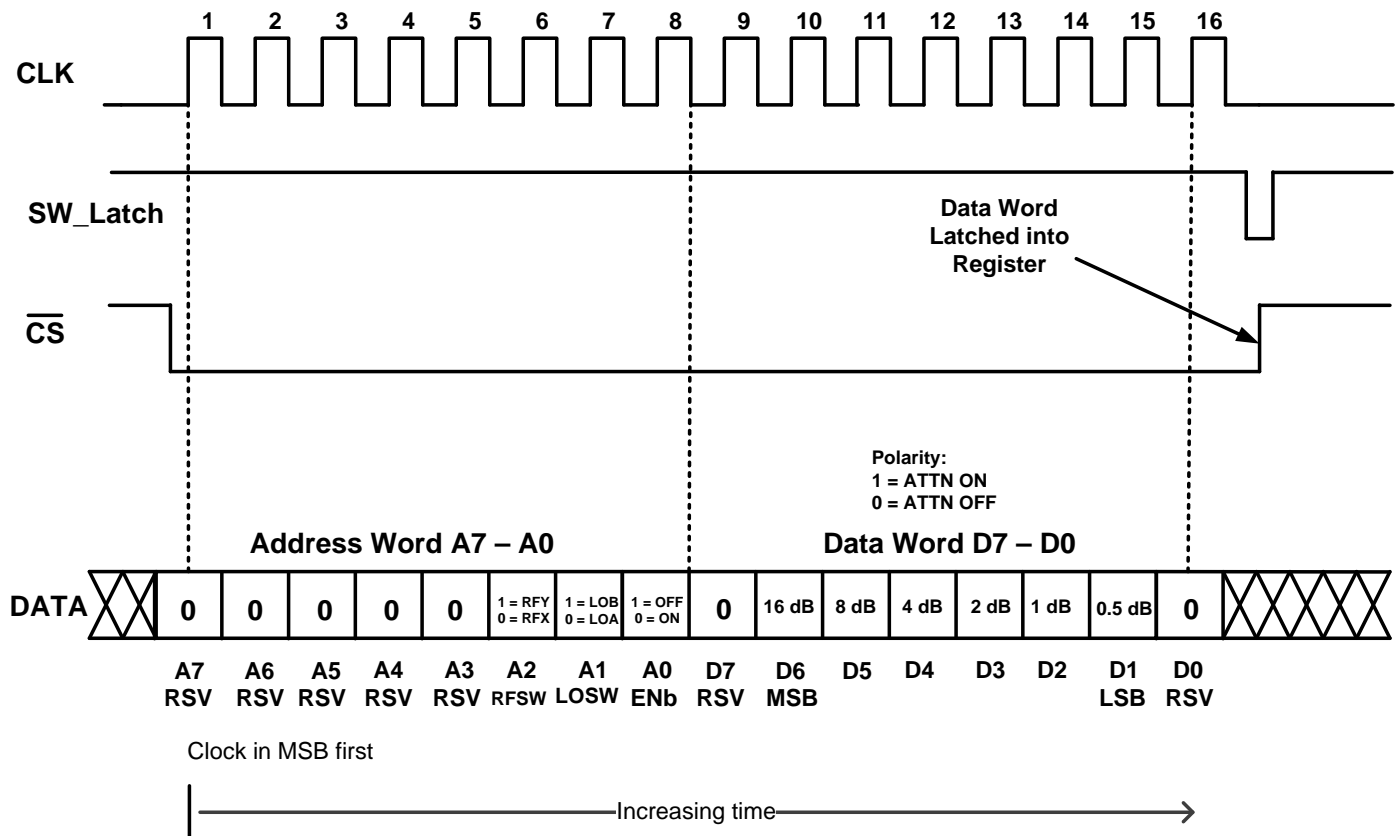
The default state after using power-on sequence:

- Maximum attenuation
- RF_INX, LO_INA selected
- Normal operation (not Standby Mode)

SERIAL PROGRAMMING

The device is programmed via the serial port by asserting Chip Select (CSb). Note: Most-Significant-Bit first, where the Address Word is the Most-Significant-Byte.

Serial mode timing diagram high level:

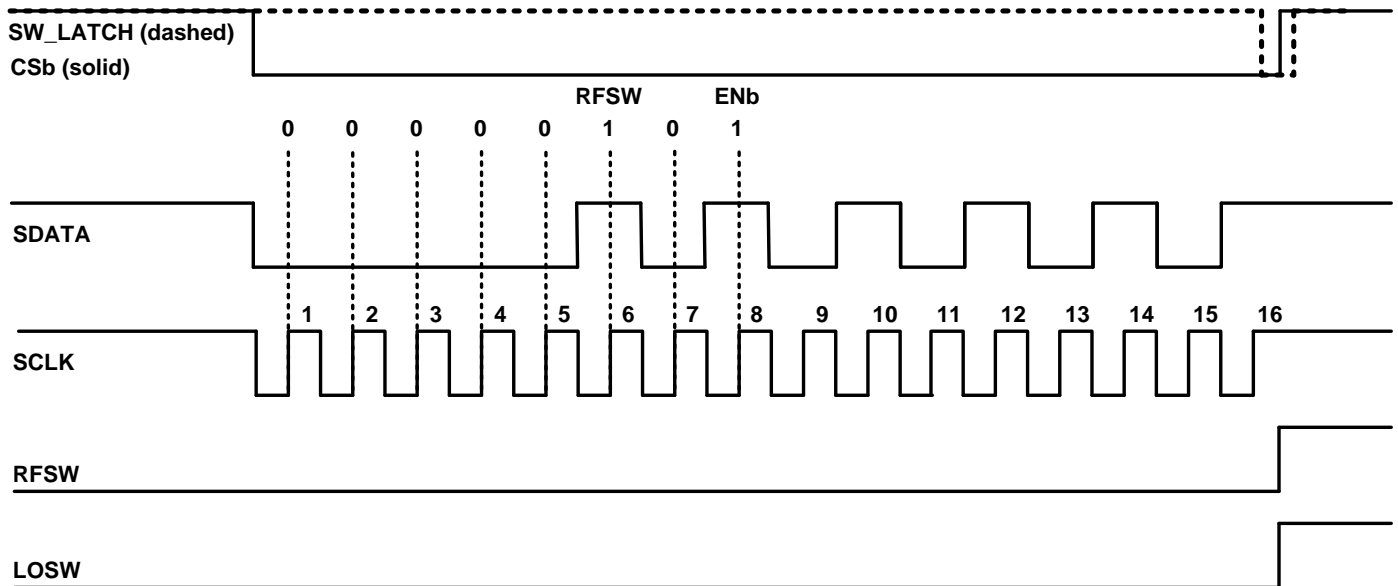


TO PROGRAM THE SERIAL INTERFACE:

If CSb is de-asserted (set to high), the serial interface will ignore the CLK line. Once CSb is asserted (set to low), the serial interface will recognize the CLK and any data present on DATA will be clocked into the registers with each rising CLK edge. After the 16th CLK cycle, and before the 17th CLK cycle, CSb must be de-asserted to successfully program the part with the desired bytes. If CSb is de-asserted before the 16th CLK cycle, or after the 17th CLK cycle, there is no guarantee that the correct bytes will be programmed and the user will have to re-program the interface in accordance with the aforementioned procedure.

SW_LATCH PROGRAMMING SEQUENCE

- When SW_LATCH is pinned high during the programming sequence, “RFSW” and “ENb” registers cannot be programmed and therefore will not toggle.
- If SW_LATCH is pinned low during the programming sequence, the “RFSW” and “ENb” register will toggle. This can be prevented with the “Programming Sequence” below.



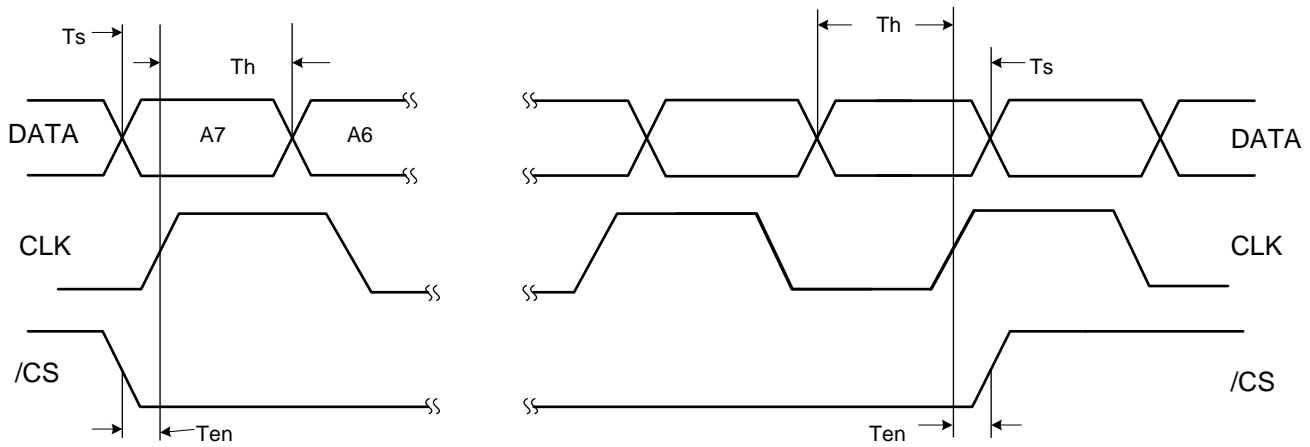
SEQUENCE FOR PROGRAMMING REGISTERS A<2>:A<0>

- 1) SW_Latch = 1; CSb = 0
- 2) CLK in 8- or 16-bit word, *do not de-assert (pull high) CSb*
- 3) Set SW_LATCH = 0 while CSb = 0 remains)
- 4) With SW_Latch = 0, set CSb = 1
- 5) Set SW_Latch = 1
- 6) Program complete

SPECIAL NOTE REGARDING PHASE OF I & Q:

- When LO is high-side injected, IF_I leads IF_Q by 90 degrees
- When LO is low-side injected, IF_Q leads IF_I by 90 degrees

SERIAL MODE TIMING DIAGRAM ZOOM:



- Data is shifted with the rising edge of CLK when /CS is low
- The rising edge of /CS latches data into the device

LOGIC TRUTH TABLE:

| STBY | SW_LATCH | MODE | WRITE ACCESS |
|------|----------|----------------|-------------------------------|
| 0 | 0 | Operating Mode | A2:A0 Enabled, D7:D0 Enabled |
| 0 | 1 | Operating Mode | A2:A0 Disabled, D7:D0 Enabled |
| 1 | 0 | Off | A2:A0 Enabled, D7:D0 Enabled |
| 1 | 1 | Off | A2:A0 Disabled, D7:D0 Enabled |

F1300 ATTENUATION TABLE

The F1300 gain/attenuation setting is controlled by 6 bits in the data word. The device provides an added attenuation range from 0 dB to 25.5 dB in 0.5 dB steps. A “high” or “1” bit corresponds to attenuation stepped IN, while a “low” or “0” bit corresponds to attenuation stepped OUT.

| F1300 DPD Demodulator - Attenuation Table (Data Word D7-D0) | | | | | | |
|--|-----|------------------|--|----------|-----|------------------|
| BINARY | HEX | Added Atten (dB) | | BINARY | HEX | Added Atten (dB) |
| 00000000 | 00 | 0 | | 00110100 | 34 | 13 |
| 00000010 | 02 | 0.5 | | 00110110 | 36 | 13.5 |
| 00000100 | 04 | 1 | | 00111000 | 38 | 14 |
| 00000110 | 06 | 1.5 | | 00111010 | 3A | 14.5 |
| 00001000 | 08 | 2 | | 00111100 | 3C | 15 |
| 00001010 | 0A | 2.5 | | 00111110 | 3E | 15.5 |
| 00001100 | 0C | 3 | | 01000000 | 40 | 16 |
| 00001110 | 0E | 3.5 | | 01000010 | 42 | 16.5 |
| 00010000 | 10 | 4 | | 01000100 | 44 | 17 |
| 00010010 | 12 | 4.5 | | 01000110 | 46 | 17.5 |
| 00010100 | 14 | 5 | | 01001000 | 48 | 18 |
| 00010110 | 16 | 5.5 | | 01001010 | 4A | 18.5 |
| 00011000 | 18 | 6 | | 01001100 | 4C | 19 |
| 00011010 | 1A | 6.5 | | 01001110 | 4E | 19.5 |
| 00011100 | 1C | 7 | | 01010000 | 50 | 20 |
| 00011110 | 1E | 7.5 | | 01010010 | 52 | 20.5 |
| 00100000 | 20 | 8 | | 01010100 | 54 | 21 |
| 00100010 | 22 | 8.5 | | 01010110 | 56 | 21.5 |
| 00100100 | 24 | 9 | | 01011000 | 58 | 22 |
| 00100110 | 26 | 9.5 | | 01011010 | 5A | 22.5 |
| 00101000 | 28 | 10 | | 01011100 | 5C | 23 |
| 00101010 | 2A | 10.5 | | 01011110 | 5E | 23.5 |
| 00101100 | 2C | 11 | | 01100000 | 60 | 24 |
| 00101110 | 2E | 11.5 | | 01100010 | 62 | 24.5 |
| 00110000 | 30 | 12 | | 01100100 | 64 | 25 |
| 00110010 | 32 | 12.5 | | 01100110 | 66 | 25.5 |

Because the first and last bits of the Data Word are not presently used by the F1300, two additional hex character pairs exists for each of those in this table. For example, data words of either H00, H80, or H01 (binary “00000000,” “10000000,” or 00000001) will place the F1300 in its minimum attenuation state. Likewise, data words of either H66, HE6, or H67 (binary “01100110” or “11100110” or “01100111”) will place the F1300 in its maximum attenuation state of 25.5 added attenuation.

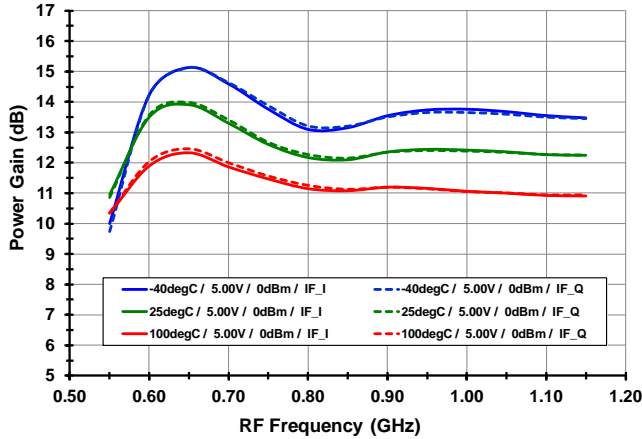
TYPICAL OPERATING CONDITIONS

Unless otherwise noted, for the TOC graphs, the following conditions apply

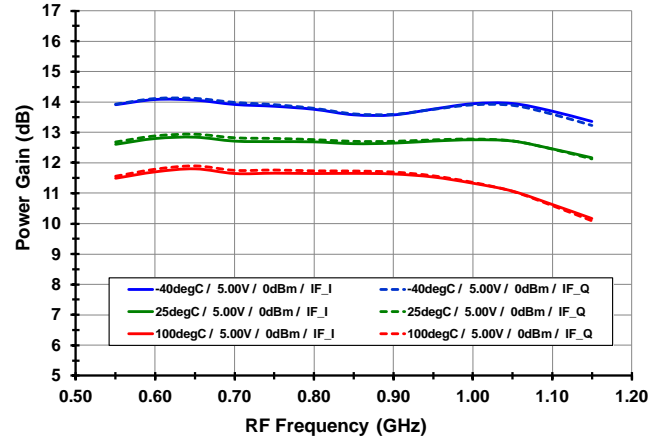
- IF = 200 MHz
- Tone spacing = 5 MHz
- Pout ~ 1 dBm
- Pin = -11 dBm
- RF_X, LO_A, IF_I selected
- Attenuation Setting = 0 dB (min ATTN or G_{MAX})
- T_{CASE} = 25C
- V_{CC} = 5.00 V
- LO level = 0 dBm
- Output Transformer losses are de-embedded
- Input RF trace losses are de-embedded

TOCs [Fixed IF] (-1-)

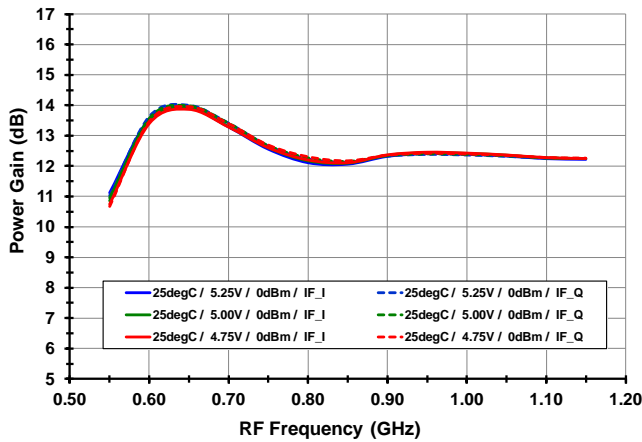
GAIN vs. T_{CASE} [Low Side Injection]



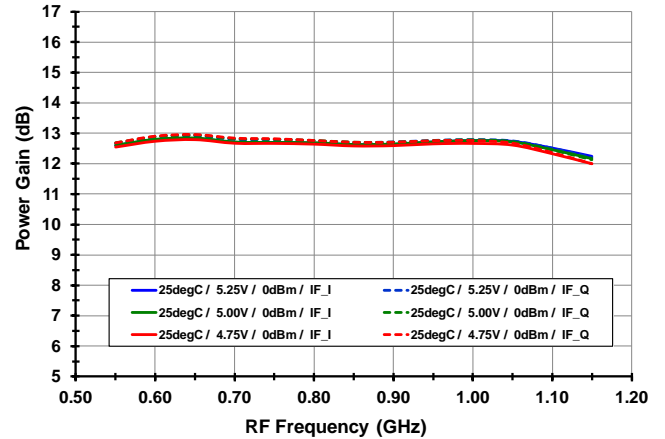
GAIN vs. T_{CASE} [High Side Injection]



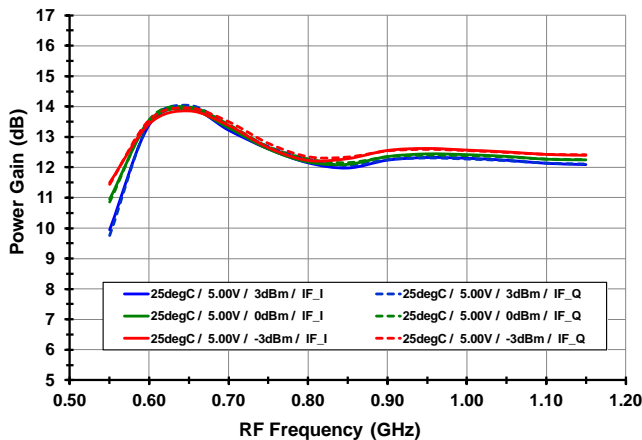
GAIN vs. V_{CC} [Low Side Injection]



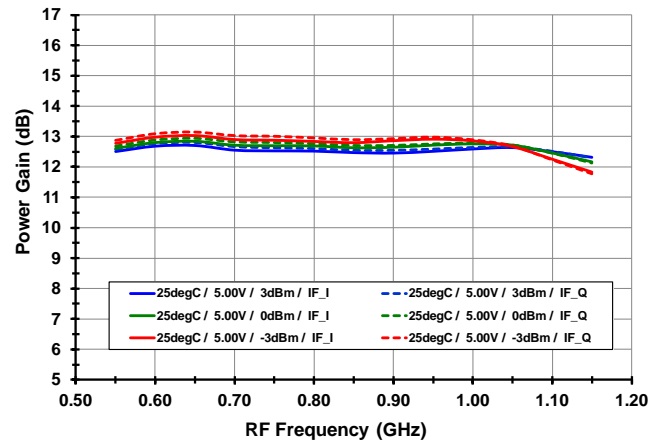
GAIN vs. V_{CC} [High Side Injection]



GAIN vs. LO level [Low Side Injection]

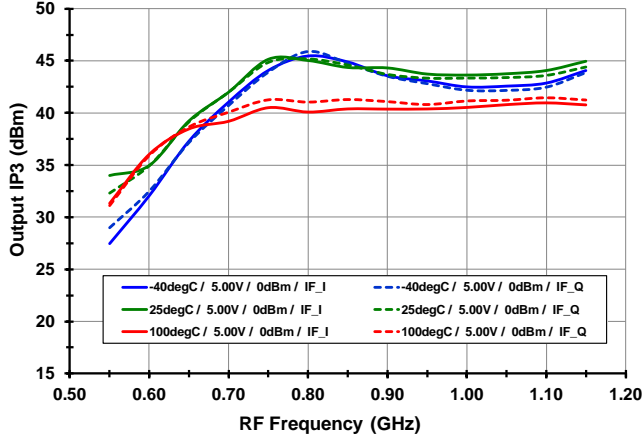


GAIN vs. LO level [High Side Injection]

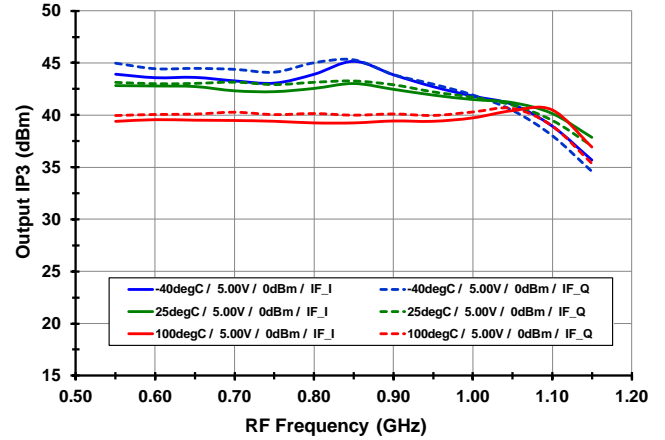


TOCs [Fixed IF] (-2-)

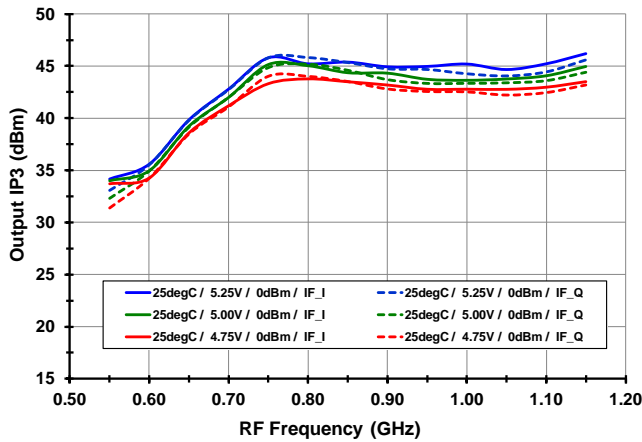
IP_{3O} vs. T_{CASE} [Low Side Injection]



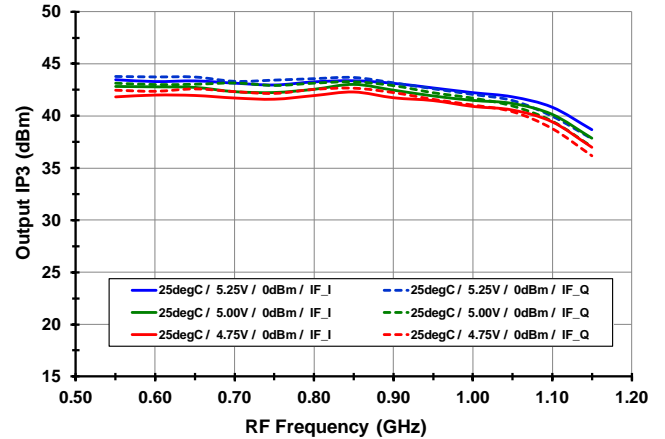
IP_{3O} vs. T_{CASE} [High Side Injection]



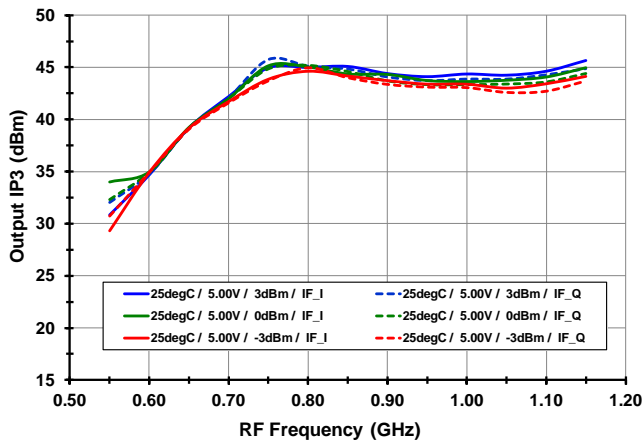
IP_{3O} vs. V_{CC} [Low Side Injection]



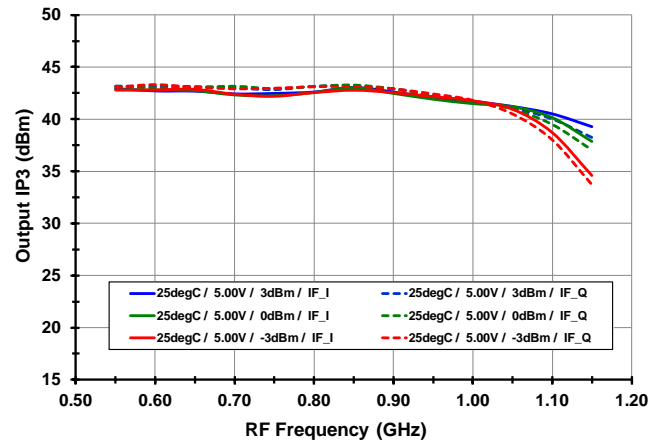
IP_{3O} vs. V_{CC} [High Side Injection]



IP_{3O} vs. LO level [Low Side Injection]

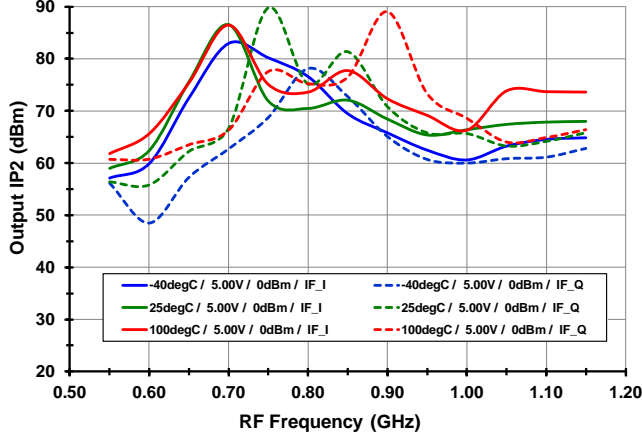


IP_{3O} vs. LO level [High Side Injection]

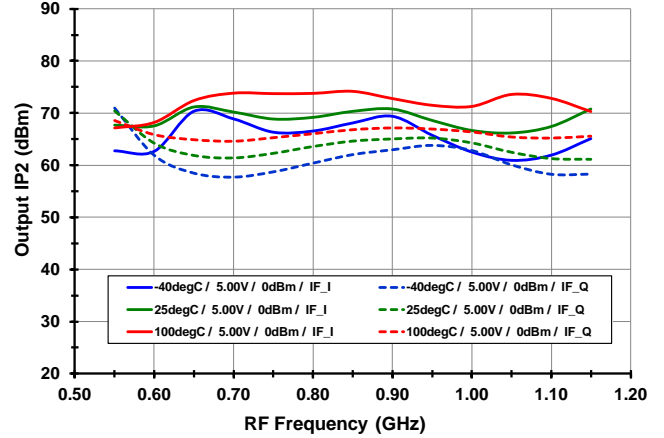


TOCs [Fixed IF] (-3-)

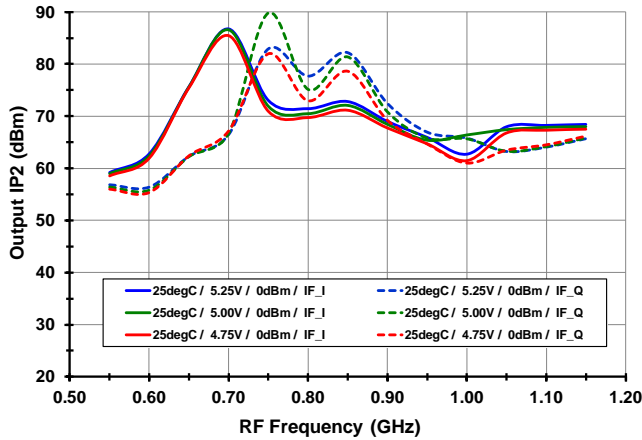
IP2_O vs. T_{CASE} [Low Side Injection]



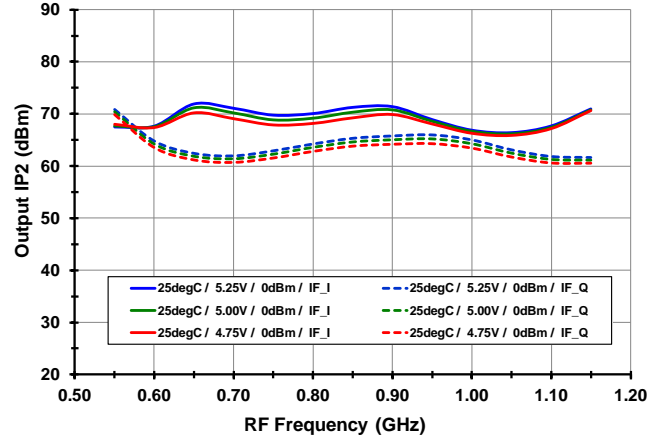
IP2_O vs. T_{CASE} [High Side Injection]



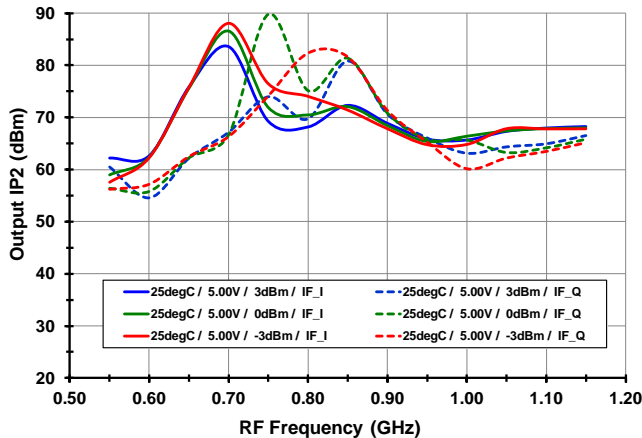
IP2_O vs. V_{CC} [Low Side Injection]



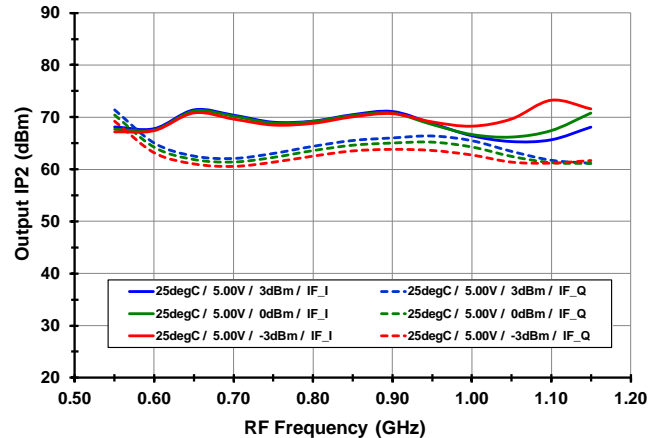
IP2_O vs. V_{CC} [High Side Injection]



IP2_O vs. LO level [Low Side Injection]

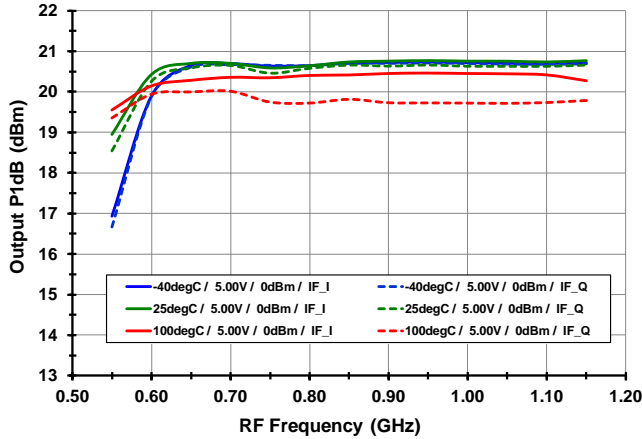


IP2_O vs. LO level [High Side Injection]

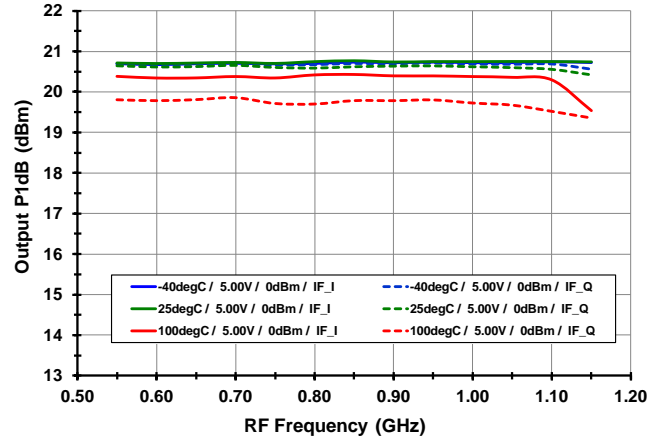


TOCs [Fixed IF] (-4-)

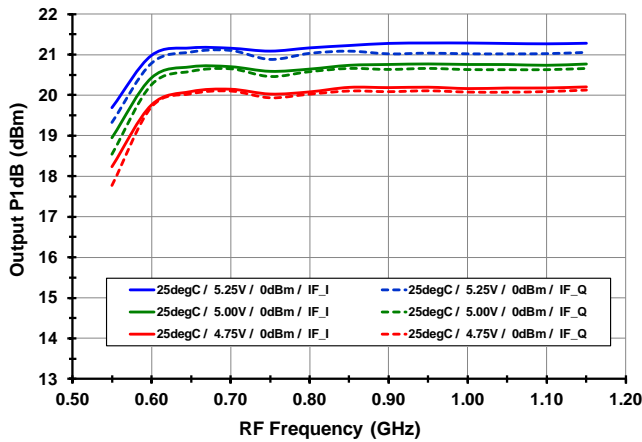
P1dB₀ vs. T_{CASE} [*Low Side Injection*]



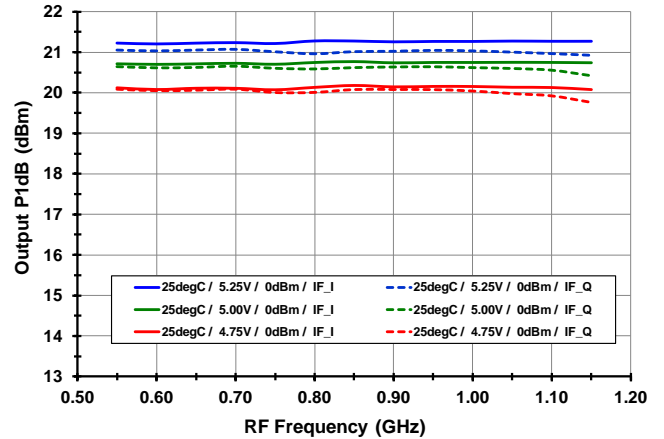
P1dB₀ vs. T_{CASE} [*High Side Injection*]



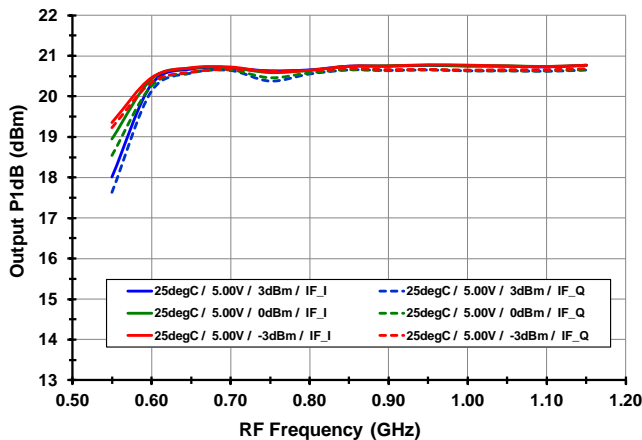
P1dB₀ vs. V_{CC} [*Low Side Injection*]



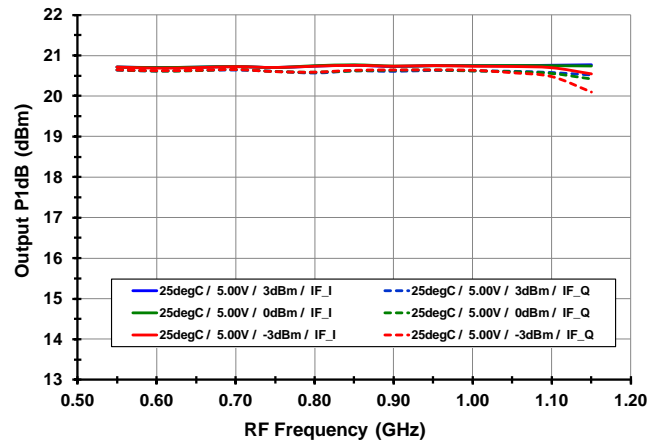
P1dB₀ vs. V_{CC} [*High Side Injection*]



P1dB₀ vs. LO level [*Low Side Injection*]

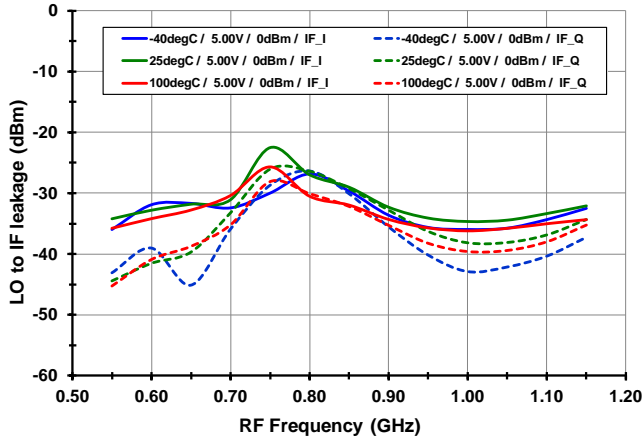


P1dB₀ vs. LO level [*High Side Injection*]

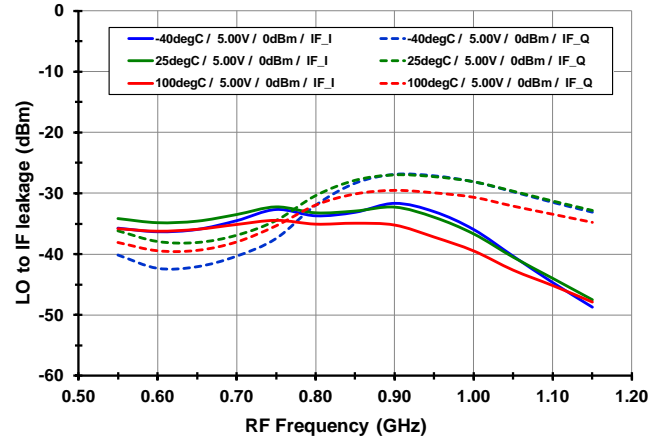


TOCs [Fixed IF] (-5-)

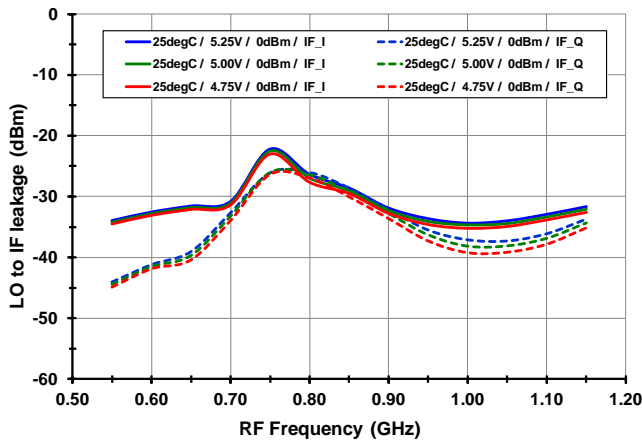
LO to IF vs. T_{CASE} [*Low Side Injection*]



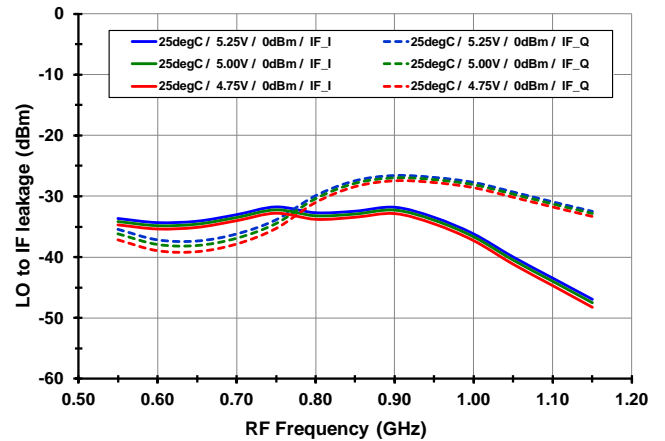
LO to IF vs. T_{CASE} [*High Side Injection*]



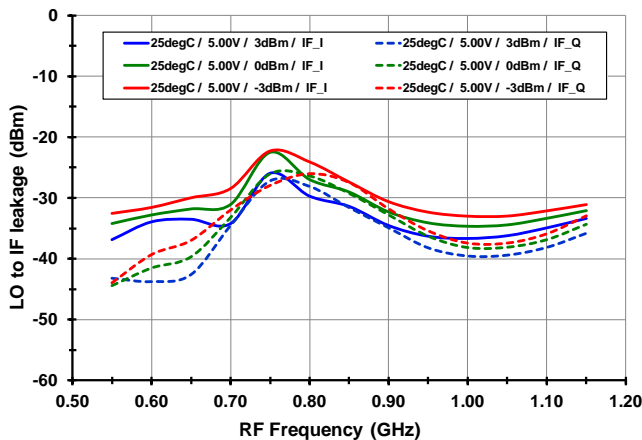
LO to IF vs. V_{CC} [*Low Side Injection*]



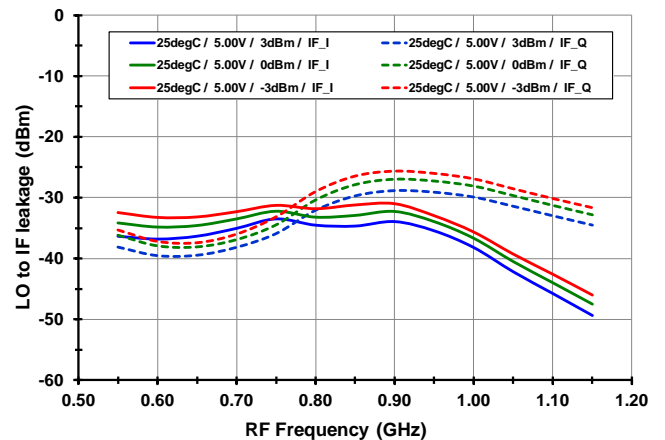
LO to IF vs. V_{CC} [*High Side Injection*]



LO to IF vs. LO level [*Low Side Injection*]

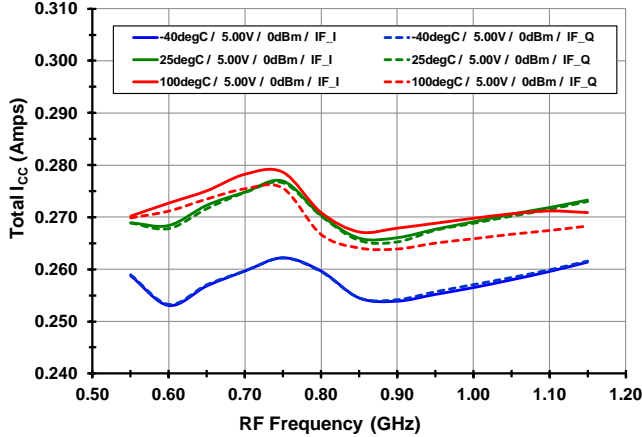


LO to IF vs. LO level [*High Side Injection*]

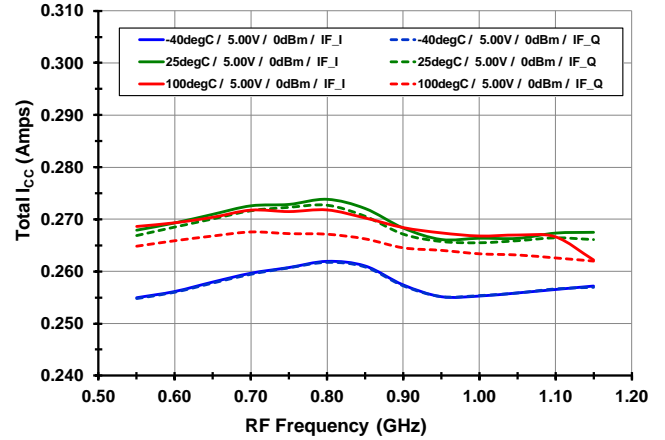


TOCs [Fixed IF] (-6-)

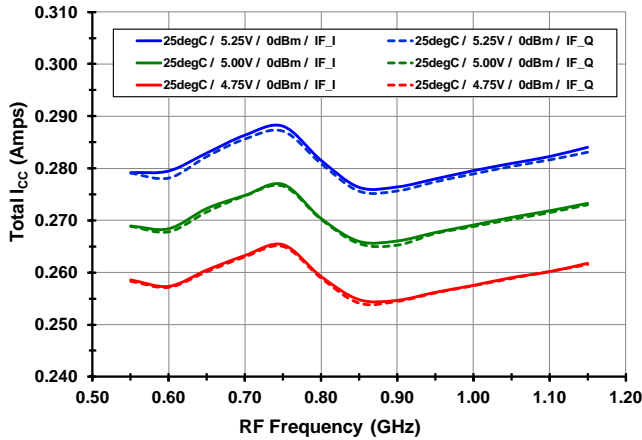
I_{CC} vs. T_{CASE} [Low Side Injection]



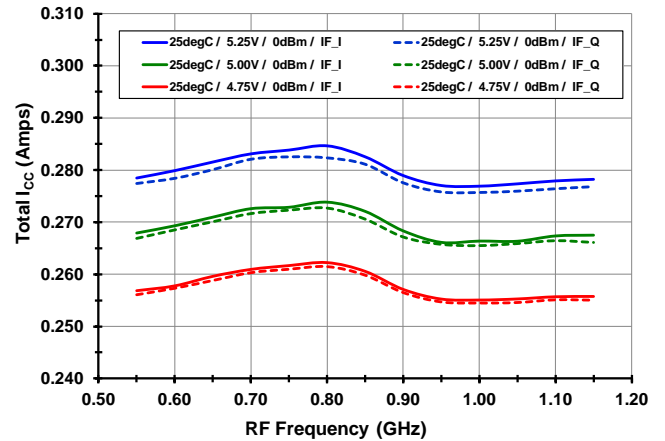
I_{CC} vs. T_{CASE} [High Side Injection]



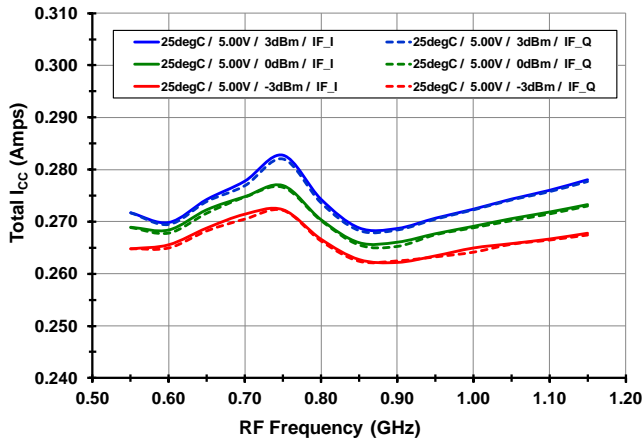
I_{CC} vs. V_{CC} [Low Side Injection]



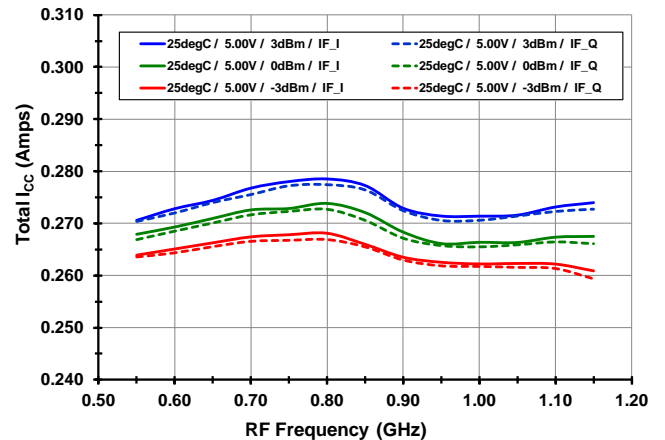
I_{CC} vs. V_{CC} [High Side Injection]



I_{CC} vs. LO level [Low Side Injection]

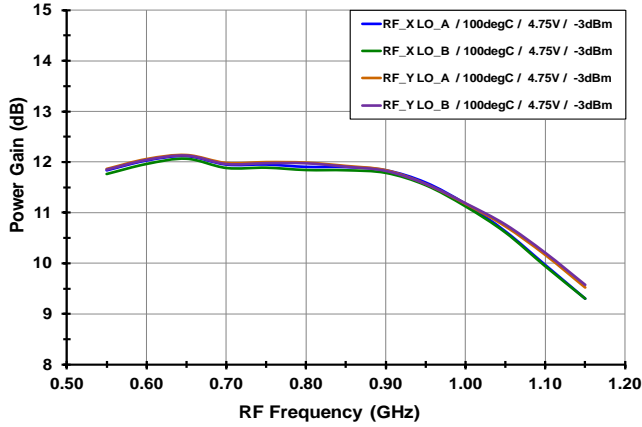


I_{CC} vs. LO level [High Side Injection]

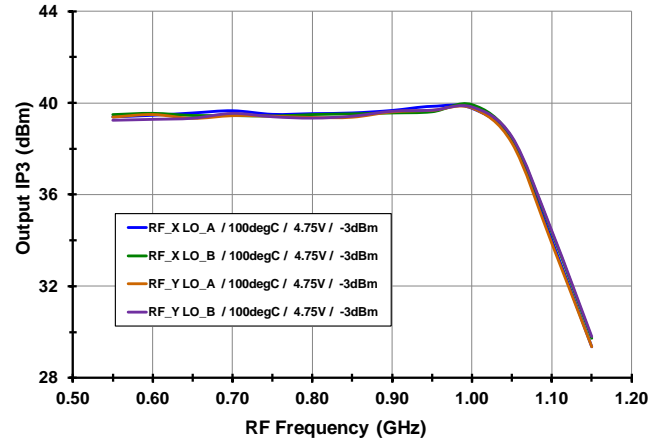


TOCs [vs. Switch Configuration, Extreme Conditions, IF_I only] (-7-)

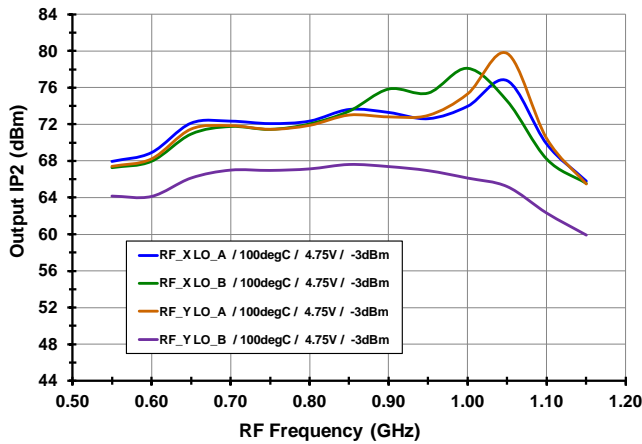
Gain [*High Side Injection*]



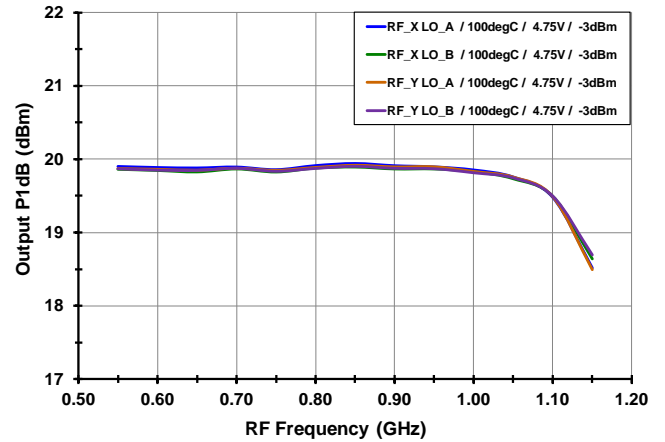
Output IP3 [*High Side Injection*]



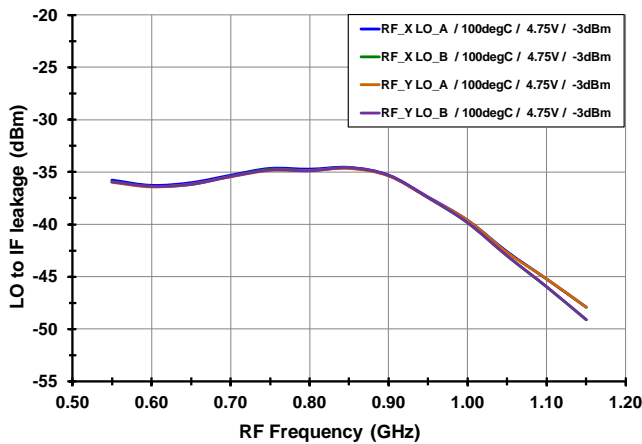
Output IP2 [*High Side Injection*]



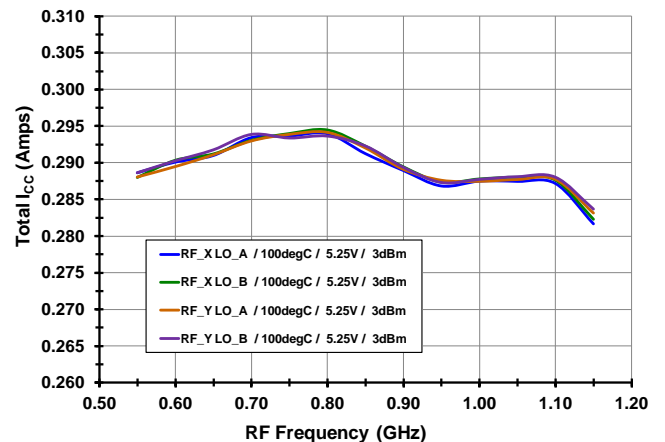
Output P1dB [*High Side Injection*]



LO to IF [*High Side Injection*]

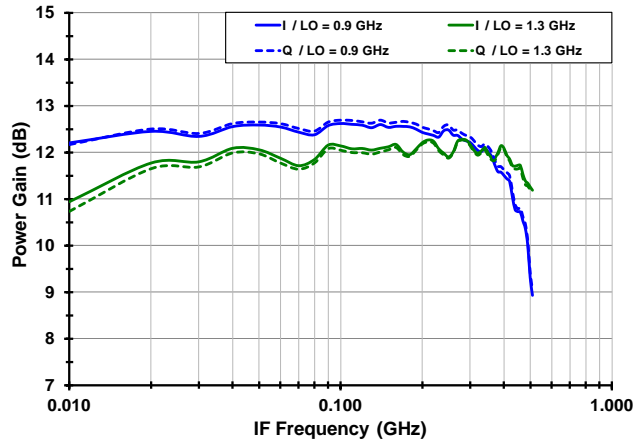


I_{CC} [*High Side Injection*]

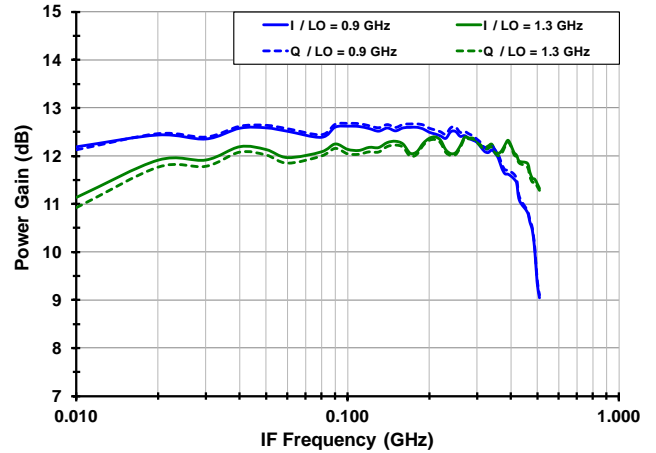


TOCs [Fixed LO] (-8-)

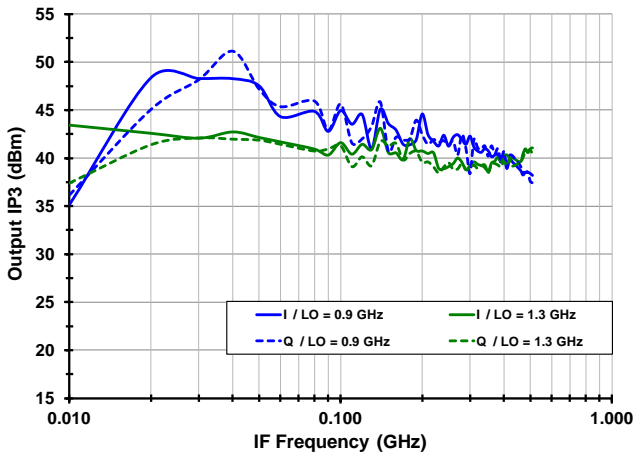
Gain Flatness [High Side Injection, RF_X LO_A]



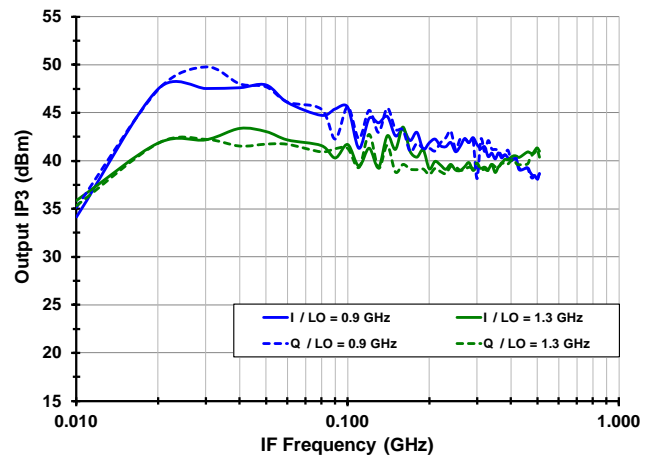
Gain Flatness [High Side Injection, RF_Y LO_B]



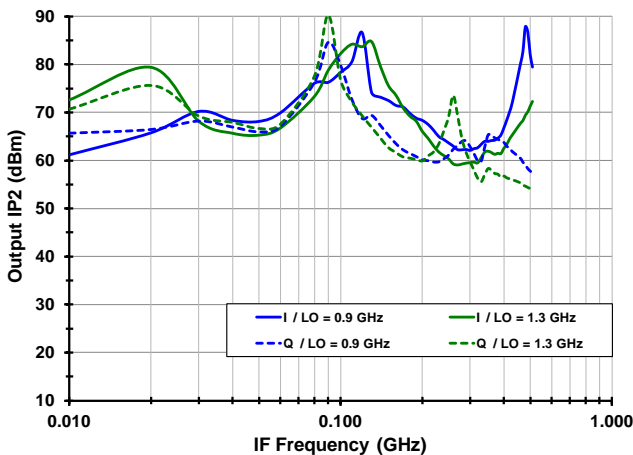
IP3₀ Flatness [High Side Injection, RF_X LO_A]



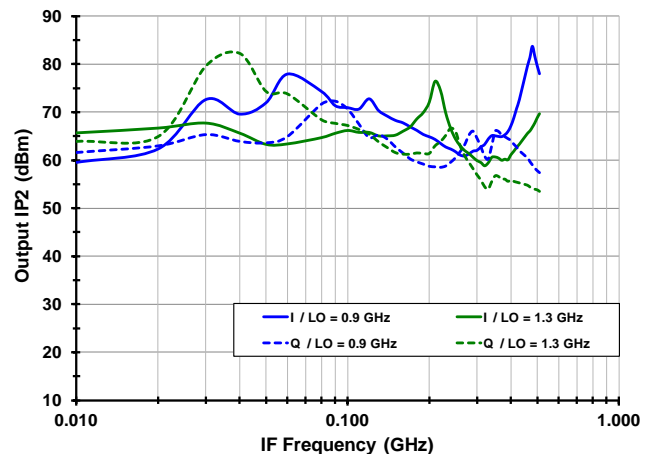
IP3₀ Flatness [High Side Injection, RF_Y LO_B]



IP2₀ Flatness [High Side Injection, RF_X LO_A]

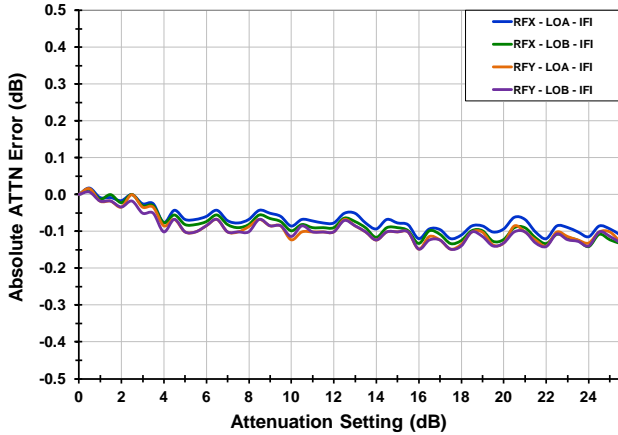


IP2₀ Flatness [High Side Injection, RF_Y LO_B]

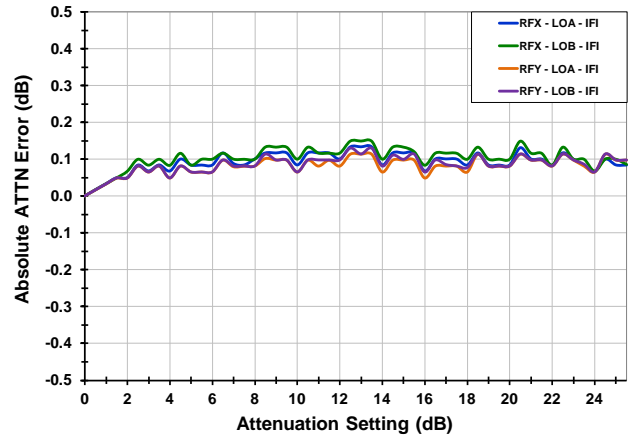


TOCs [vs. Attenuation Setting] (-9-)

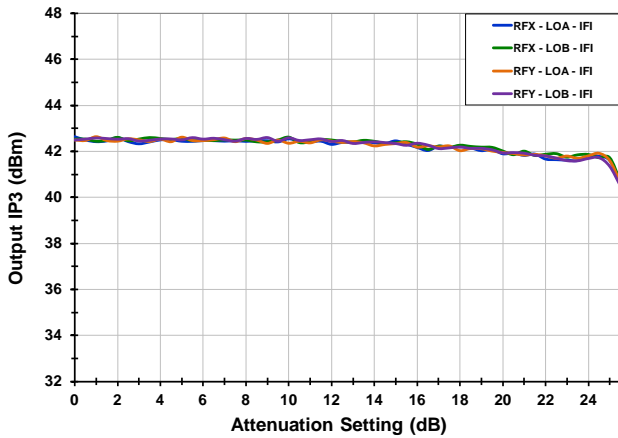
ATTN Accuracy [0.8 GHz RF, *HiSide* Inj.]



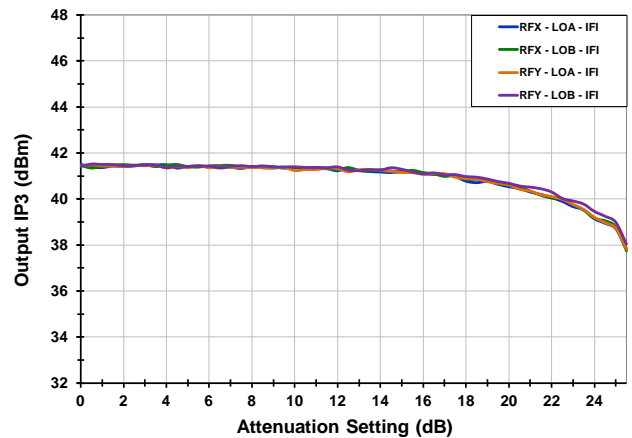
ATTN Accuracy [1.0 GHz RF, *HiSide* Inj.]



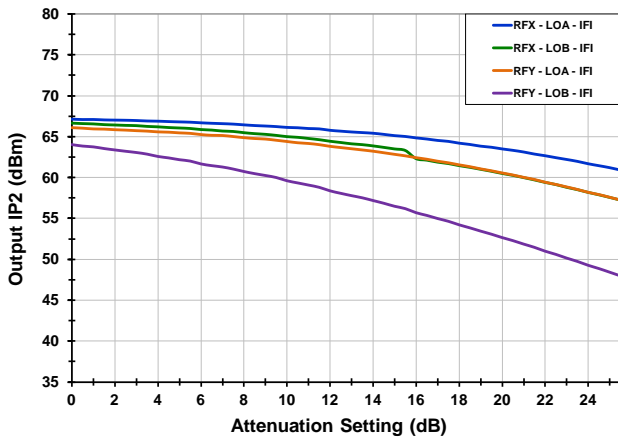
IP3_o [0.8 GHz RF, *HiSide* Inj.]



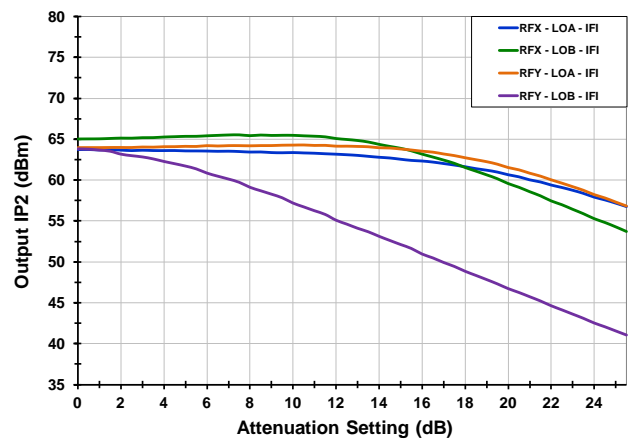
IP3_o [1.0 GHz RF, *HiSide* Inj.]



IP2_o [0.8 GHz RF, *HiSide* Inj.]

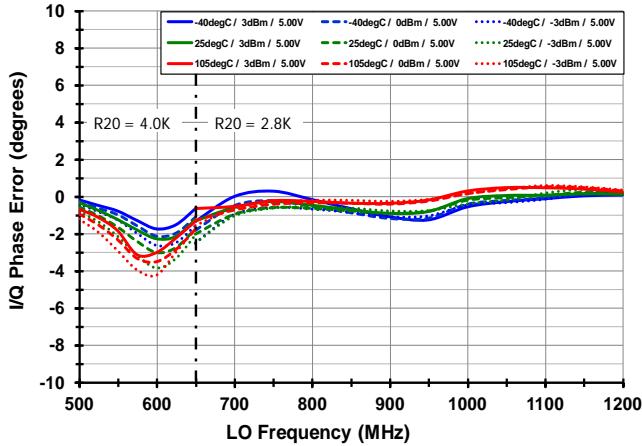


IP2_o [1.0 GHz RF, *HiSide* Inj.]

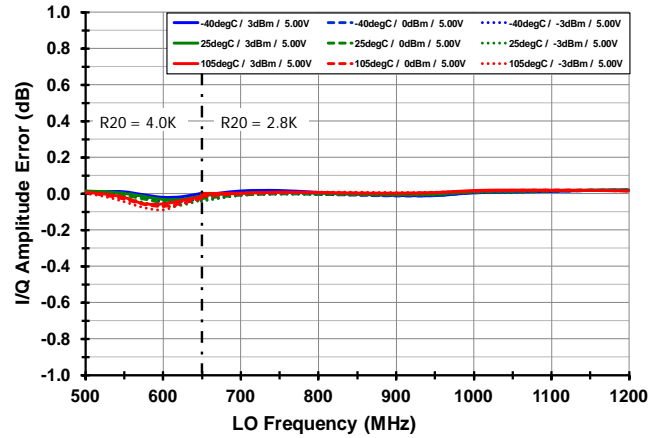


TOCs [Quadrature] (-10-)

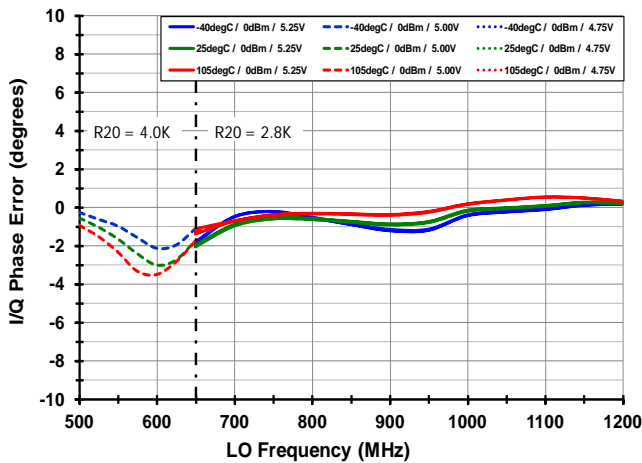
I/Q Phase Error vs. LO Level & T_{CASE}



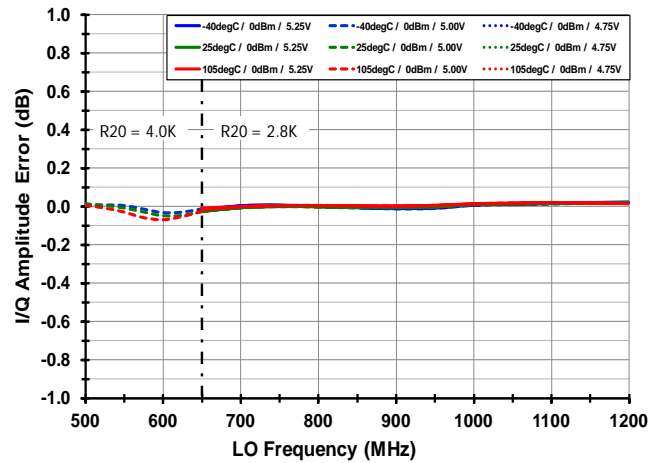
I/Q Amplitude Error vs. LO Level & T_{CASE}



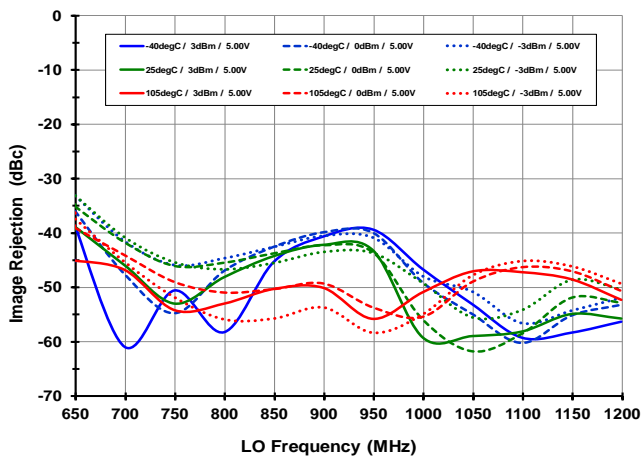
I/Q Phase Error vs. V_{CC} & T_{CASE}



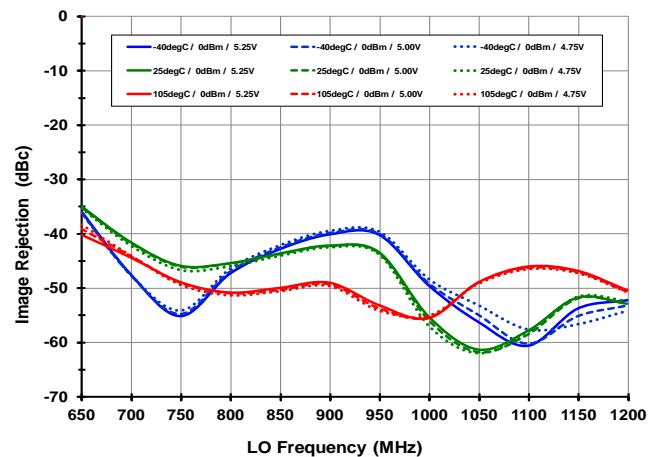
I/Q Amplitude Error vs. V_{CC} & T_{CASE}



I/Q Image Rejection vs. LO Level & T_{CASE}

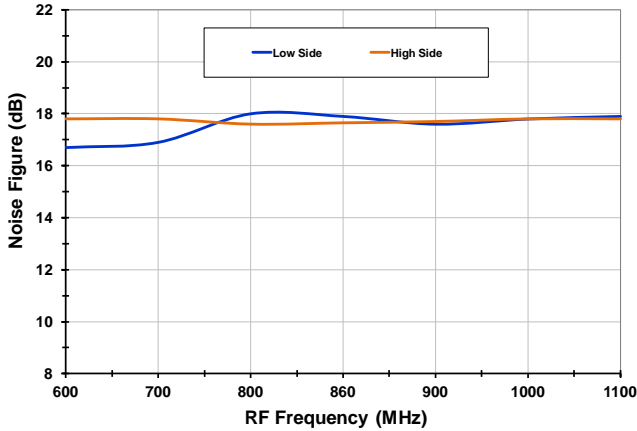


I/Q Image Rejection vs. V_{CC} & T_{CASE}

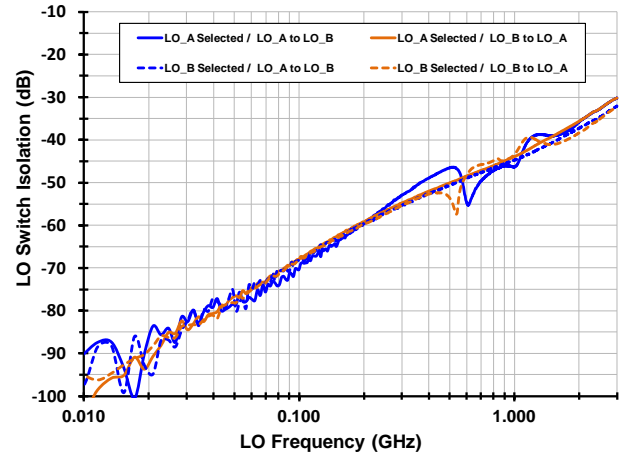


TOCs [NF, Switch Iso, Port Matches] (-11-)

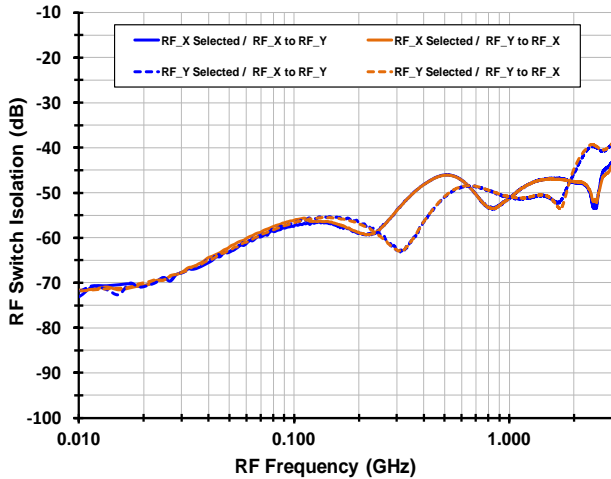
Noise Figure



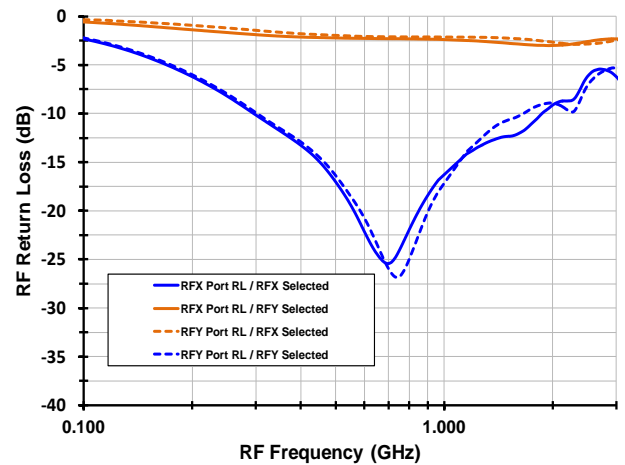
LO Switch Isolation



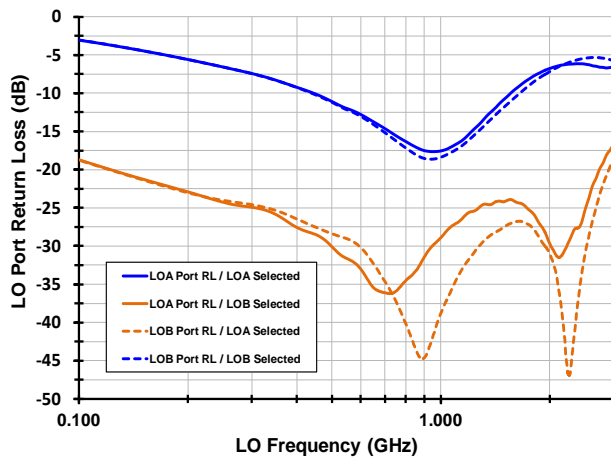
RF Switch Isolation



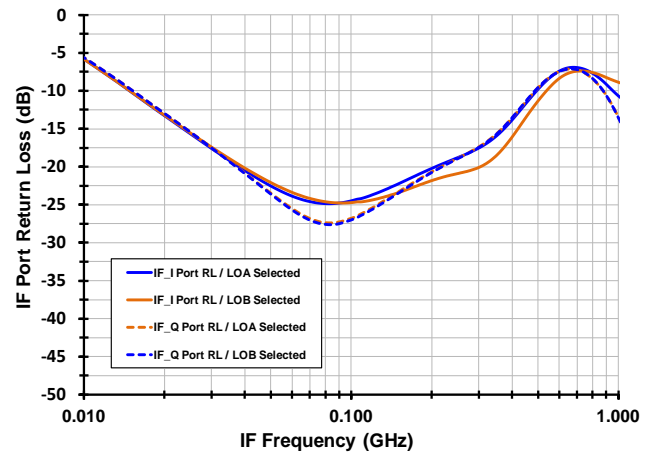
RF Port Return Loss [LO=1.06 GHz, LOA selected]



LO Port Return Loss



IF Port Return Loss



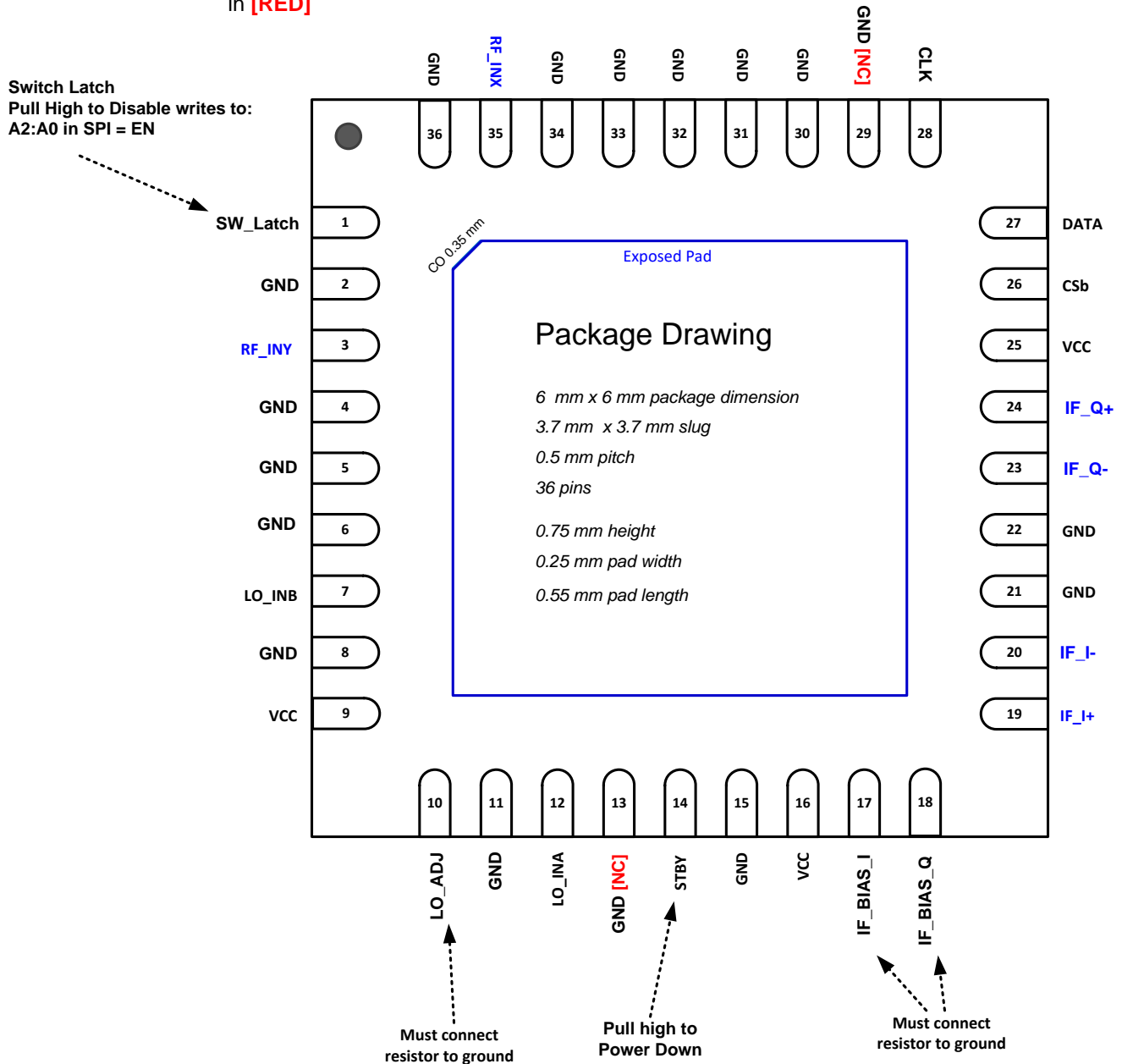
PACKAGE OUTLINE DRAWINGS

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

PIN DIAGRAM

Signal Path Inputs & Outputs in **BLUE**

Internal Connections in **[RED]**



PIN DESCRIPTIONS

| Pins | Name | Function |
|---|------------------------|--|
| 1 | SW_LATCH | Stand-by latch. Pull Low or Ground for Normal Operation. If left floating, this input will be internally pulled high, disabling SPI writes to ENb (Standby) and RF SW bits (A0, A2). |
| 2, 4, 5, 6, 8, 11, 15, 21, 22, 30, 31, 32, 33, 34, 36 | GND | Ground these Pins. |
| 3 | RF_INY | Alternate RF Input. Separated from RF_INX by internal SP2T. AC couple to this pin. Internally matched to 50 ohms |
| 7 | LO_INB | LO Input B. AC couple to this pin. Internally matched to 50 ohms. Selected via SPI port. |
| 9, 16, 25 | VCC | Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin. |
| 10 | LO_ADJ | Connect the specified resistor from this pin to ground to set the LO path I _{cc} . This IS a current setting resistor |
| 12 | LO_INA | LO Input A. AC couple to this pin. Internally matched to 50 ohms. Selected via SPI port. |
| 13, 29 | N.C. | No Connection. Not internally connected. OK to connect to V _{cc} . Recommended Connection is Ground |
| 14 | STBY | STBY Mode. Pull this pin high for Standby mode (30mA). Pull low or Ground for normal Operation |
| 17, 18 | IF_BIAS_I IF_BIAS_Q | Connect the specified resistor from this pin to ground to set the IF amplifier bias reference. This is NOT a current setting resistor |
| 19, 20 | IF_I+, IF_I- | <i>In-Phase</i> Mixer Differential IF Output. Connect pullup inductors from each of these pins to V _{cc} (see the Typical Application Circuit). |
| 23, 24 | IF_Q-, IF_Q+ | <i>Quadrature</i> Mixer Differential IF Output. Connect pullup inductors from each of these pins to V _{cc} (see the Typical Application Circuit). |
| 26 | CSb | Chip Select Bar. The falling edge initiates a programming cycle and the rising edge latches the programmed shift register data into the active register. |
| 27 | DATA | Serial Data Input |
| 28 | CLK | Serial Clock Input |
| 35 | RF_INX | Main RF Input. Separated from RF_INY by internal SP2T. AC couple to this pin. Internally matched to 50 ohms |
| | — EP | Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance. |
| | | |

CONTROL PIN VOLTAGE & RESISTANCE VALUES

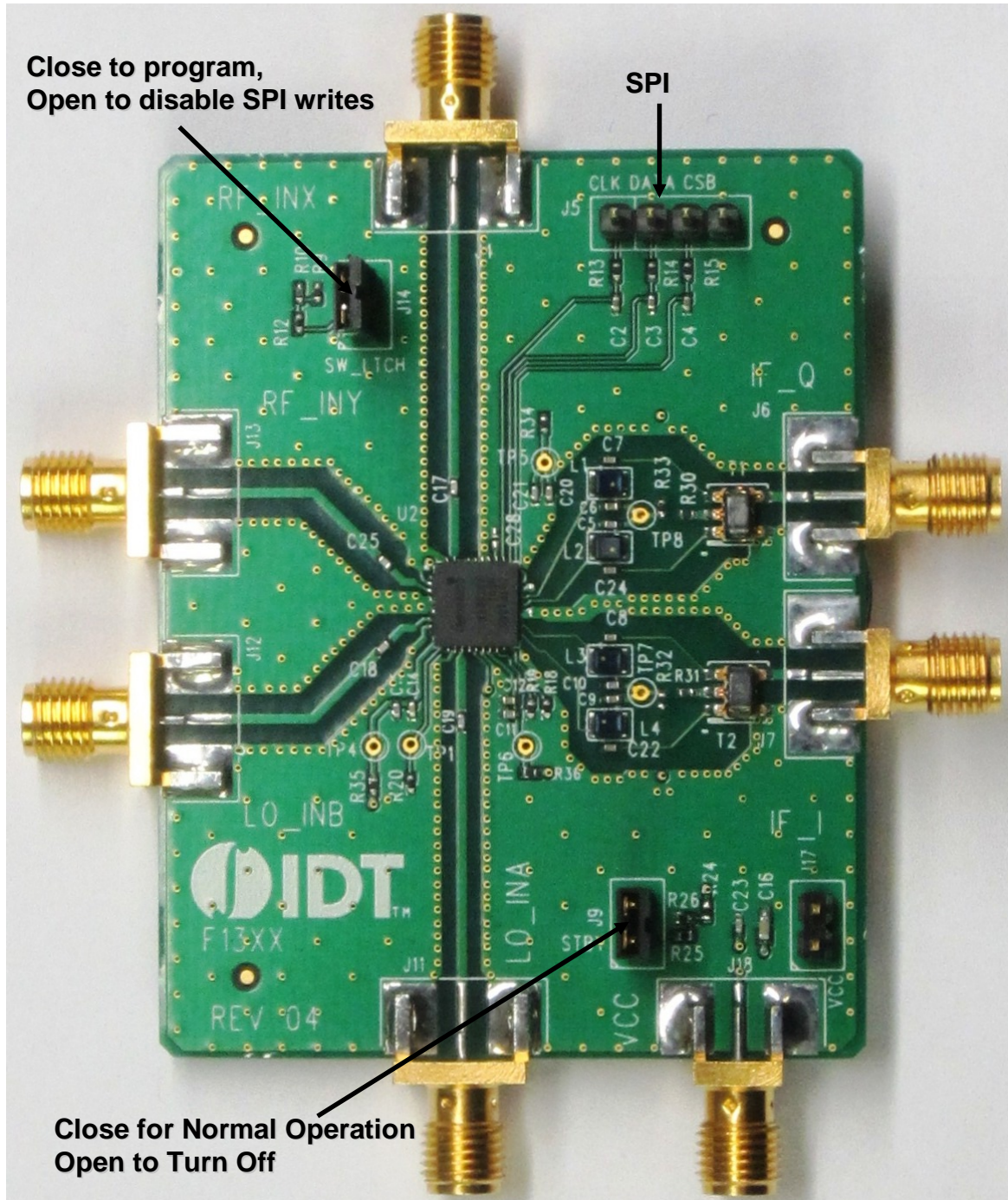
The following table provides open-circuit DC voltage and resistance values referenced to ground for each of the control pins listed.

| Pin | Name | DC voltage (volts) | Resistance (ohms) |
|-----|----------|--------------------|-------------------|
| 1 | SW_LATCH | 1.75 | 1.6M |
| 14 | STBY | 5 | 50k |
| 26 | CSb | 1.75 | 1.6M |
| 27 | DATA | 1.75 | 1.6M |
| 28 | CLK | 1.75 | 1.6M |

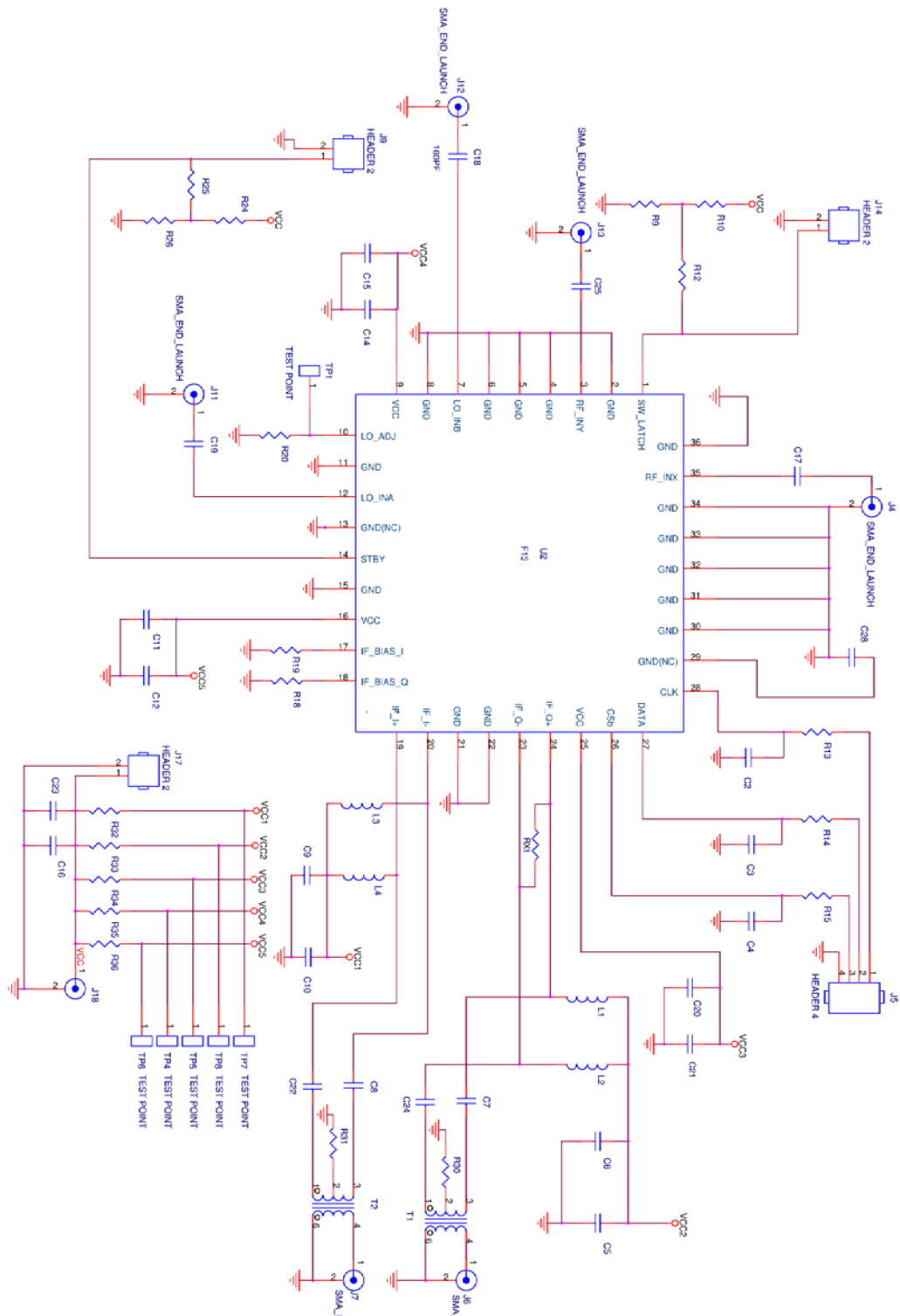
POWER SUPPLIES

All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than $1V/20\mu s$. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

EVKIT PICTURE / LAYOUT / OPERATION



EVKIT / APPLICATIONS CIRCUIT



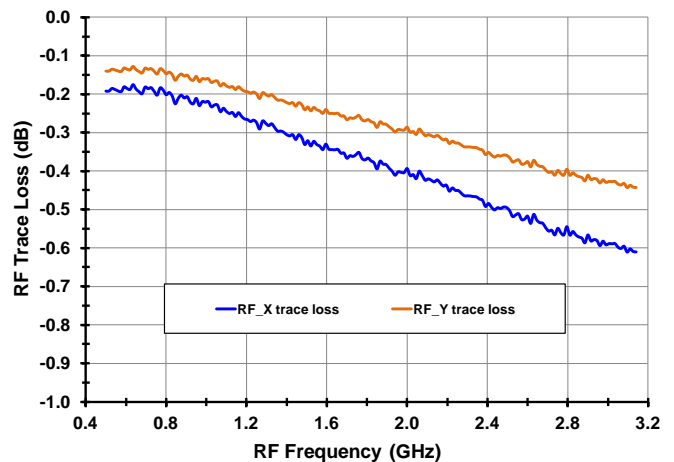
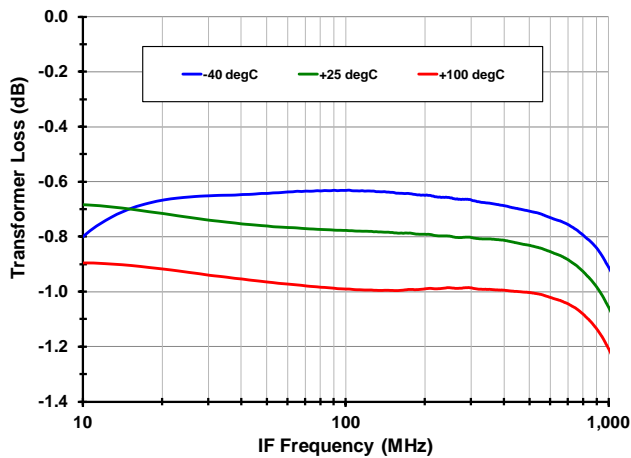
EVKIT BOM

F1300 BOM
9/17/2013

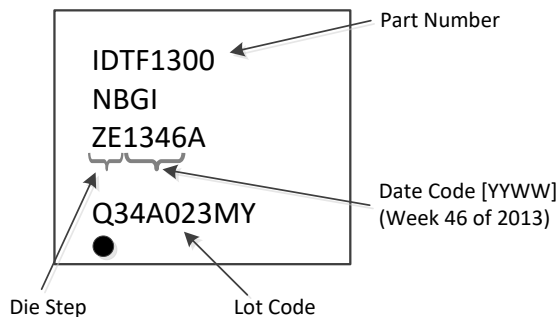
| Item # | Value | Size | Desc | Mfr. Part # | Mfr. | Supplier Part # | Supplier | Part Reference | Qty |
|--------|----------------|--------|-------------------------------------|--------------------|-----------------|------------------|-----------|-------------------------|-----|
| 1 | 100pF | 0402 | CAP CER 100PF 50V 5% NP0 0402 | GRM1555C1H101JZ01D | MURATA | 490-3458-1-ND | Digikey | C2-C4 | 3 |
| 2 | 10nF | 0402 | CAP CER 1000PF 16V 10% X7R 0402 | GRM155R71C103KA01D | MURATA | 490-1313-1-ND | Digikey | C6,7,8,9,12,14,21,22,24 | 9 |
| 3 | 1000pF | 0402 | CAP CER 1000PF 50V C0G 0402 | GRM1555C1H102JA01D | MURATA | 490-3244-1-ND | Digikey | C5,10,11,15,20,23 | 6 |
| 4 | 160pF | 0402 | CAP CER 160PF 50V 5% NP0 0402 | GRM1555C1H161JA01D | MURATA | 490-3230-1-ND | Digikey | C17,18,19,25 | 4 |
| 5 | 10uF | 0603 | CAP CER 10UF 6.3V X5R 0603 | GRM188R60J106ME47D | MURATA | 490-3896-1-ND | Digikey | C16 | 1 |
| 6 | Header 2 Pin | TH 2 | CONN HEADER VERT SGL 2POS GOLD | 961102-6404-AR | 3M | 3M9447-ND | Digikey | J9,14,17 | 3 |
| 7 | Header 4 Pin | TH 4 | CONN HEADER VERT SGL 4POS GOLD | 961104-6404-AR | 3M | 3M9449-ND | Digikey | J5 | 1 |
| 8 | SMA_END_LAUNCH | .062 | SMA_END_LAUNCH (Small) | 142-0711-821 | Emerson Johnson | 530-142-0711-821 | Mouser | J6,7,18 | 3 |
| 9 | SMA_END_LAUNCH | .062 | SMA_END_LAUNCH (Big) | 142-0701-851 | Emerson Johnson | 530-142-0701-851 | Mouser | J4,11,12,13 | 4 |
| 10 | 1uH | 0805 | 0805LS (2012) Ceramic Chip Inductor | 0805LS-102XJLB | COILCRAFT | 0805LS-102XJLB | COILCRAFT | L1,2,3,4 | 4 |
| 11 | 43K | 0402 | RES 43K OHM 1/10W 1% 0402 SMD | ERJ-2RKF4302X | Panasonic | P43.0KLCT-ND | Digikey | R10,24 | 2 |
| 12 | 75K | 0402 | RES 75K OHM 1/10W 1% 0402 SMD | ERJ-2RKF7502X | Panasonic | P75.0KLCT-ND | Digikey | R9,26 | 2 |
| 13 | 2.8K | 0402 | RES 2.8K OHM 1/10W 1% 0402 SMD | ERJ-2RKF2801X | Panasonic | P2.80KLCT-ND | Digikey | R20 (Note 1) | 1 |
| | 4.02K | 0402 | RES 4.02K OHM 1/10W 1% 0402 SMD | ERJ-2RKF4021X | Panasonic | P4.02KLCT-ND | Digikey | R20 (Note 2) | |
| 14 | 121 | 0402 | RES 121 OHM 1/10W 1% 0402 SMD | ERJ-2RKF1210X | Panasonic | P121LCT-ND | Digikey | R18,19 | 2 |
| 15 | 47K | 0402 | RES 47.0K OHM 1/16W 1% 0402 SMD | RC0402FR-0747KL | Yageo | 311-47.0KLRCT-ND | Digikey | R12,25 | 2 |
| 16 | 100 | 0402 | RES 100 OHM 1/10W 1% 0402 SMD | ERJ-2RKF1000X | Panasonic | P100LCT-ND | Digikey | R13-15 | 3 |
| 17 | 0 | 0402 | RES 0.0 OHM 1/10W 0402 SMD | ERJ-2GE0R00X | Panasonic | P0.0JCT-ND | Digikey | R30,31,32,33,34,35,36 | 7 |
| 18 | 1:4 Balun | SM-22 | SMT TRANSFORMER 10MHZ-1.9GHZ | RFXF6553-TR13 | RFMD | 689-1067-1-ND | Digikey | T1,2 | 2 |
| 19 | F1300 | QFN-36 | DPD Demodulator | F1300 | IDT | F1300 | IDT | U1 | 1 |
| 20 | PCB | 05 | Printed Circuit Board | F13XX REV 05 | | | SBC | | 1 |
| 21 | BOM | 02 | Bill Of Material | | | | | | |
| Total | | | | | | | | | 61 |

Note 1: Use this value for LO Freq Range 1 as specified in the Electrical Specification table in this datasheet
 Note 2: Use this value for LO Freq Range 2 as specified in the Electrical Specification table in this datasheet

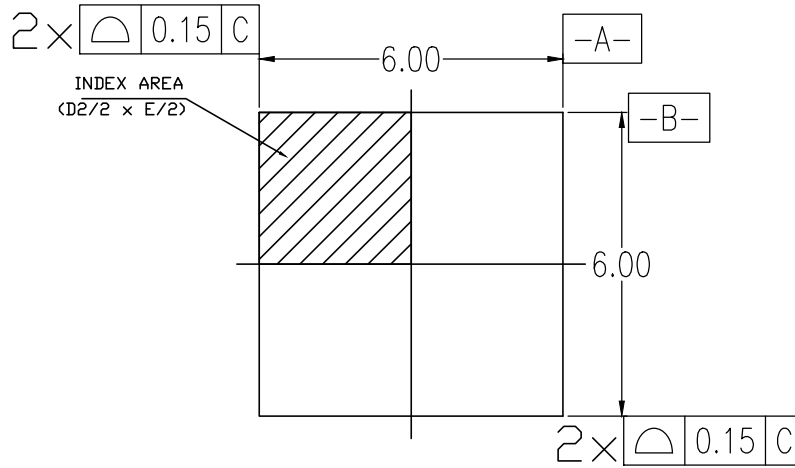
EVKIT LOSSES



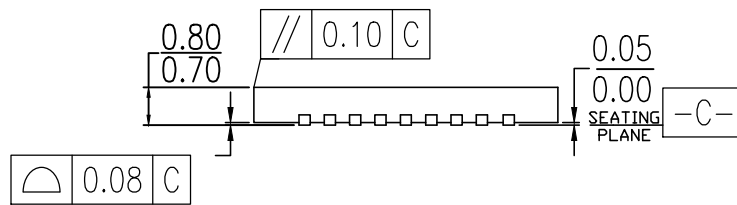
TOP MARKINGS



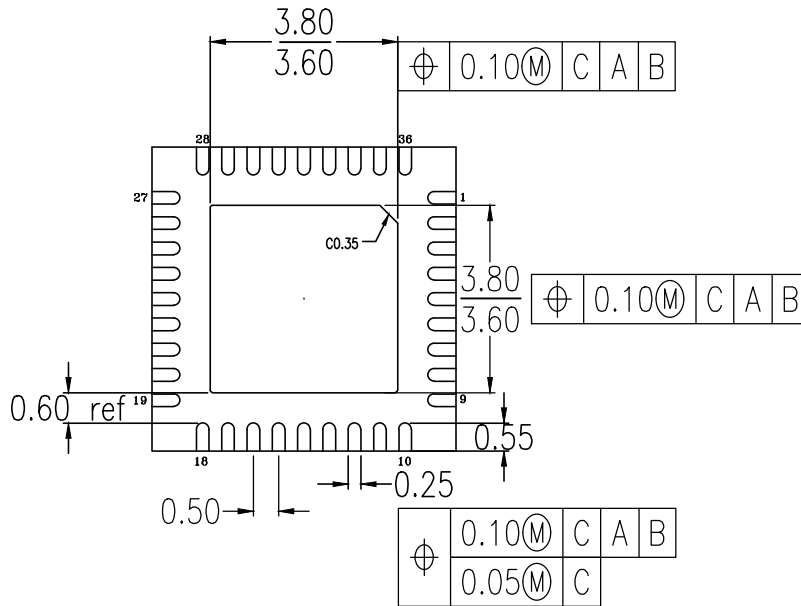
| Revision Date | Description |
|------------------|-----------------------|
| February 7, 2022 | Rebranded to Renesas. |
| May 5, 2014 | Initial release. |



TOP VIEW



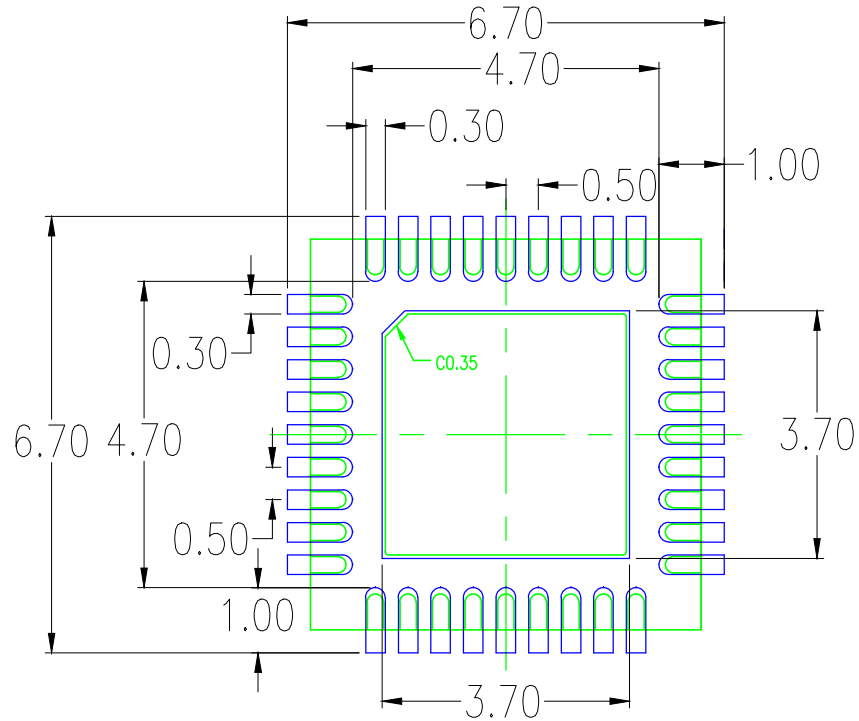
SIDE VIEW



BOTTOM VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| Package Revision History | | |
|--------------------------|---------|-------------------------------------|
| Date Created | Rev No. | Description |
| Nov 8, 2021 | 01 | Update IDT format to Renesas format |
| Apr 6, 2016 | 00 | Initial Release |

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