- **Outstanding Combination of dc Precision and AC Performance:**
  Unity-Gain Bandwidth . . . 15 MHz Typ
  V_n . . . . 3.3 nV/√Hz at f = 10 Hz Typ, 2.5 nV/√Hz at f = 1 kHz Typ
  V_{IO} . . . . 25 μV Max
  A_{VD} . . . 45 V/μV Typ With R_L = 2 kΩ, 19 V/μV Typ With R_L = 600 Ω
- **Available in Standard-Pinout Small-Outline Package**
- **Output Features Saturation Recovery Circuitry**
- **Macromodels and Statistical information**

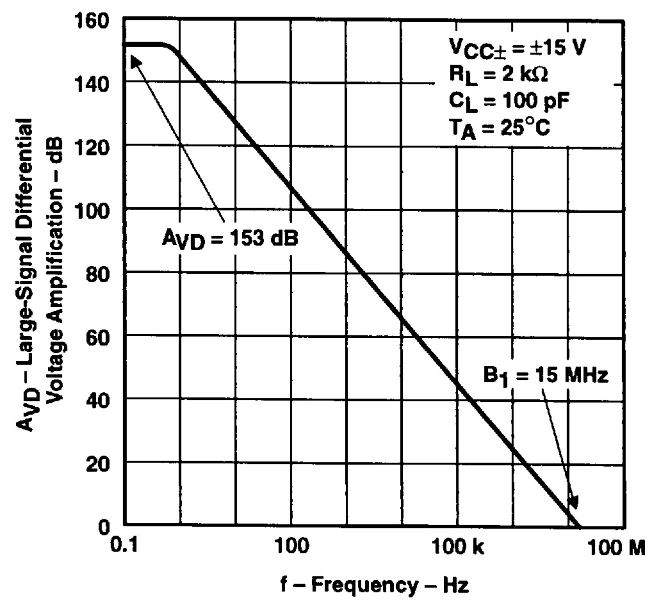
description

The TLE2027 and TLE2027A contain innovative circuit design expertise and high-quality process control techniques to produce a level of ac performance and dc precision previously unavailable in single operational amplifiers. Manufactured using Texas Instruments state-of-the-art Excalibur process, these devices allow upgrades to systems that use lower-precision devices.

In the area of dc precision, the TLE2027 and TLE2027A offer maximum offset voltages of 100 μV and 25 μV, respectively, common-mode rejection ratio of 131 dB (typ), supply voltage rejection ratio of 144 dB (typ), and dc gain of 45 V/μV (typ).

The ac performance is highlighted by a typical unity-gain bandwidth specification of 15 MHz, 55° of phase margin, and noise voltage specifications of 3.3 nV/√Hz and 2.5 nV/√Hz at frequencies of 10 Hz and 1 kHz respectively.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	25 μV 100 μV	TLE2027ACD TLE2027CD	— —	— —	TLE2027ACP TLE2027CP	— TLE2027Y
−40°C to 105°C	25 μV 100 μV	TLE2027AID TLE2027ID	— —	— —	TLE2027AIP TLE2027IP	— —
−55°C to 125°C	25 μV 100 μV	TLE2027AMD TLE2027MD	TLE2027AMFK TLE2027MFK	TLE2027AMJG TLE2027MJG	TLE2027AMP TLE2027MP	— —

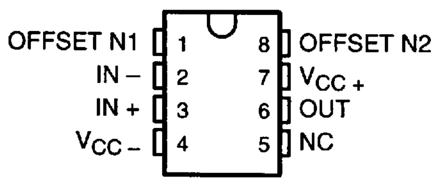
The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2027ACDR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

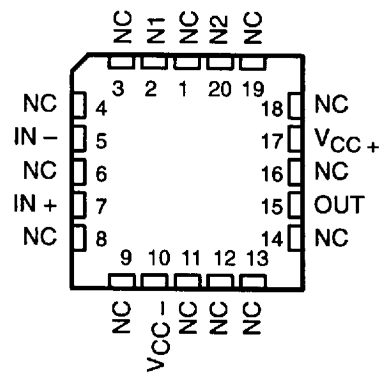
description (continued)

Both the TLE2027 and TLE2027A are available in a wide variety of packages, including the industry-standard 8-pin small-outline version for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 105°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

D, JG, OR P PACKAGE
(TOP VIEW)

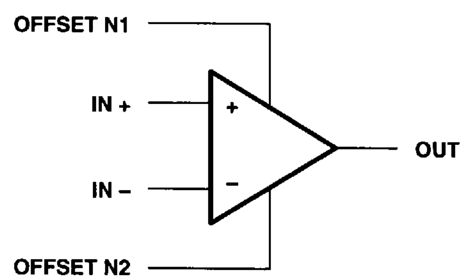


FK PACKAGE
(TOP VIEW)



NC – No internal connection

symbol

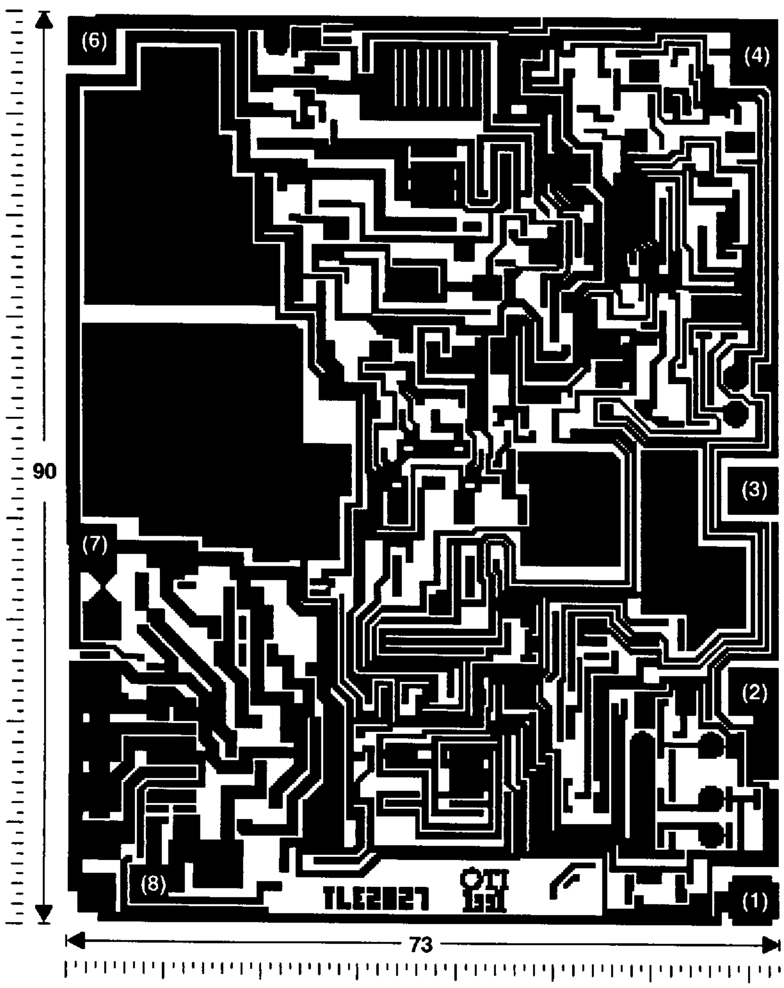


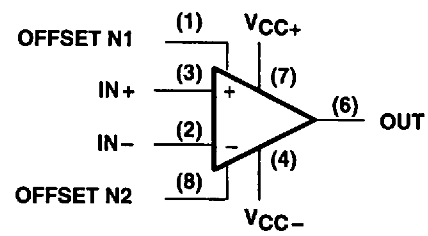
8961724 0103598 394

TLE2027Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2027C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

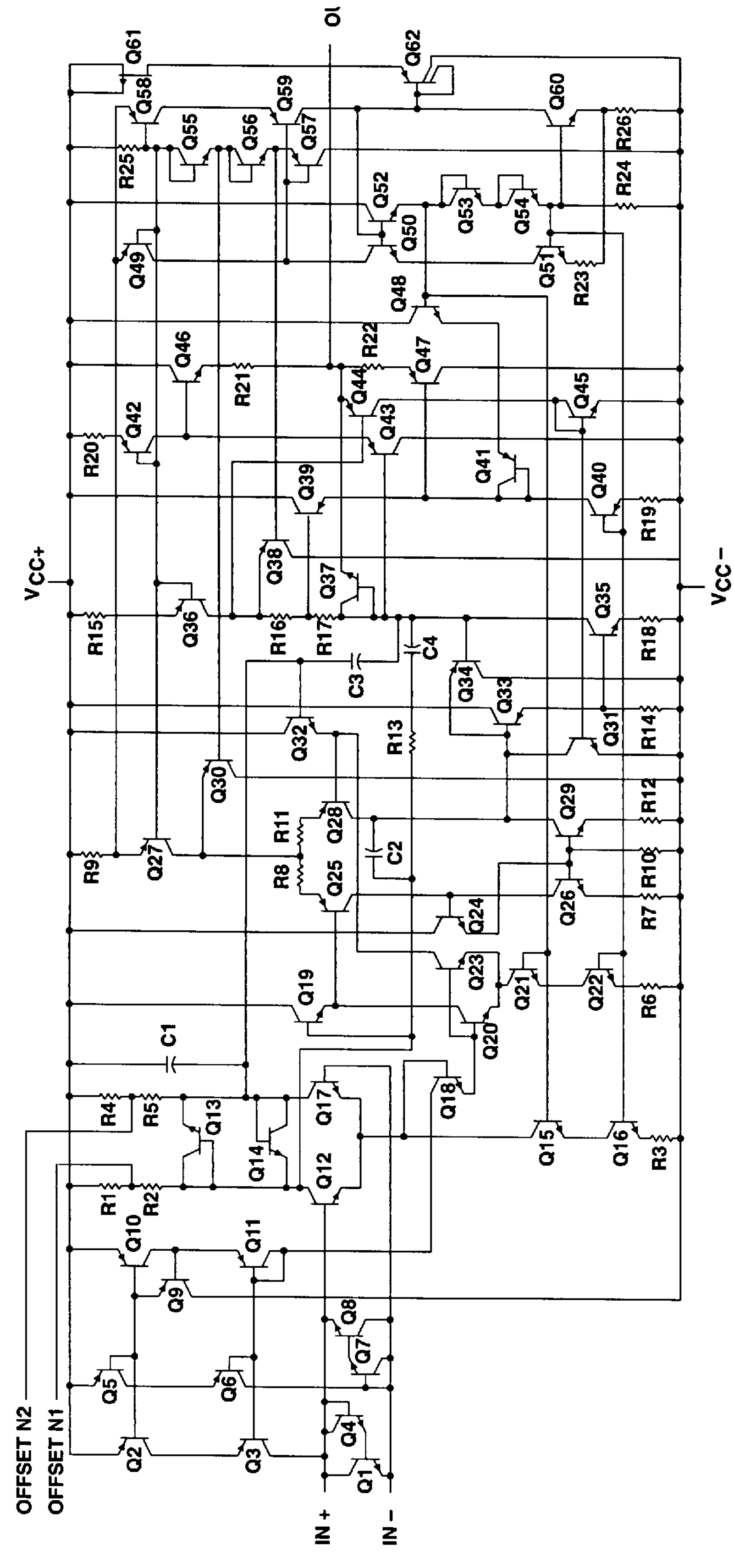
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic



COMPONENT COUNT	
Transistors	61
Resistors	26
Capacitors	4
epi FET	1

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) .... 19 V
Supply voltage, V_{CC-} .... – 19 V
Differential input voltage, V_{ID} (see Note 2) .... ±1.2 V
Input voltage range, V_I (any input) .... $V_{CC\pm}$
Input current, I_I (each Input) .... ±1 mA
Output current, I_O .... ± 50 mA
Total current into V_{CC+} .... 50 mA
Total current out of V_{CC-} .... 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .... unlimited
Continuous total power dissipation .... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix .... 0°C to 70°C
I suffix .... – 40°C to 105°C
M suffix .... – 55°C to 125°C
Storage temperature range, T_{stg} .... – 65°C to 150°C
Case temperature for 60 seconds, T_C: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package .... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–. Excessive current flows if a differential input voltage in excess of approximately ±1.2 V is applied between the inputs unless some limiting resistance is used.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	495 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	378 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	360 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±4	± 19	±4	±19	±4	±19	V
Common-mode input voltage, V_{IC}	$T_A = 25°C$	–11	11	–11	11	–11	11	V
	T_A = Full range‡	–10.5	10.5	–10.4	10.4	–10.2	10.2	
Operating free-air temperature, T_A		0	70	–40	105	–55	125	°C

‡ Full range is 0°C to 70°C for C-suffix devices, –40°C to 105°C for I-suffix devices, and –55°C to 125°C for M-suffix devices.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2027C MIN	TLE2027C TYP	TLE2027C MAX	TLE2027AC MIN	TLE2027AC TYP	TLE2027AC MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		20	100		10	25	µV
			Full range			145			70	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	µV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−11 to 11	−13 to 13		−11 to 11	−13 to 13		V
			Full range	−10.5 to 10.5			−10.5 to 10.5			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω	25°C	10.5			10.5			V
			Full range	10			10			
		R_L = 2 kΩ	25°C	12			12			
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω	25°C	−10.5	−13		−10.5	−13		V
			Full range	−10			−10			
		R_L = 2 kΩ	25°C	−12	−13.5		−12	−13.5		
			Full range	−11			−11			
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V, R_L = 2 kΩ	25°C	5	45		10	45		V/µV
		V_O = ±10 V, R_L = 2 kΩ	Full range	2			4			
		V_O = ±10 V, R_L = 1 kΩ	25°C	3.5	38		8	38		
			Full range	1			2.5			
		V_O = ±10 V, R_L = 600 Ω	25°C	2	19		5	19		
			Full range	0.5			2			
C_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	100	131		117	131		dB
			Full range	98			114			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	25°C	94	144		110	144		dB
		$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	Full range	92			106			
I_{CC}	Supply current	V_O = 0, No load	25°C		3.8	5.3		3.8	5.3	mA
			Full range			5.6			5.6	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS	T_A†	TLE2027C			TLE2027AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1	25°C	1.7	2.8		1.7	2.8		V/μs
			Full range	1.2			1.2			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 20$ Ω, f = 10 Hz	25°C		3.3	8		3.3	4.5	nV/√Hz
		$R_S = 20$ Ω, f = 1 kHz			2.5	4.5		2.5	3.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250		50	130	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6		0.4	0.6	
THD	Total harmonic distortion	$V_O = +10$ V, $A_{VD} = 5$, See Note 5	25°C		<0.002%			<0.002%		
B_1	Unity-gain bandwidth (see Figure 3)	$R_L = 2$ kΩ, $C_L = 100$ pF	25°C	7	13		9	13		MHz
B_{OM}	Maximum output-swing bandwidth	$R_L = 2$ kΩ	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 2$ kΩ, $C_L = 100$ pF	25°C		55°			55°		

† Full range is 0°C to 70°C.
NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2027I			TLE2027AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		20	100		10	25	µV
			Full range			180			105	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	µV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	−11 to 11	−13 to 13		−11 to 11	−13 to 13		V
			Full range	−10.4 to 10.4			−10.4 to 10.4			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 600\ \Omega$	25°C	10.5			10.5			V
			Full range	10			10			
		$R_L = 2\ k\Omega$	25°C	12			12			
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 600\ \Omega$	25°C	−10.5	−13		−10.5	−13		V
			Full range	−10			−10			
		$R_L = 2\ k\Omega$	25°C	− 12	−13.5		− 12	−13.5		
			Full range	− 11			− 11			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm11$ V, $R_L = 2\ k\Omega$	25°C	5	45		10	45		V/µV
		$V_O = \pm10$ V, $R_L = 2\ k\Omega$	Full range	2			3.5			
		$V_O = \pm10$ V, $R_L = 1\ k\Omega$	25°C	3.5	38		8	38		
			Full range	1			2.2			
		$V_O = \pm10$ V, $R_L = 600\ \Omega$	25°C	2	19		5	19		
			Full range	0.5			1.1			
C_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	$I_O = 0$	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	100	131		117	131		dB
			Full range	96			113			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm4$ V to ±18 V, $R_S = 50\ \Omega$	25°C	94	144		110	144		dB
		$V_{CC\pm} = \pm4$ V to ±18 V, $R_S = 50\ \Omega$	Full range	90			105			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		3.8	5.3		3.8	5.3	mA
			Full range			5.6			5.6	

† Full range is – 40°C to 105°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V

PARAMETER		TEST CONDITIONS	T_A†	TLE2027I			TLE2027AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figure 1	25°C	1.7	2.8		1.7	2.8		V/µs
			Full range	1.1			1.1			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 20\ \Omega$, f = 10 Hz	25°C		3.3	8		3.3	4.5	nV/√Hz
		$R_S = 20\ \Omega$, f = 1 kHz			2.5	4.5		2.5	3.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250		50	130	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6		0.4	0.6	
THD	Total harmonic distortion	$V_O = +10$ V, $A_{VD} = 1$, See Note 5	25°C		< 0.002%			< 0.002%		
B_1	Unity-gain bandwidth (see Figure 3)	$R_L = 2\ k\Omega$, $C_L = 100$ pF	25°C	7	13		9	13		MHz
B_{OM}	Maximum output-swing bandwidth	$R_L = 2\ k\Omega$	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 2\ k\Omega$, $C_L = 100$ pF	25°C		55°			55°		

† Full range is – 40°C to 105°C.
NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2027M MIN	TLE2027M TYP	TLE2027M MAX	TLE2027AM MIN	TLE2027AM TYP	TLE2027AM MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		20	100		10	25	µV
			Full range			200			105	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1*		0.2	1*	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1*		0.006	1*	µV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	−11 to 11	−13 to 13		−11 to 11	−13 to 13		V
			Full range	−10.3 to 10.3			−10.4 to 10.4			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 600\ \Omega$	25°C	10.5			10.5			V
			Full range	10			10			
		$R_L = 2\ k\Omega$	25°C	12			12			
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 600\ \Omega$	25°C	−10.5	−13		−10.5	−13		V
			Full range	−10			−10			
		$R_L = 2\ k\Omega$	25°C	−12	−13.5		−12	−13.5		
			Full range	−11			−11			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm11$ V, $R_L = 2\ k\Omega$	25°C	5	45		10	45		V/µV
		$V_O = \pm10$ V, $R_L = 2\ k\Omega$	Full range	2.5			3.5			
		$V_O = \pm10$ V, $R_L = 1\ k\Omega$	25°C	3.5	38		8	38		
			Full range	1.8			2.2			
		$V_O = \pm10$ V, $R_L = 600\ \Omega$	25°C	2	19		5	19		
C_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	$I_O = 0$	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	100	131		117	131		dB
			Full range	96			113			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm4$ V to ±18 V, $R_S = 50\ \Omega$	25°C	94	144		110	144		dB
		$V_{CC\pm} = \pm4$ V to ±18 V, $R_S = 50\ \Omega$	Full range	90			105			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		3.8	5.3		3.8	5.3	mA
			Full range			5.6			5.6	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† Full range is – 55°C to 125°C.
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V

PARAMETER		TEST CONDITIONS	T_A†	TLE2027M			TLE2027AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1	25°C	1.7	2.8		1.7	2.8		V/μs
			Full range	1			1			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω, f = 10 Hz	25°C		3.3	8*		3.3	4.5*	nV/√Hz
		R_S = 20 Ω, f = 1 kHz			2.5	4.5*		2.5	3.8*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250*		50	130*	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4*		1.5	4*	pA/√Hz
		f = 1 kHz			0.4	0.6*		0.4	0.6*	
THD	Total harmonic distortion	V_O = +10 V, A_{VD} = 1, See Note 5	25°C		< 0.002%			< 0.002%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	25°C	7*	13		9*	13		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	25°C		55°			55°		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† Full range is – 55°C to 125°C.
NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TLE2027Y MIN	TLE2027Y TYP	TLE2027Y MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$		20	100	µV
	Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0$, $R_S = 50\ \Omega$		0.006		µV/mo
I_{IO}	Input offset current	$V_{IC} = 0$, $R_S = 50\ \Omega$		6		nA
I_{IB}	Input bias current	$V_{IC} = 0$, $R_S = 50\ \Omega$		15		nA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		–13 to 13		V
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 600\ \Omega$		–13		V
		$R_L = 2\ k\Omega$		–13.5		V
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 11$ V, $R_L = 2\ k\Omega$		45		V/µV
		$V_O = \pm 10$ V, $R_L = 1\ k\Omega$		38		V/µV
		$V_O = \pm 10$ V, $R_L = 600\ \Omega$		19		V/µV
C_i	Input capacitance			8		pF
z_o	Open-loop output impedance	$I_O = 0$		50		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $R_S = 50\ \Omega$		131		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 4$ V to ± 18 V, $R_S = 50\ \Omega$		144		dB
I_{CC}	Supply current	$V_O = 0$, No load		3.8		mA

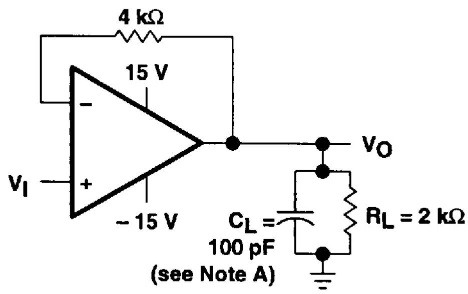
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS	TLE2027Y			UNIT
			MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figure 1		2.8		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 20\ \Omega$, f = 10 Hz		3.3		nV/√Hz
		$R_S = 20\ \Omega$, f = 1 kHz		2.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		50		nV
I_n	Equivalent input noise current	f = 10 Hz		1.5		pA/√Hz
		f = 1 kHz		0.4		
THD	Total harmonic distortion	$V_O = +10$ V, $A_{VD} = 5$, See Note 5		<0.002%		
B_1	Unity-gain bandwidth (see Figure 3)	$R_L = 2\ k\Omega$, $C_L = 100$ pF		13		MHz
B_{OM}	Maximum output-swing bandwidth	$R_L = 2\ k\Omega$		30		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 2\ k\Omega$, $C_L = 100$ pF		55°		

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

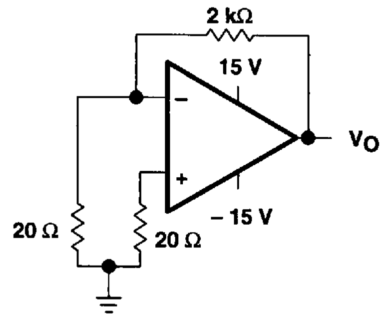
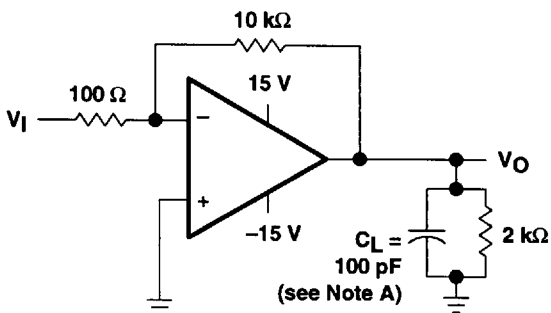
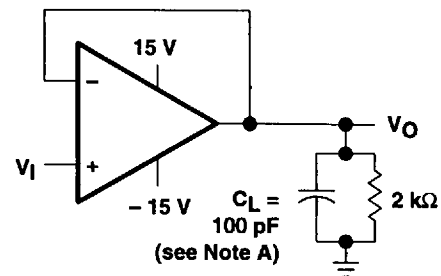


Figure 2. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 4. Small-Signal Pulse-Response Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

initial estimates of parameter distributions

In the ongoing program of improving data sheets and supplying more information to our customers, Texas Instruments has added an estimate of not only the typical values but also the spread around these values. These are in the form of distribution bars that show the 95% (upper) points and the 5% (lower) points from the characterization of the initial wafer lots of this new device type (see Figure 5). The distribution bars are shown at the points where data was actually collected. The 95% and 5% points are used instead of ± 3 sigma since some of the distributions are not true Gaussian distributions.

The number of units tested and the number of different wafer lots used are on all of the graphs where distribution bars are shown. As noted in Figure 5, there were a total of 835 units from two wafer lots. In this case, there is a good estimate for the within-lot variability and a possibly poor estimate of the lot-to-lot variability. This is always the case on newly released products since there can only be data available from a few wafer lots.

The distribution bars are not intended to replace the minimum and maximum limits in the electrical tables. Each distribution bar represents 90% of the total units tested at a specific temperature. While 10% of the units tested fell outside any given distribution bar, this should not be interpreted to mean that the same individual devices fell outside every distribution bar.

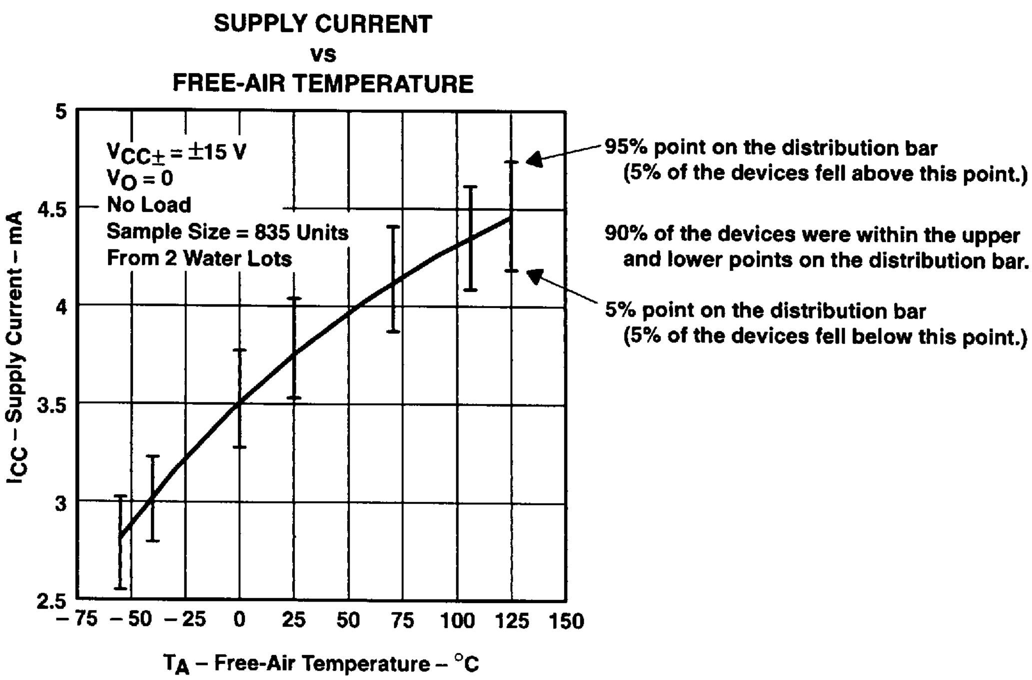


Figure 5. Sample Graph With Distribution Bars

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
ΔV_{IO}	Input offset voltage change	vs Time after power on	7, 8
I_{IO}	Input offset current	vs Free-air temperature	9
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	10 11
I_I	Input current	vs Differential input voltage	12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13
V_{OM}	Maximum (positive/negative) peak output voltage	vs Load resistance vs Free-air temperature	14, 15 16, 17
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Load resistance vs Frequency vs Free-air temperature	18 19 20, 21 22
z_o	Output impedance	vs Frequency	23
CMRR	Common-mode rejection ratio	vs Frequency	24
k_{SVR}	Supply voltage rejection ratio	vs Frequency	25
I_{OS}	Short-circut output current	vs Supply voltage vs Elapsed time vs Free-air temperature	26, 27 28, 29 30, 31
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	32 33
	Pulse response	Small signal Large signal	34 35
V_n	Equivalent input noise voltage	vs Frequency	36
	Noise voltage (referred to input)	vs Time	37
B_1	Unity-gain bandwidth	vs Supply voltage vs Load capacitance	38 39
SR	Slew rate	vs Free-air temperature	40
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	41 42 43
	Phase shift	vs Frequency	20, 21

TYPICAL CHARACTERISTICS

TLE2027 DISTRIBUTION INPUT OFFSET VOLTAGE

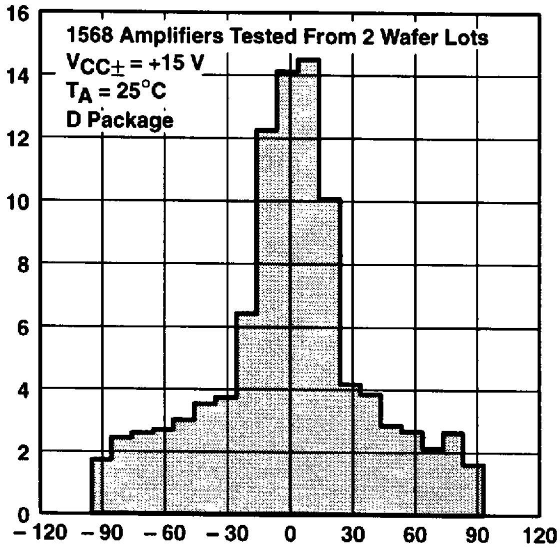


Figure 6

INPUT OFFSET VOLTAGE CHANGE vs TIME AFTER POWER ON

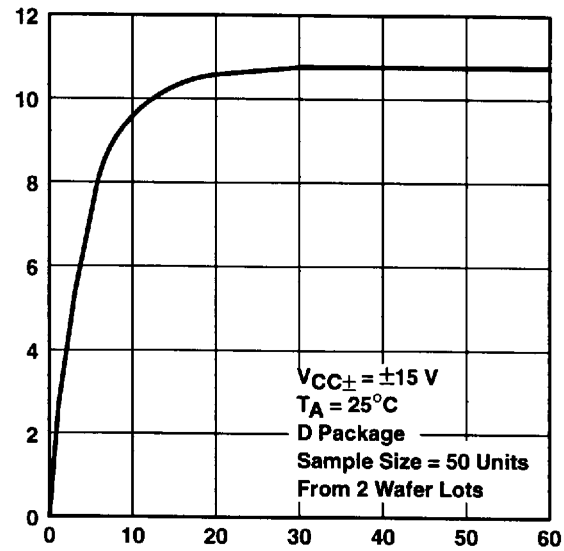


Figure 7

INPUT OFFSET VOLTAGE CHANGE vs TIME AFTER POWER ON

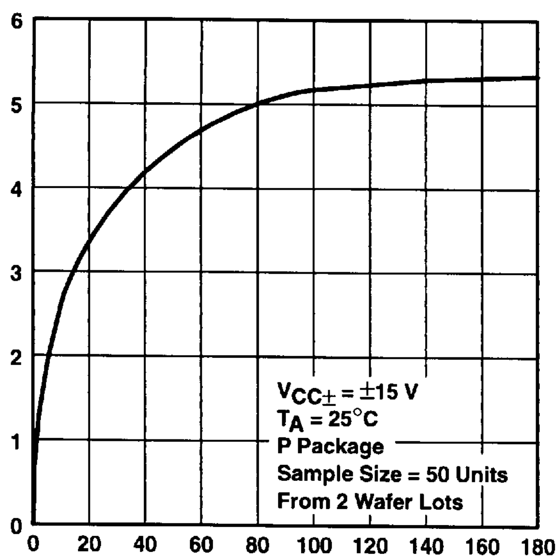
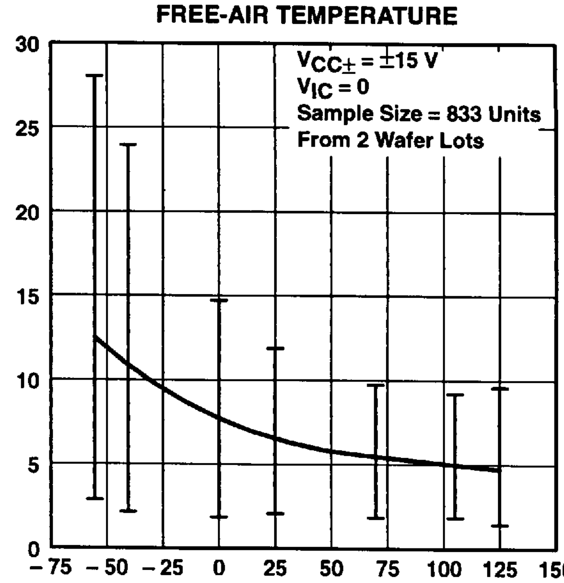


Figure 8

INPUT OFFSET CURRENT† vs FREE-AIR TEMPERATURE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 9

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

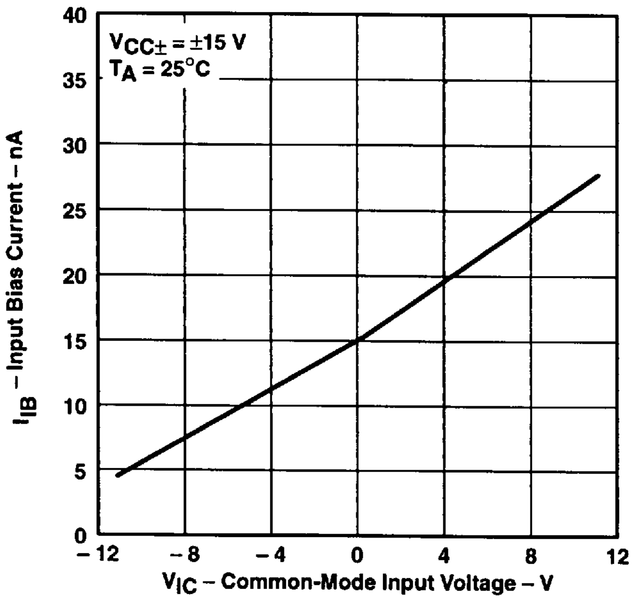
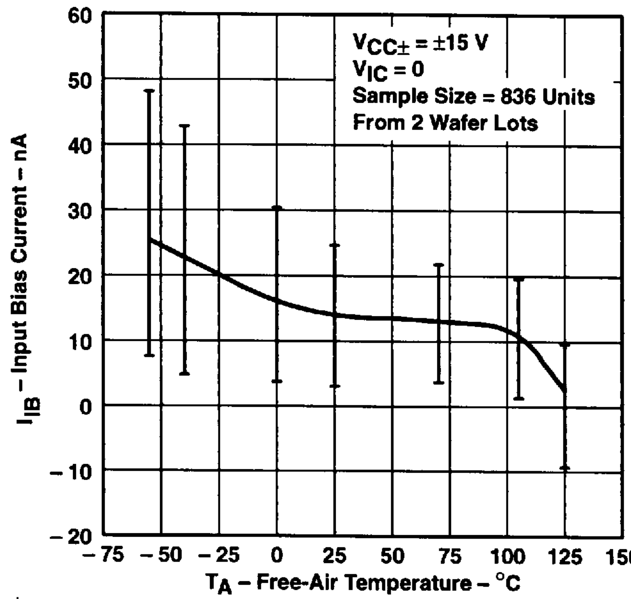


Figure 10

INPUT BIAS CURRENT† vs FREE-AIR TEMPERATURE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 11

TYPICAL CHARACTERISTICS

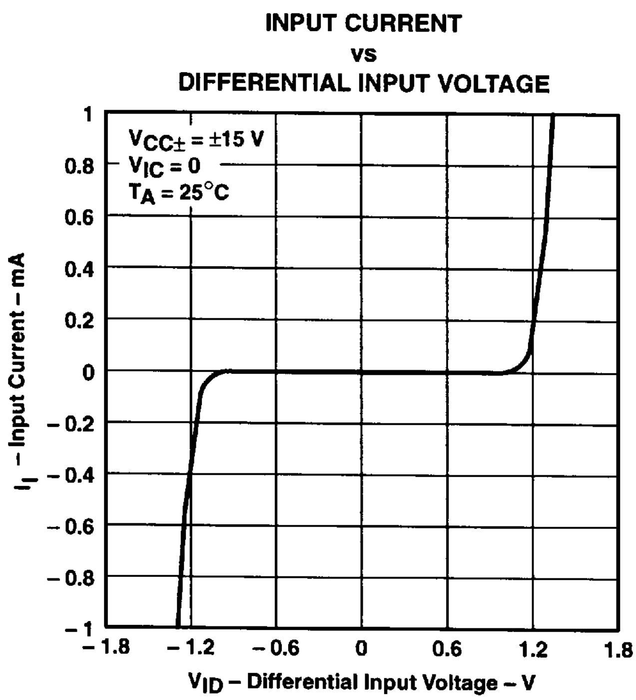
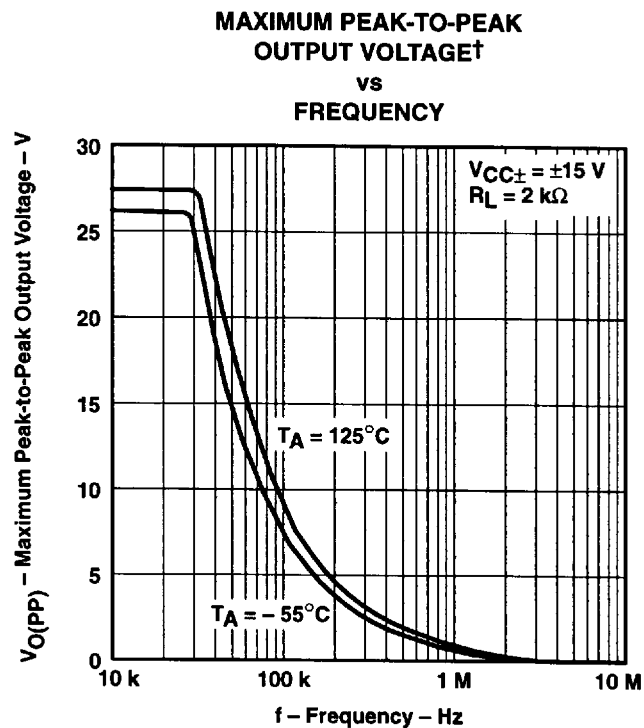


Figure 12



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 13

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

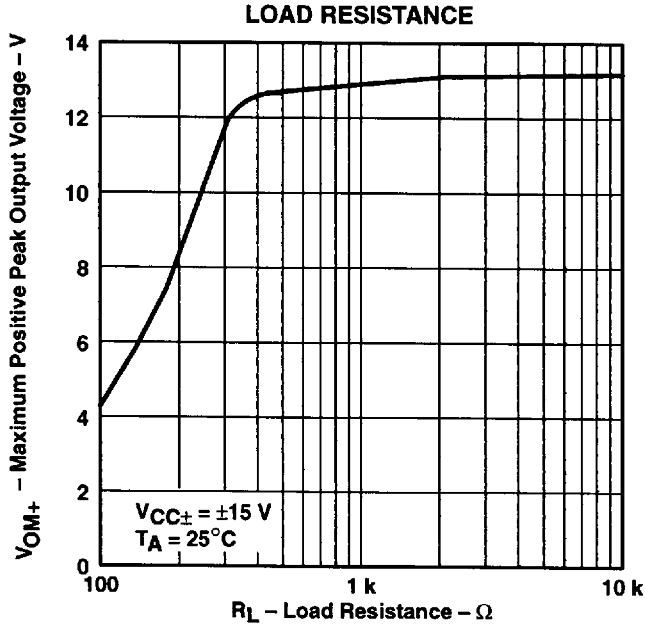


Figure 14

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

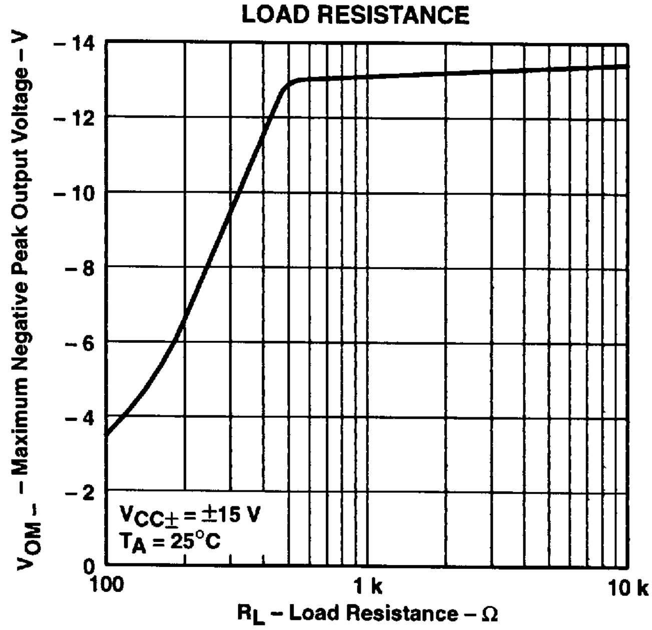
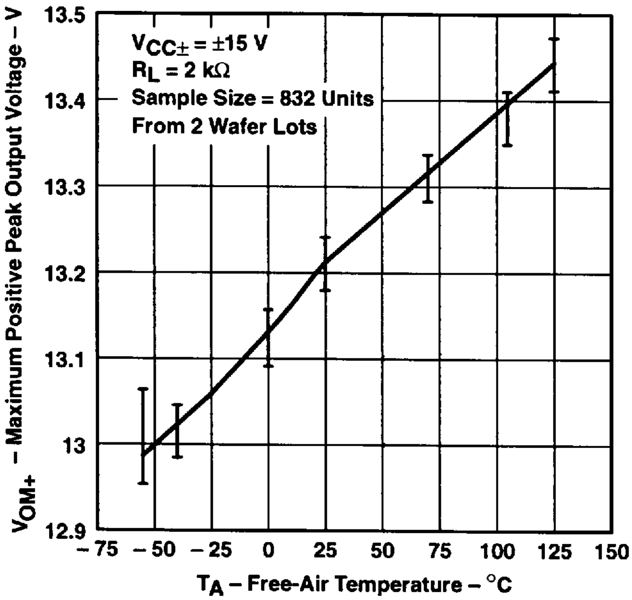


Figure 15

TYPICAL CHARACTERISTICS

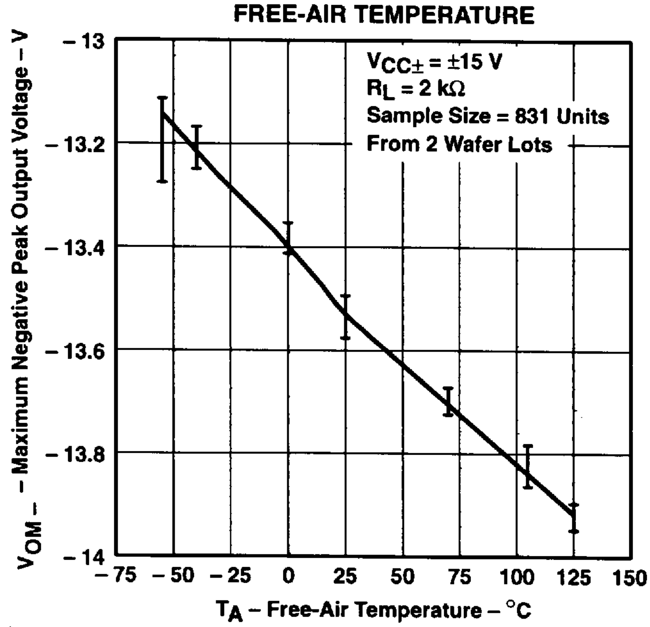
MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE† vs FREE-AIR TEMPERATURE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 16

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE† vs FREE-AIR TEMPERATURE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 17

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

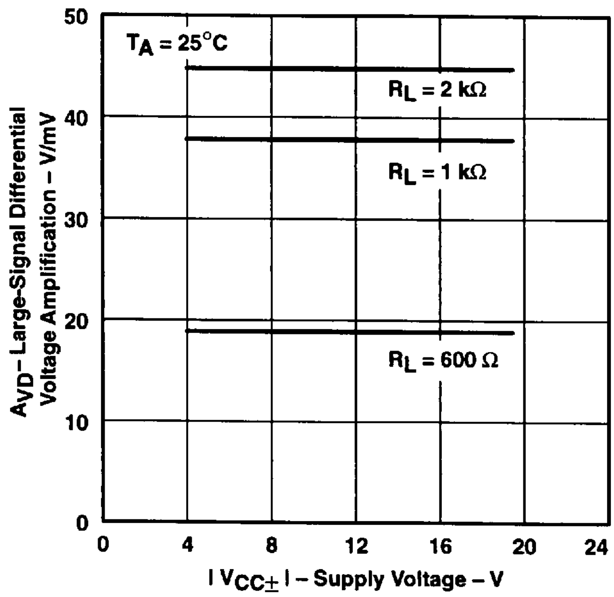


Figure 18

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION
vs
LOAD RESISTANCE

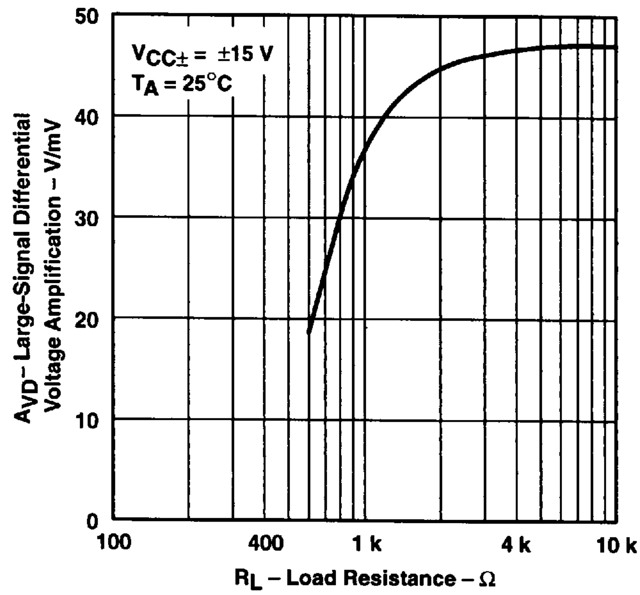


Figure 19

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

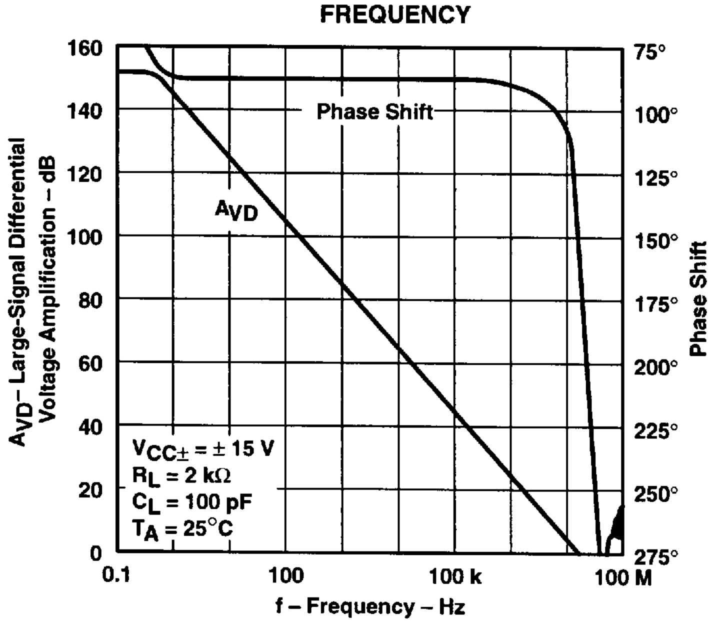


Figure 20

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

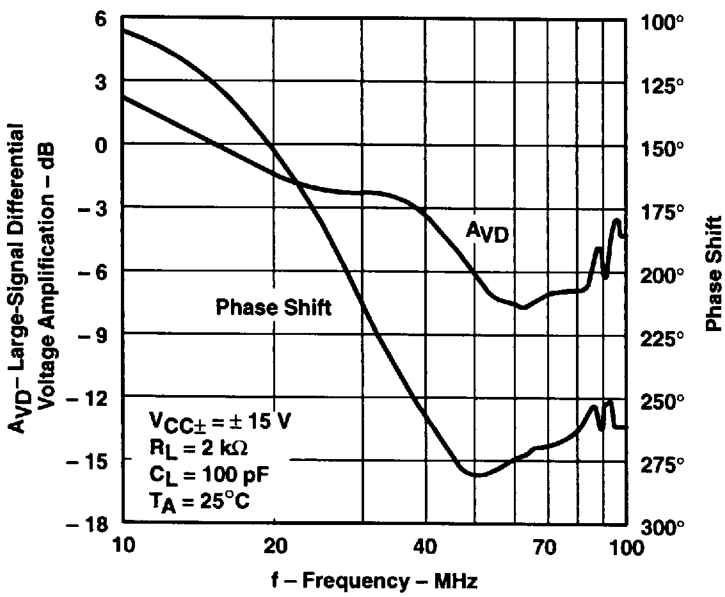
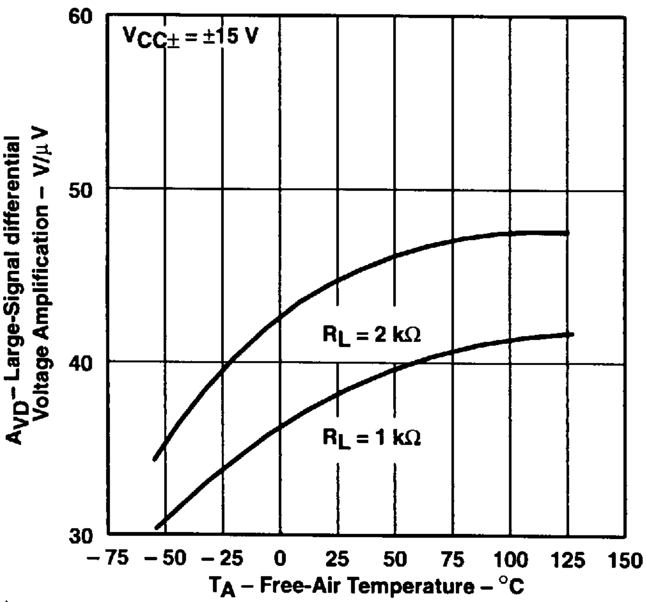


Figure 21

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†
vs
FREE-AIR TEMPERATURE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 22

OUTPUT IMPEDANCE
vs
FREQUENCY

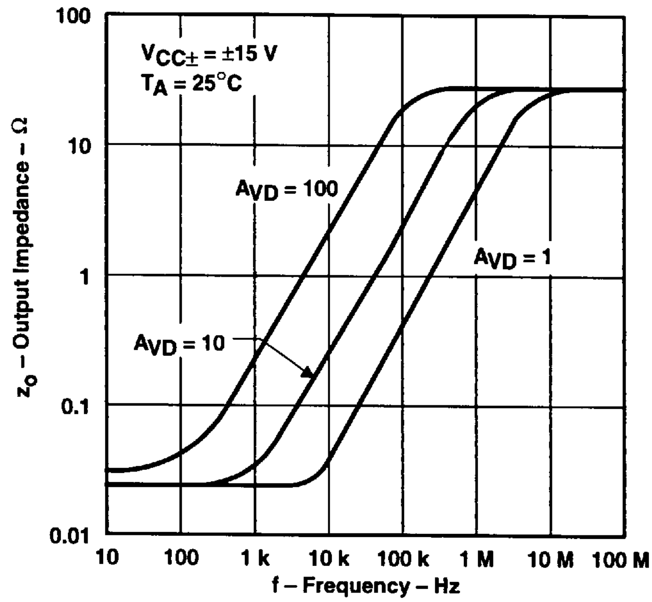


Figure 23

8961724 0103620 660

TYPICAL CHARACTERISTICS

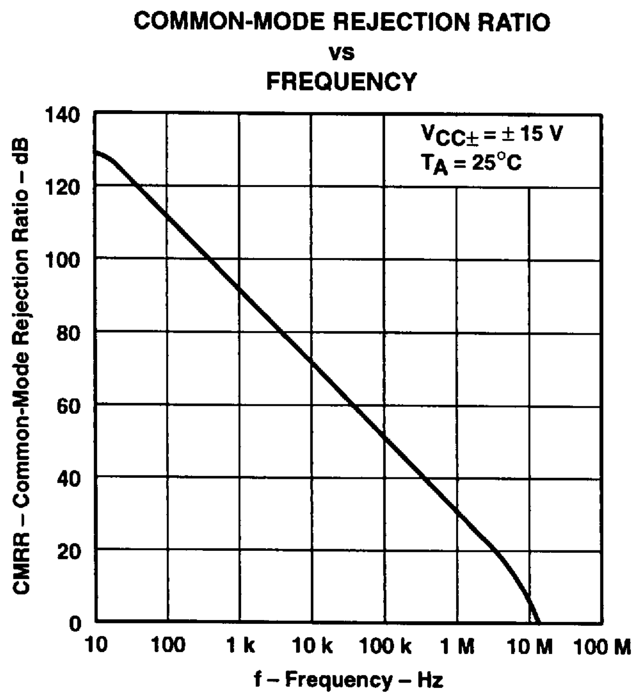


Figure 24

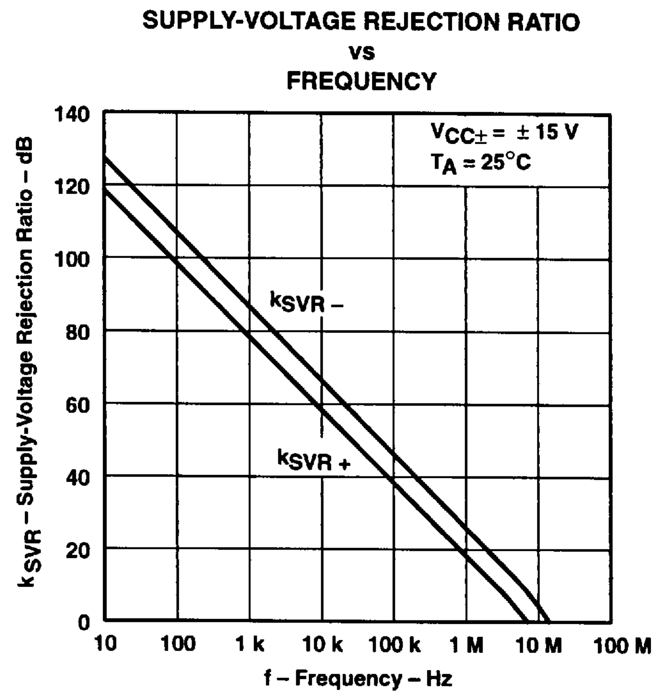


Figure 25

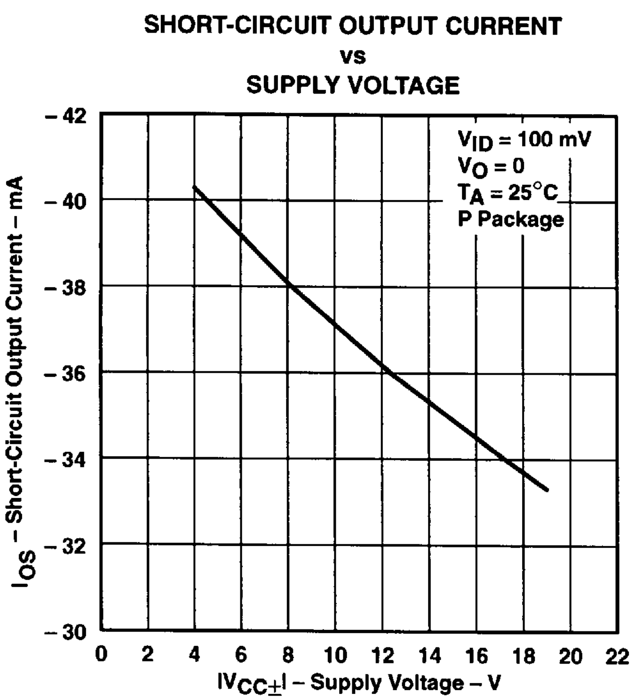


Figure 26

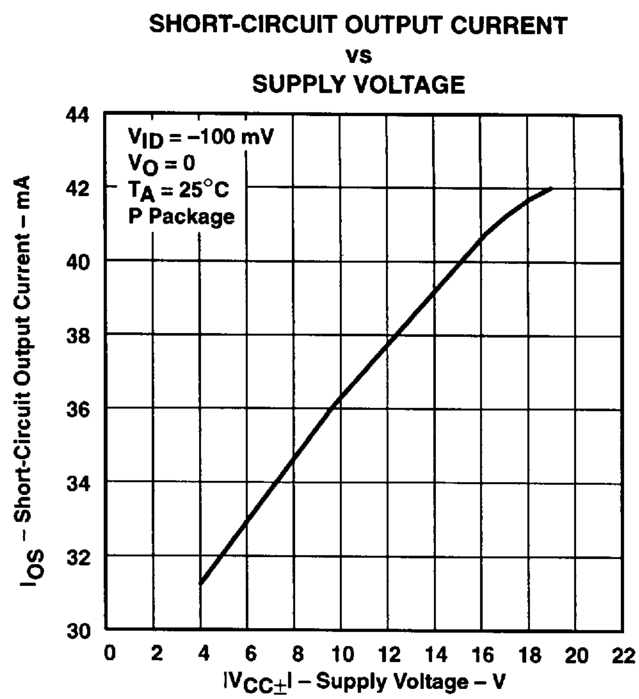


Figure 27

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

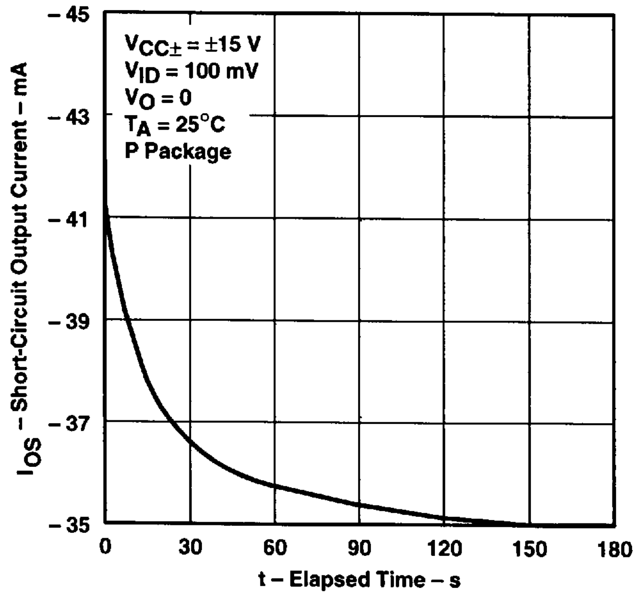


Figure 28

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

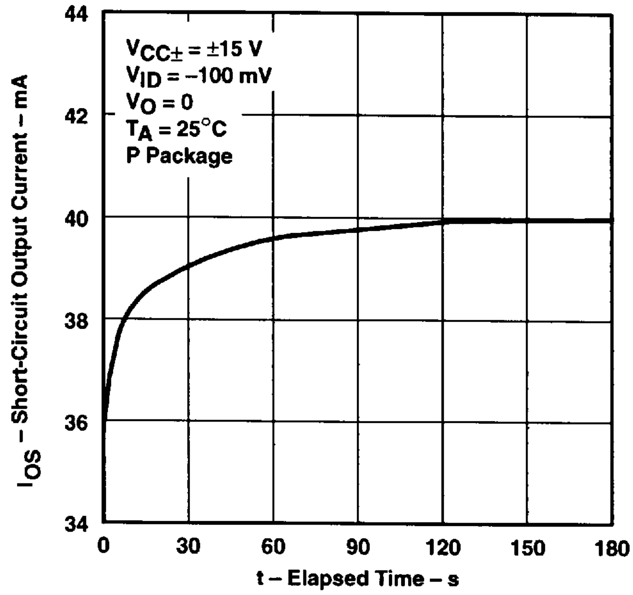
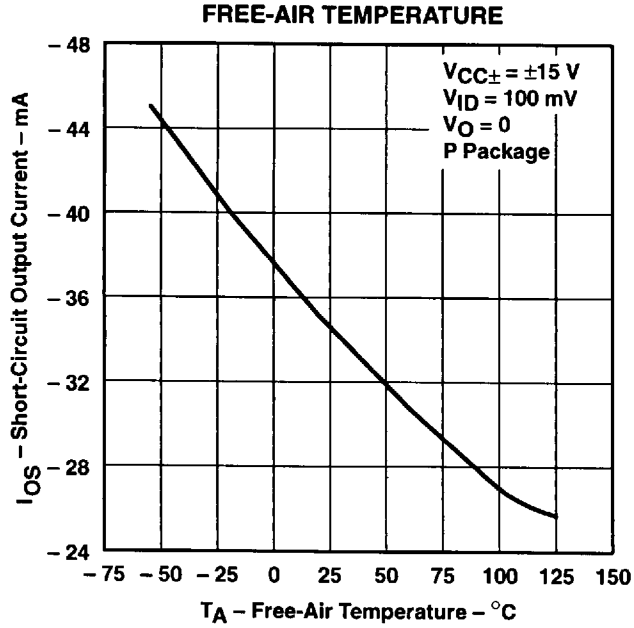


Figure 29

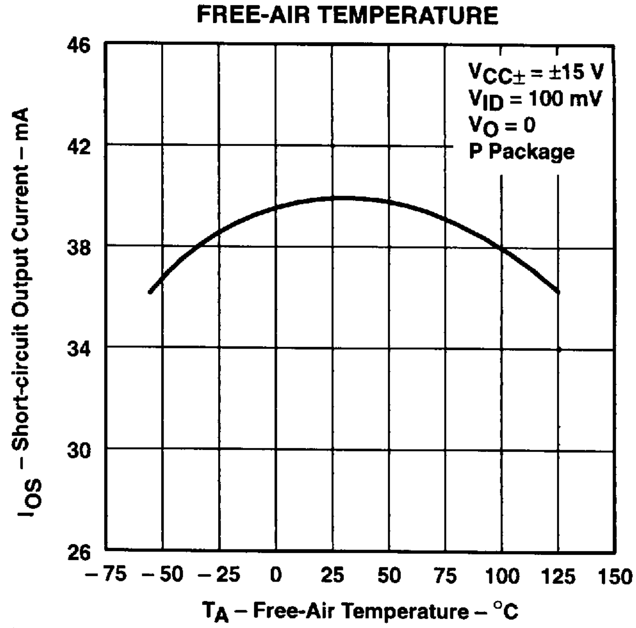
SHORT-CIRCUIT OUTPUT CURRENT† vs FREE-AIR TEMPERATURE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 30

SHORT-CIRCUIT OUTPUT CURRENT† vs FREE-AIR TEMPERATURE

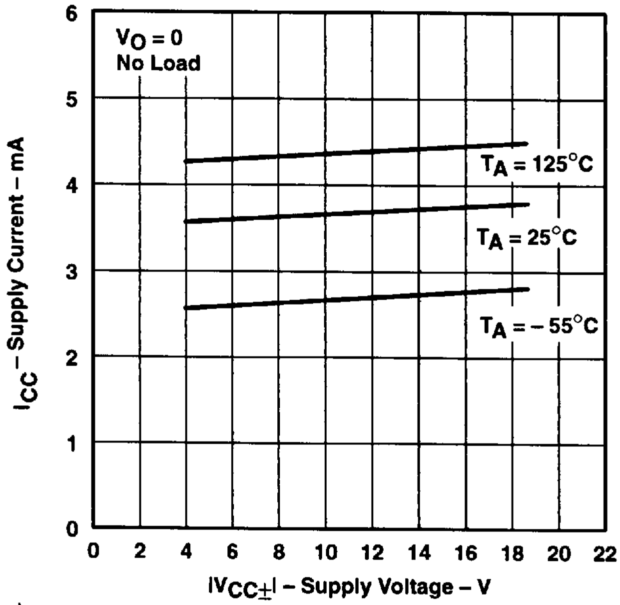


† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 31

TYPICAL CHARACTERISTICS

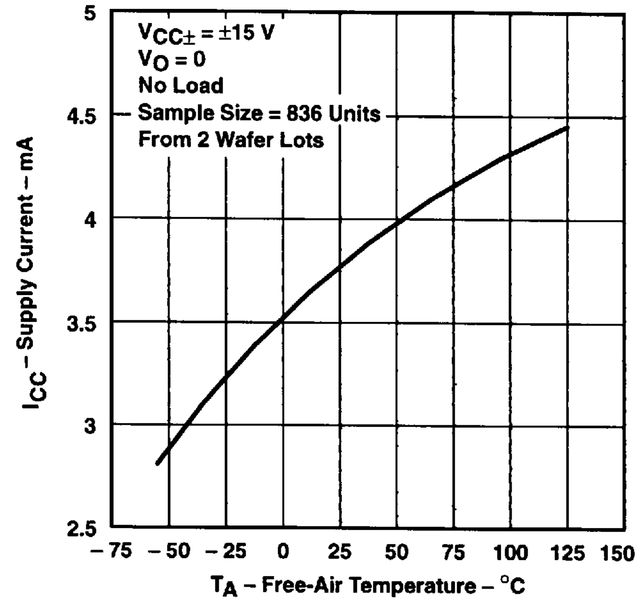
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 32

SUPPLY CURRENT†
vs
FREE-AIR TEMPERATURE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 33

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

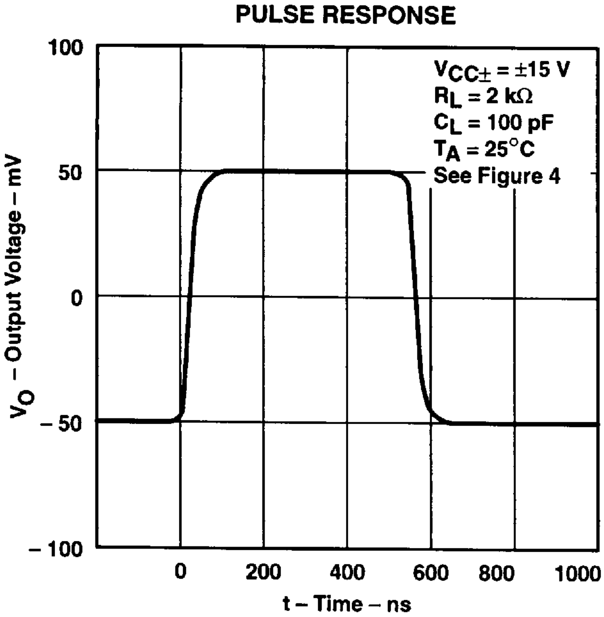


Figure 34

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

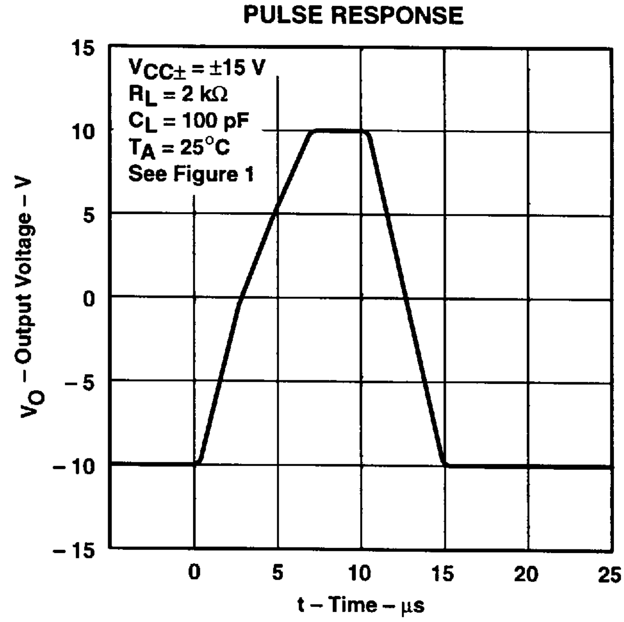


Figure 35

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

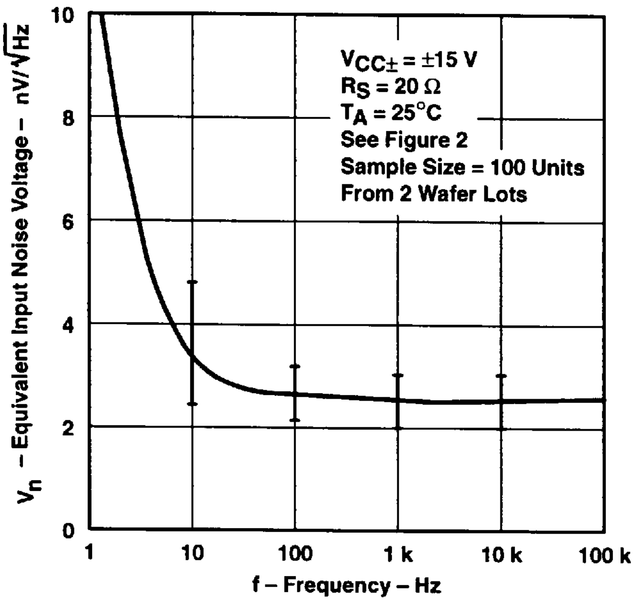


Figure 36

NOISE VOLTAGE
(REFERRED TO INPUT)
OVER A 10-SECOND INTERVAL

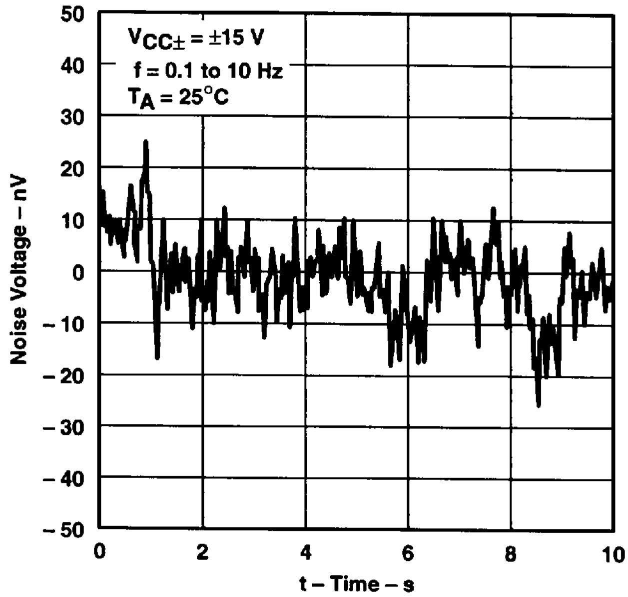


Figure 37

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

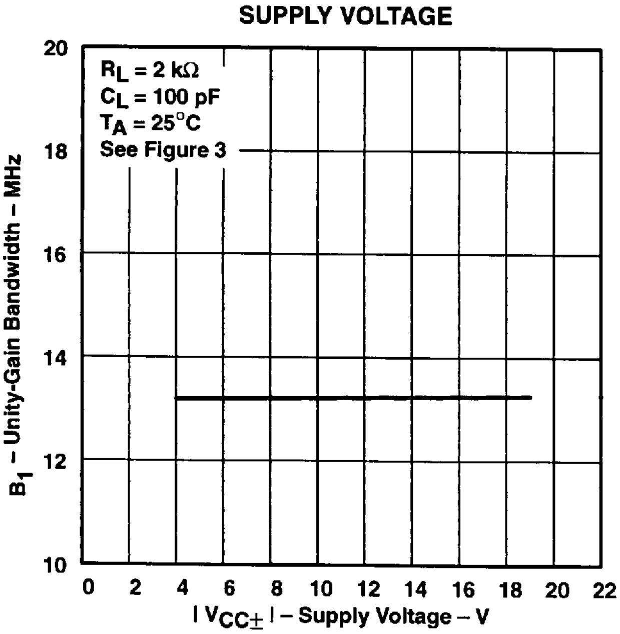


Figure 38

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

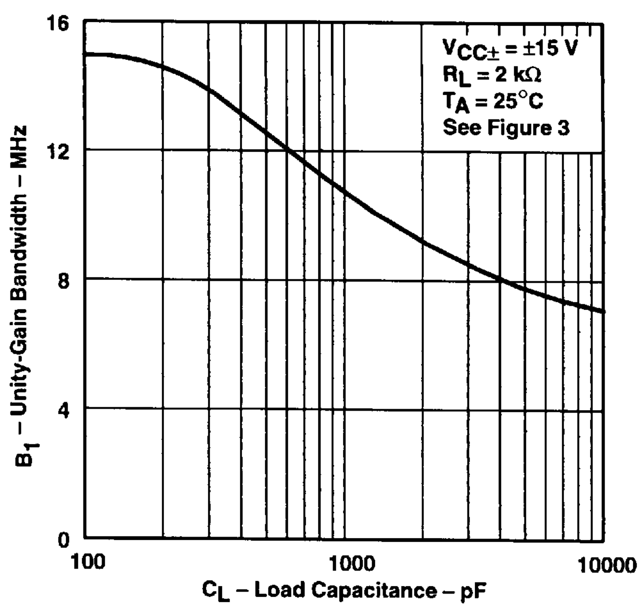
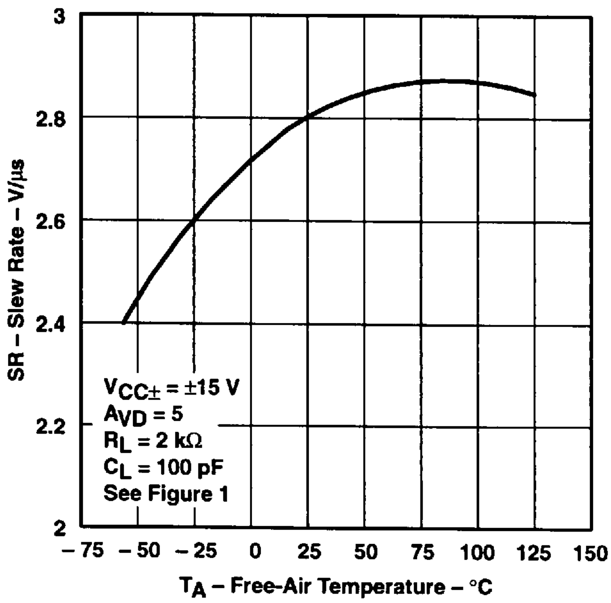


Figure 39

TYPICAL CHARACTERISTICS

SLEW RATE†
vs
FREE-AIR TEMPERATURE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 40

PHASE MARGIN
vs
SUPPLY VOLTAGE

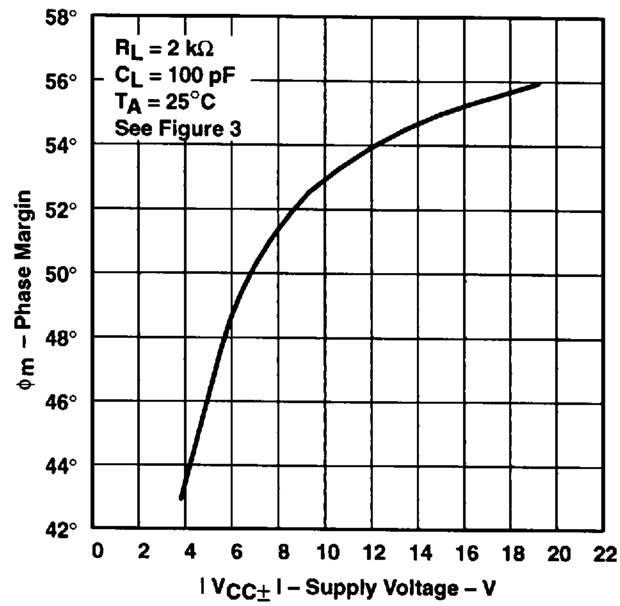


Figure 41

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
LOAD CAPACITANCE

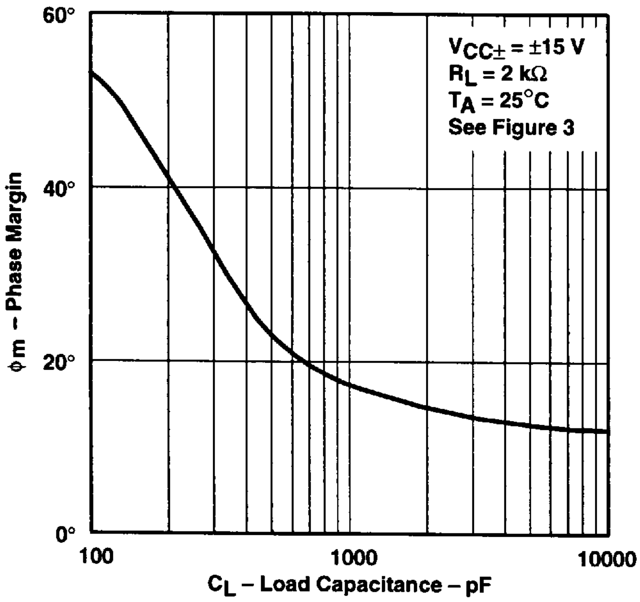
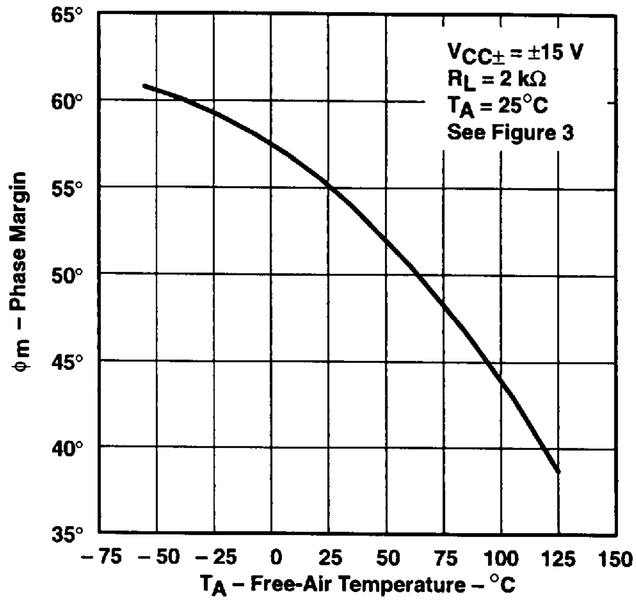


Figure 42

PHASE MARGIN†
vs
FREE-AIR TEMPERATURE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 43

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 6) and subcircuit in Figures 44 and 45 were generated using the TLE2027 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Gain-bandwidth product
- Common-mode rejection ratio
- Phase margin
- dc output resistance
- ac output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

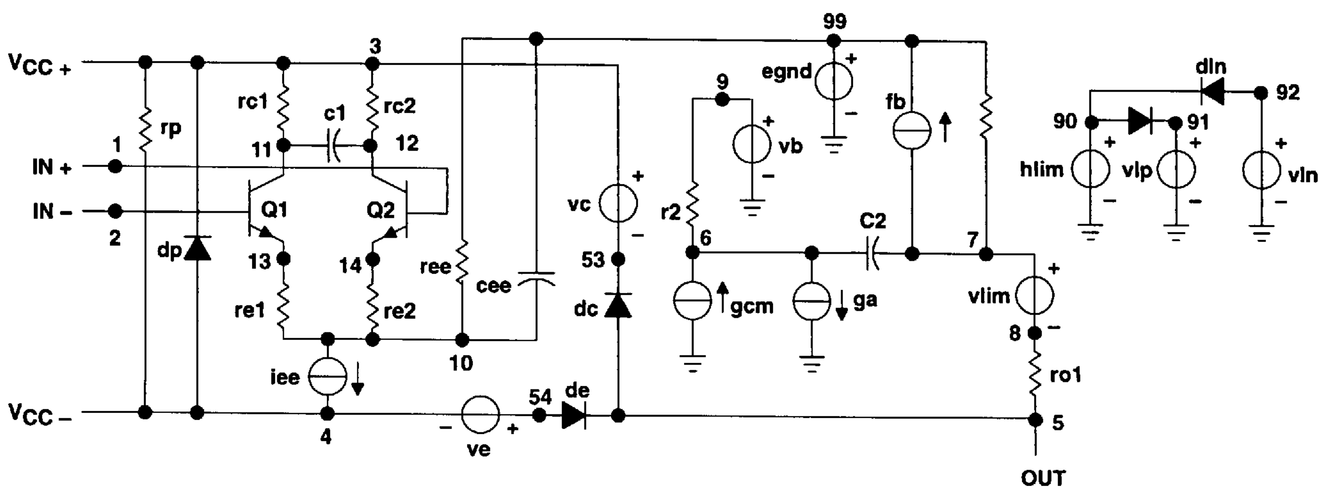


Figure 44. Boyle Macromodel

PSpice and *Parts* are trademarks of MicroSim Corporation.

APPLICATION INFORMATION

macromodel information (continued)

```
.subckt TLE2027 1 2 3 4 5
*
  c1      11   12   4.003E-12
  c2       6    7   20.00E-12
  dc       5   53   dz
  de      54    5   dz
  dlp     90   91   dz
  dln     92   90   dx
  dp       4    3   dz
  egnd    99    0   poly(2) (3,0) (4,0) 0 5 .5
  fb       7   99   poly(5) vb vc ve vlp vln 0 954.8E6 -1E9 1E9 1E9 -1E9
  ga       6    0   11  12   2.062E-3
  gcm      0    6   10  99   531.3E-12
  iee     10    4   dc  56.01E-6
  hlim    90    0   vlim 1K
  q1      11    2   13 qx
  q2      12    1   14 qx
  r2       6    9   100.0E3
  rc1      3   11   530.5
  rc2      3   12   530.5
  re1     13   10   -393.2
  re2     14   10   -393.2
  ree     10   99   3.571E6
  ro1      8    5   25
  ro2      7   99   25
  rp       3    4   8.013E3
  vb       9    0   dc  0
  vc       3   53   dc  2.400
  ve      54    4   dc  2.100
  vlim     7    8   dc  0
  vlp     91    0   dc  40
  vln      0   92   dc  40
.modeldx D(Is=800.0E-18)
.modelqx NPN(Is=800.0E-18 Bf=7.000E3)
.ends
```

Figure 45. Macromodel Subcircuit

APPLICATION INFORMATION

voltage-follower applications

The TLE2027 circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. It is recommended that a feedback resistor be used to limit the current to a maximum of 1 mA to prevent degradation of the device. Also, this feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10 kΩ, this pole degrades the amplifier phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 46).

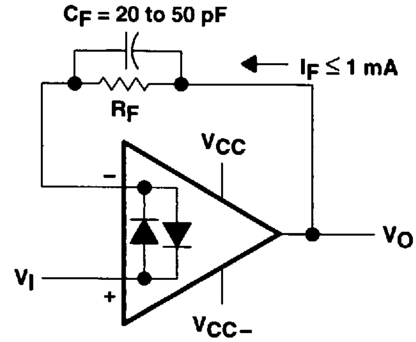


Figure 46. Voltage Follower

Input offset voltage nulling

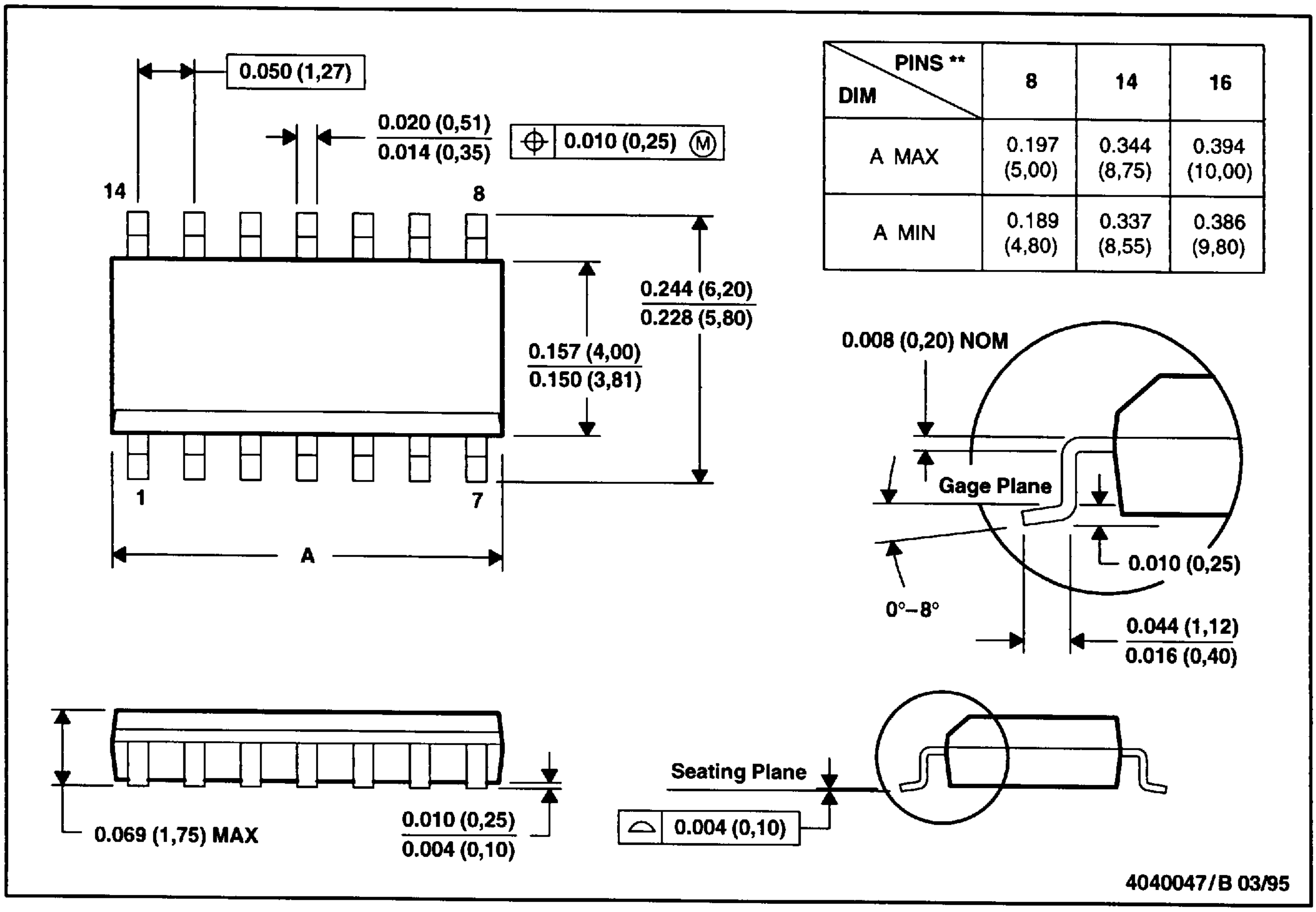
The TLE2027 series offers external null terminals that can further reduce the input offset voltage. The circuits of Figure 47 can be connected as shown if the feature is desired. If external nulling is not needed, the null terminals may be left disconnected.

Figure 47. Input Offset-Voltage Nulling Circuits

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



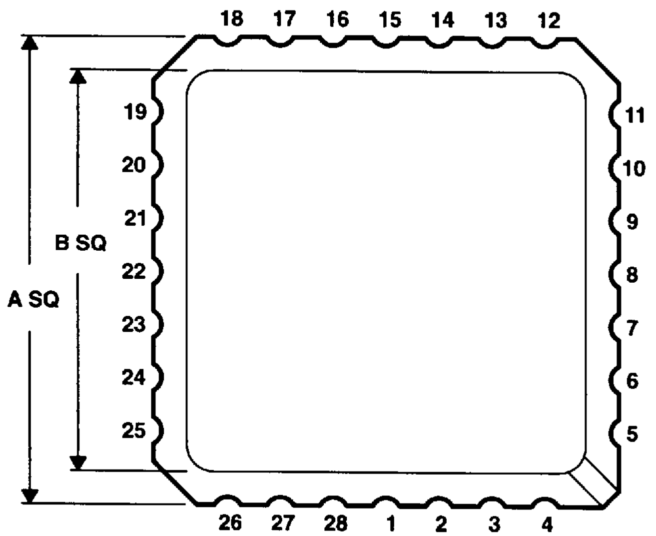
PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

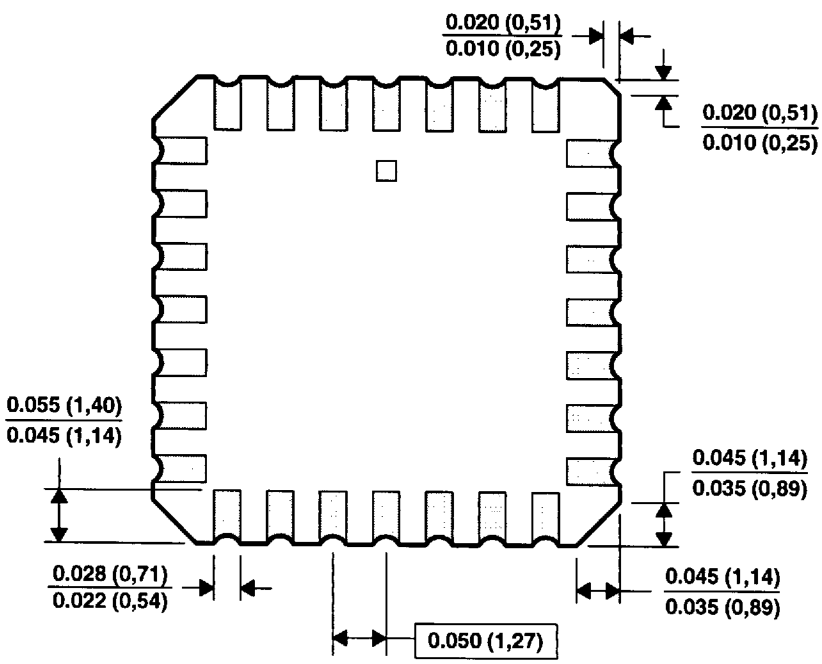
MECHANICAL INFORMATION

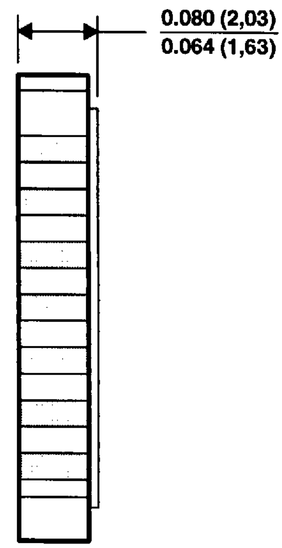
FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



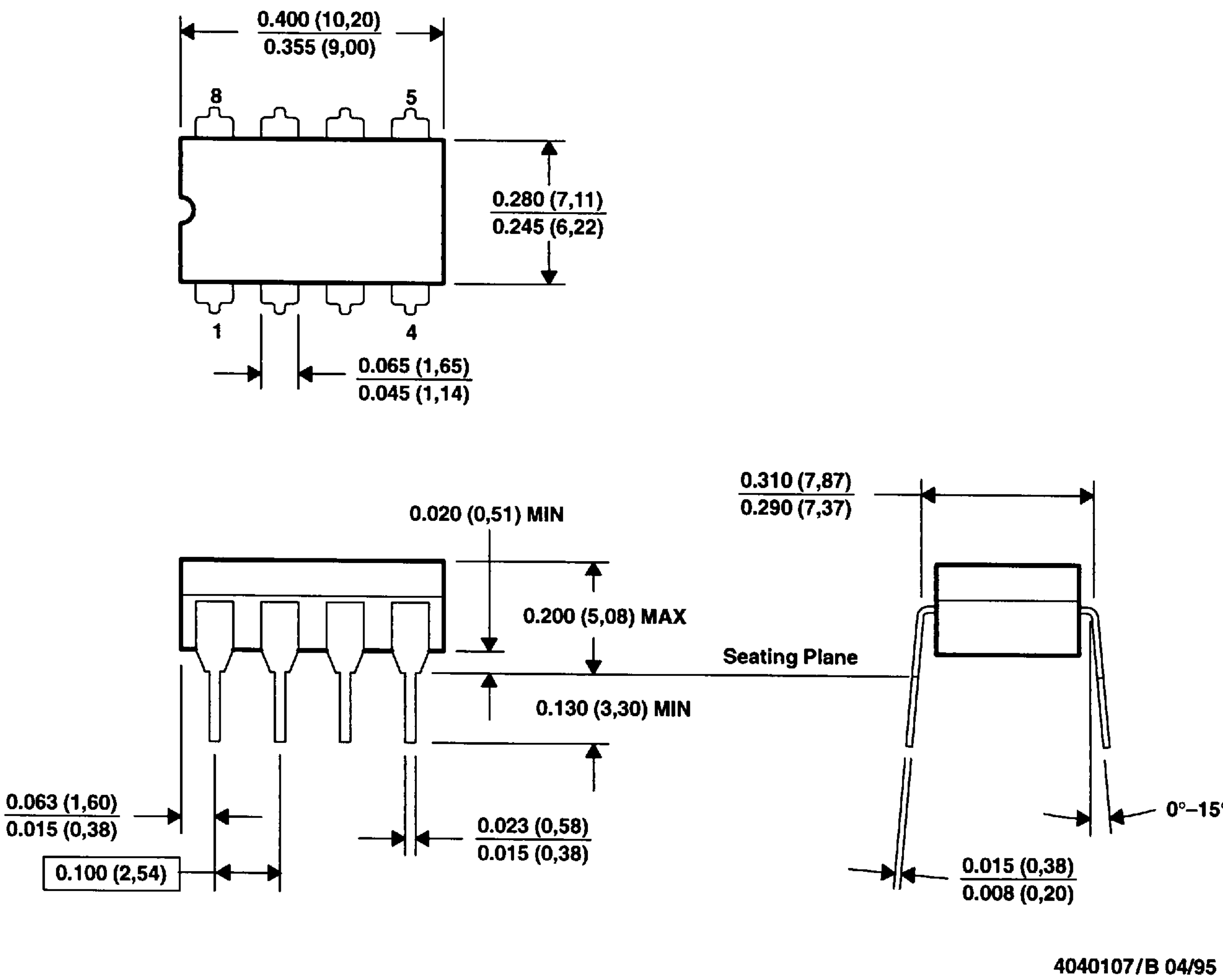


4040140/C 11/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

MECHANICAL INFORMATION

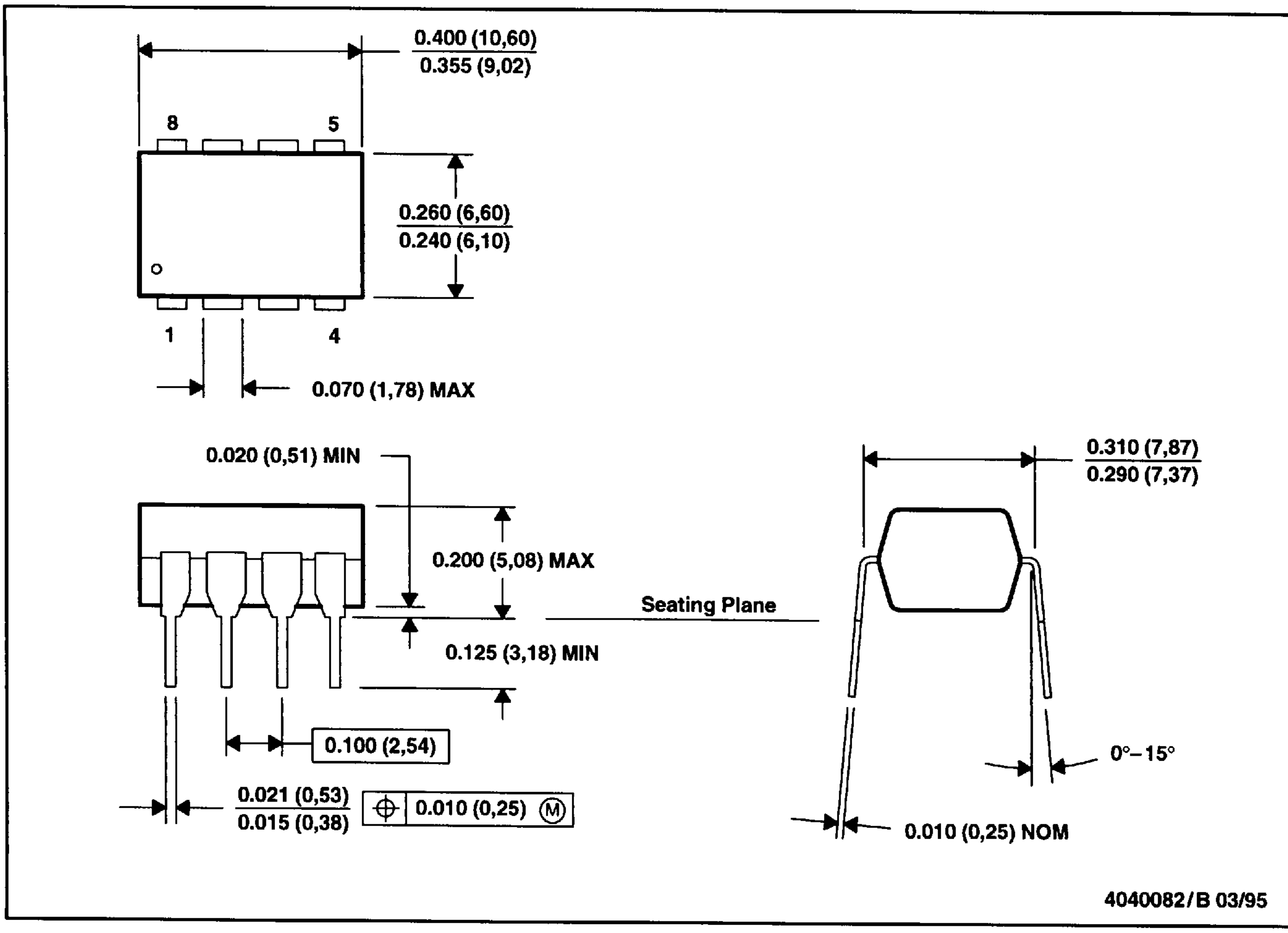
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
- E. Falls within MIL-STD-1835 GDIP1-T8

MECHANICAL INFORMATION

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001