

NSB1706DMW5T1G, NSVB1706DMW5T1G

Dual Bias Resistor Transistor

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSB1706DMW5T1G, two BRT devices are housed in the SC-88A package which is ideal for low power surface mount applications where board space is at a premium.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted, common for Q₁ and Q₂)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V _{CBO}	50	Vdc
Collector-Emitter Voltage	V _{CEO}	50	Vdc
Collector Current	I _C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation T _A = 25°C Derate above 25°C	P _D	187 (Note 1) 256 (Note 2) 1.5 (Note 1) 2.0 (Note 2)	mW mW/°C
Thermal Resistance, Junction-to-Ambient	R _{θJA}	670 (Note 1) 490 (Note 2)	°C/W
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation T _A = 25°C Derate above 25°C	P _D	250 (Note 1) 385 (Note 2) 2.0 (Note 1) 3.0 (Note 2)	mW mW/°C
Thermal Resistance, Junction-to-Ambient	R _{θJA}	493 (Note 1) 325 (Note 2)	°C/W
Thermal Resistance, Junction-to-Lead	R _{θJL}	188 (Note 1) 208 (Note 2)	°C/W
Junction and Storage Temperature	T _J , T _{stg}	-55 to +150	°C

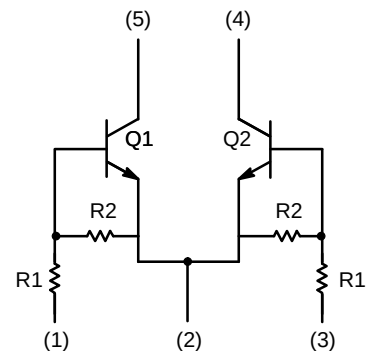
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-4 @ Minimum Pad.
2. FR-4 @ 1.0 x 1.0 inch Pad.



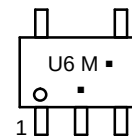
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SC-88A
CASE 419A
STYLE 1

MARKING DIAGRAM



U6 = Device Marking
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NSB1706DMW5T1G	SC-88A (Pb-Free)	3000 / Tape & Reel
NSVB1706DMW5T1G	SC-88A (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NSB1706DMW5T1G, NSVB1706DMW5T1G

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q₁ and Q₂)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current ($V_{CB} = 50\text{ V}$, $I_E = 0$)	I_{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current ($V_{CE} = 50\text{ V}$, $I_B = 0$)	I_{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current ($V_{EB} = 6.0\text{ V}$, $I_C = 0$)	I_{EBO}	–	–	0.18	mAdc
Collector-Base Breakdown Voltage ($I_C = 10\text{ }\mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 3) ($I_C = 2.0\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	50	–	–	Vdc

ON CHARACTERISTICS (Note 3)

DC Current Gain ($V_{CE} = 10\text{ V}$, $I_C = 5.0\text{ mA}$)	h_{FE}	80	200	–	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ mA}$, $I_B = 1\text{ mA}$)	$V_{CE(sat)}$	–	–	0.25	Vdc
Input Voltage (off) ($V_{CE} = 5.0\text{ V}$, $I_C = 100\text{ }\mu\text{A}$)	$V_{i(off)}$	–	0.6	0.5	Vdc
Input Voltage (on) ($V_{CE} = 0.3\text{ V}$, $I_C = 5\text{ mA}$)	$V_{i(on)}$	1.3	0.9	–	Vdc
Output Voltage (on) ($V_{CC} = 5.0\text{ V}$, $V_B = 2.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	V_{OL}	–	–	0.2	Vdc
Output Voltage (off) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.25\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	V_{OH}	4.9	–	–	Vdc
Input Resistor	R1	3.3	4.7	6.1	k Ω
Resistor Ratio	R1/R2	0.055	0.1	0.185	

NOTE: New resistor combinations. Updated curves to follow in subsequent data sheets.

3. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%.

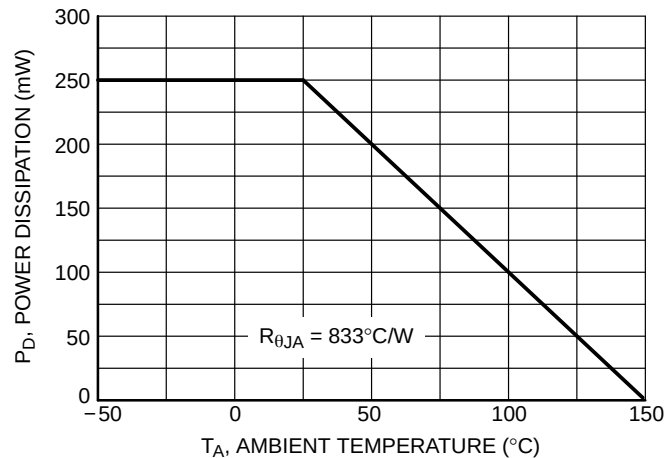


Figure 1. Derating Curve

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

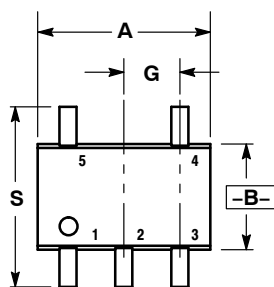
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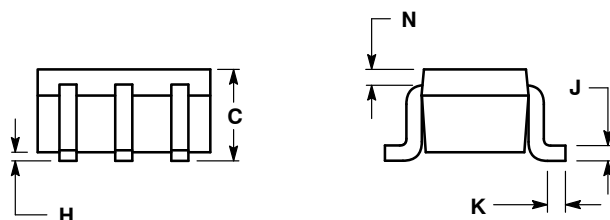
SCALE 2:1

SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE L

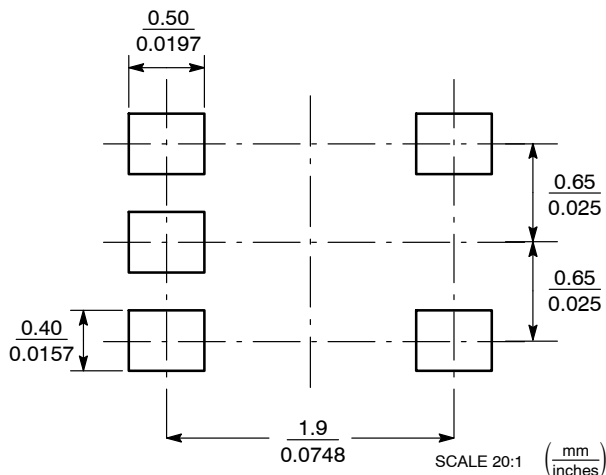
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D 5 PL $\oplus$ 0.2 (0.008) (M) B (M)



SOLDER FOOTPRINT

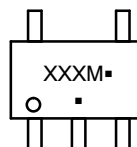


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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DESCRIPTION:	SC-88A (SC-70-5/SOT-353)	PAGE 1 OF 1

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