

# MUN5312DW1, NSBC124EPDXV6, NSBC124EPDP6

## Complementary Bias Resistor Transistors

**R1 = 22 kΩ, R2 = 22 kΩ**

### NPN and PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

#### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable\*
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### MAXIMUM RATINGS

(T<sub>A</sub> = 25°C both polarities Q<sub>1</sub> (PNP) & Q<sub>2</sub> (NPN), unless otherwise noted)

| Rating                         | Symbol               | Max | Unit             |
|--------------------------------|----------------------|-----|------------------|
| Collector-Base Voltage         | V <sub>CBO</sub>     | 50  | Vdc              |
| Collector-Emitter Voltage      | V <sub>CEO</sub>     | 50  | Vdc              |
| Collector Current – Continuous | I <sub>C</sub>       | 100 | mA <sub>dc</sub> |
| Input Forward Voltage          | V <sub>IN(fwd)</sub> | 40  | Vdc              |
| Input Reverse Voltage          | V <sub>IN(rev)</sub> | 10  | Vdc              |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### ORDERING INFORMATION

| Device                                  | Package | Shipping <sup>†</sup> |
|-----------------------------------------|---------|-----------------------|
| MUN5312DW1T1G,<br>SMUN5312DW1T1G*       | SOT-363 | 3,000 / Tape & Reel   |
| NSVMUN5312DW1T3G*                       | SOT-363 | 10,000 / Tape & Reel  |
| MUN5312DW1T2G,<br>NSVMUN5312DW1T2G*     | SOT-363 | 3,000 / Tape & Reel   |
| NSBC124EPDXV6T1G,<br>NSVBC124EPDXV6T1G* | SOT-563 | 4,000 / Tape & Reel   |
| NSBC124EPDXV6T5G                        | SOT-563 | 8,000 / Tape & Reel   |
| NSBC124EPDP6T5G                         | SOT-963 | 8,000 / Tape & Reel   |

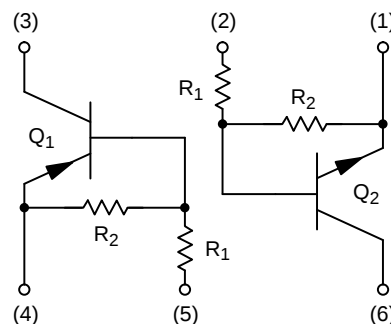
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



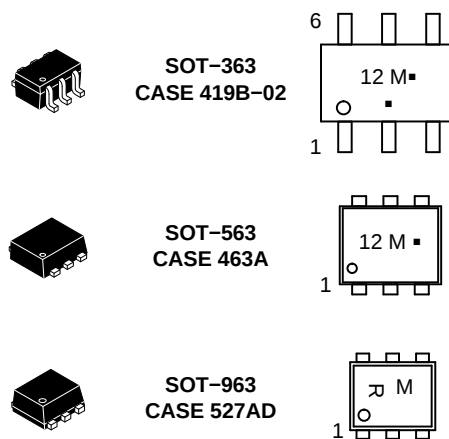
**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)

#### PIN CONNECTIONS



#### MARKING DIAGRAMS



12/R = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

# MUN5312DW1, NSBC124EPDXV6, NSBC124EPDP6

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|----------------|--------|-----|------|
|----------------|--------|-----|------|

### MUN5312DW1 (SOT-363) ONE JUNCTION HEATED

|                                                                                                                  |                  |                          |                 |
|------------------------------------------------------------------------------------------------------------------|------------------|--------------------------|-----------------|
| Total Device Dissipation<br>T <sub>A</sub> = 25°C (Note 1)<br>(Note 2)<br>Derate above 25°C (Note 1)<br>(Note 2) | P <sub>D</sub>   | 187<br>256<br>1.5<br>2.0 | mW<br><br>mW/°C |
| Thermal Resistance,<br>Junction to Ambient (Note 1)<br>(Note 2)                                                  | R <sub>θJA</sub> | 670<br>490               | °C/W            |

### MUN5312DW1 (SOT-363) BOTH JUNCTION HEATED (Note 3)

|                                                                                                                  |                                   |                          |                 |
|------------------------------------------------------------------------------------------------------------------|-----------------------------------|--------------------------|-----------------|
| Total Device Dissipation<br>T <sub>A</sub> = 25°C (Note 1)<br>(Note 2)<br>Derate above 25°C (Note 1)<br>(Note 2) | P <sub>D</sub>                    | 250<br>385<br>2.0<br>3.0 | mW<br><br>mW/°C |
| Thermal Resistance,<br>Junction to Ambient (Note 1)<br>(Note 2)                                                  | R <sub>θJA</sub>                  | 493<br>325               | °C/W            |
| Thermal Resistance,<br>Junction to Lead (Note 1)<br>(Note 2)                                                     | R <sub>θJL</sub>                  | 188<br>208               | °C/W            |
| Junction and Storage Temperature Range                                                                           | T <sub>J</sub> , T <sub>stg</sub> | -55 to +150              | °C              |

### NSBC124EPDXV6 (SOT-563) ONE JUNCTION HEATED

|                                                                                          |                  |            |             |
|------------------------------------------------------------------------------------------|------------------|------------|-------------|
| Total Device Dissipation<br>T <sub>A</sub> = 25°C (Note 1)<br>Derate above 25°C (Note 1) | P <sub>D</sub>   | 357<br>2.9 | mW<br>mW/°C |
| Thermal Resistance,<br>Junction to Ambient (Note 1)                                      | R <sub>θJA</sub> | 350        | °C/W        |

### NSBC124EPDXV6 (SOT-563) BOTH JUNCTION HEATED (Note 3)

|                                                                                          |                                   |             |             |
|------------------------------------------------------------------------------------------|-----------------------------------|-------------|-------------|
| Total Device Dissipation<br>T <sub>A</sub> = 25°C (Note 1)<br>Derate above 25°C (Note 1) | P <sub>D</sub>                    | 500<br>4.0  | mW<br>mW/°C |
| Thermal Resistance,<br>Junction to Ambient (Note 1)                                      | R <sub>θJA</sub>                  | 250         | °C/W        |
| Junction and Storage Temperature Range                                                   | T <sub>J</sub> , T <sub>stg</sub> | -55 to +150 | °C          |

### NSBC124EPDP6 (SOT-963) ONE JUNCTION HEATED

|                                                                                                                  |                  |                          |                 |
|------------------------------------------------------------------------------------------------------------------|------------------|--------------------------|-----------------|
| Total Device Dissipation<br>T <sub>A</sub> = 25°C (Note 4)<br>(Note 5)<br>Derate above 25°C (Note 4)<br>(Note 5) | P <sub>D</sub>   | 231<br>269<br>1.9<br>2.2 | MW<br><br>mW/°C |
| Thermal Resistance,<br>Junction to Ambient (Note 4)<br>(Note 5)                                                  | R <sub>θJA</sub> | 540<br>464               | °C/W            |

### NSBC124EPDP6 (SOT-963) BOTH JUNCTION HEATED (Note 3)

|                                                                                                                  |                                   |                          |                 |
|------------------------------------------------------------------------------------------------------------------|-----------------------------------|--------------------------|-----------------|
| Total Device Dissipation<br>T <sub>A</sub> = 25°C (Note 4)<br>(Note 5)<br>Derate above 25°C (Note 4)<br>(Note 5) | P <sub>D</sub>                    | 339<br>408<br>2.7<br>3.3 | MW<br><br>mW/°C |
| Thermal Resistance,<br>Junction to Ambient (Note 4)<br>(Note 5)                                                  | R <sub>θJA</sub>                  | 369<br>306               | °C/W            |
| Junction and Storage Temperature Range                                                                           | T <sub>J</sub> , T <sub>stg</sub> | -55 to +150              | °C              |

1. FR-4 @ Minimum Pad.
2. FR-4 @ 1.0 × 1.0 Inch Pad.
3. Both junction heated values assume total power is sum of two equally powered channels.
4. FR-4 @ 100 mm<sup>2</sup>, 1 oz. copper traces, still air.
5. FR-4 @ 500 mm<sup>2</sup>, 1 oz. copper traces, still air.

# MUN5312DW1, NSBC124EPDXV6, NSBC124EPDP6

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ both polarities $Q_1$ (PNP) & $Q_2$ (NPN), unless otherwise noted)

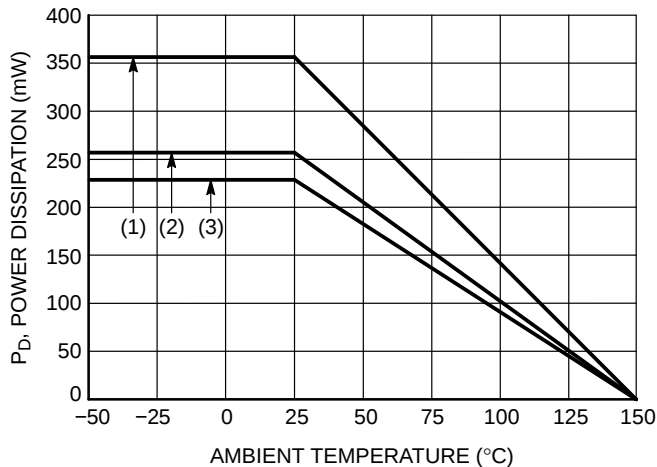
| Characteristic                                                                        | Symbol        | Min | Typ | Max | Unit |
|---------------------------------------------------------------------------------------|---------------|-----|-----|-----|------|
| <b>OFF CHARACTERISTICS</b>                                                            |               |     |     |     |      |
| Collector-Base Cutoff Current<br>( $V_{CB} = 50\text{ V}$ , $I_E = 0$ )               | $I_{CBO}$     | –   | –   | 100 | nAdc |
| Collector-Emitter Cutoff Current<br>( $V_{CE} = 50\text{ V}$ , $I_B = 0$ )            | $I_{CEO}$     | –   | –   | 500 | nAdc |
| Emitter-Base Cutoff Current<br>( $V_{EB} = 6.0\text{ V}$ , $I_C = 0$ )                | $I_{EBO}$     | –   | –   | 0.2 | mAdc |
| Collector-Base Breakdown Voltage<br>( $I_C = 10\text{ }\mu\text{A}$ , $I_E = 0$ )     | $V_{(BR)CBO}$ | 50  | –   | –   | Vdc  |
| Collector-Emitter Breakdown Voltage (Note 6)<br>( $I_C = 2.0\text{ mA}$ , $I_B = 0$ ) | $V_{(BR)CEO}$ | 50  | –   | –   | Vdc  |

## ON CHARACTERISTICS

|                                                                                                                                                                 |               |        |            |        |            |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|--------|------------|--------|------------|
| DC Current Gain (Note 6)<br>( $I_C = 5.0\text{ mA}$ , $V_{CE} = 10\text{ V}$ )                                                                                  | $h_{FE}$      | 60     | 100        | –      |            |
| Collector-Emitter Saturation Voltage (Note 6)<br>( $I_C = 10\text{ mA}$ , $I_B = 0.3\text{ mA}$ )                                                               | $V_{CE(sat)}$ | –      | –          | 0.25   | V          |
| Input Voltage (Off)<br>( $V_{CE} = 5.0\text{ V}$ , $I_C = 100\text{ }\mu\text{A}$ ) (NPN)<br>( $V_{CE} = 5.0\text{ V}$ , $I_C = 100\text{ }\mu\text{A}$ ) (PNP) | $V_{i(off)}$  | –<br>– | 1.2<br>1.2 | –<br>– | Vdc        |
| Input Voltage (On)<br>( $V_{CE} = 0.2\text{ V}$ , $I_C = 5.0\text{ mA}$ ) (NPN)<br>( $V_{CE} = 0.2\text{ V}$ , $I_C = 5.0\text{ mA}$ ) (PNP)                    | $V_{i(on)}$   | –<br>– | 1.9<br>2.0 | –<br>– | Vdc        |
| Output Voltage (On)<br>( $V_{CC} = 5.0\text{ V}$ , $V_B = 2.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )                                                          | $V_{OL}$      | –      | –          | 0.2    | Vdc        |
| Output Voltage (Off)<br>( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )                                                         | $V_{OH}$      | 4.9    | –          | –      | Vdc        |
| Input Resistor                                                                                                                                                  | $R_1$         | 15.4   | 22         | 28.6   | k $\Omega$ |
| Resistor Ratio                                                                                                                                                  | $R_1/R_2$     | 0.8    | 1.0        | 1.2    |            |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle  $\leq 2\%$ .



- (1) SOT-363; 1.0 x 1.0 Inch Pad
- (2) SOT-563; Minimum Pad
- (3) SOT-963; 100 mm<sup>2</sup>, 1 oz. Copper Trace

Figure 1. Derating Curve

TYPICAL CHARACTERISTICS – NPN TRANSISTOR  
MUN5312DW1, NSBC124EPDXV6

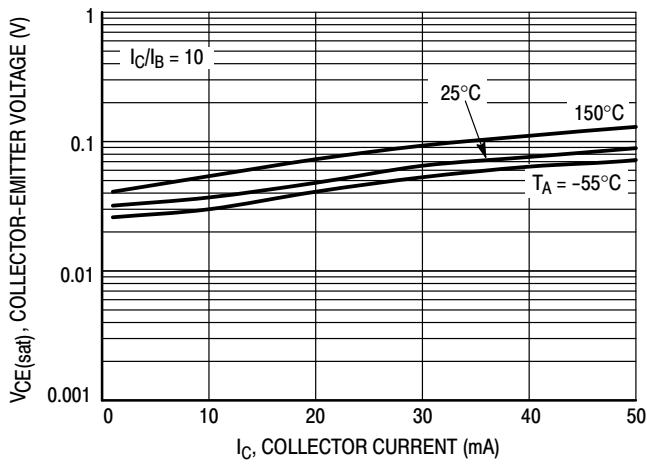


Figure 2.  $V_{CE(sat)}$  vs.  $I_C$

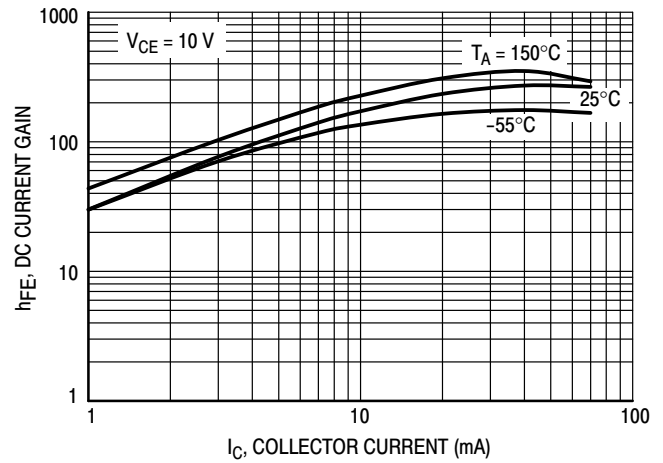


Figure 3. DC Current Gain

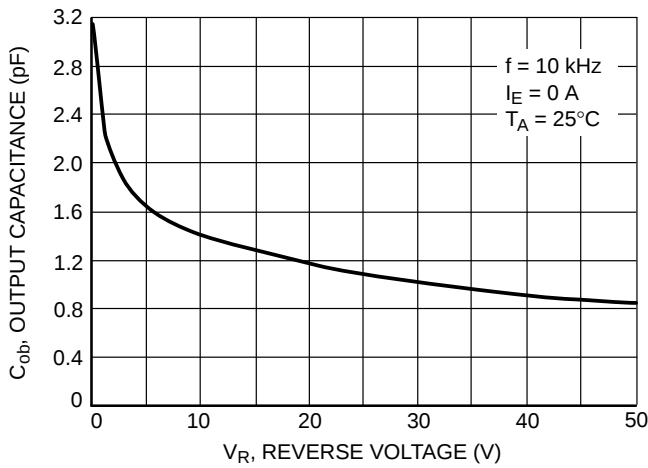


Figure 4. Output Capacitance

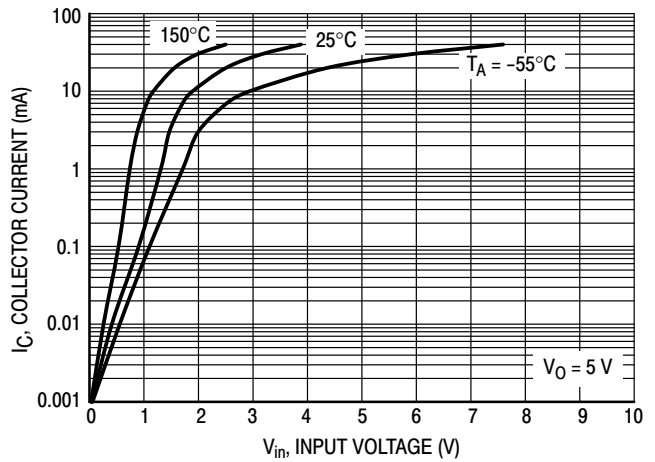


Figure 5. Output Current vs. Input Voltage

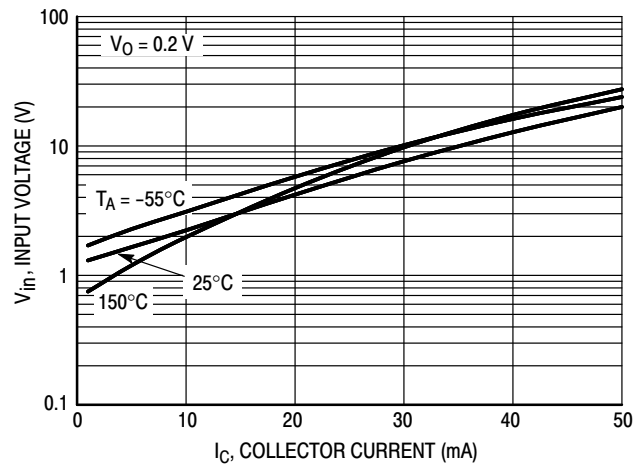


Figure 6. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – PNP TRANSISTOR  
MUN5312DW1, NSBC124EPDXV6

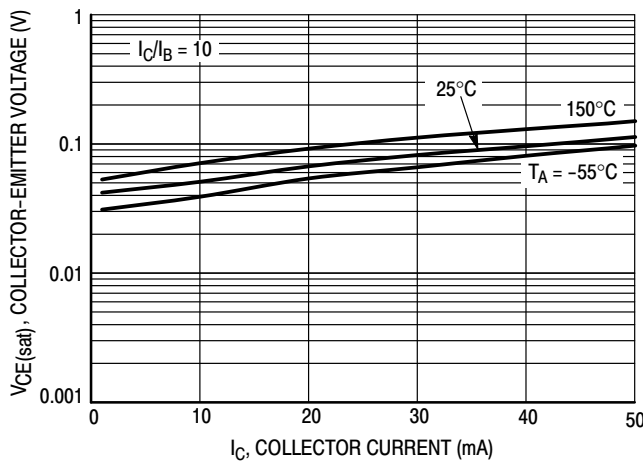


Figure 7.  $V_{CE(sat)}$  vs.  $I_C$

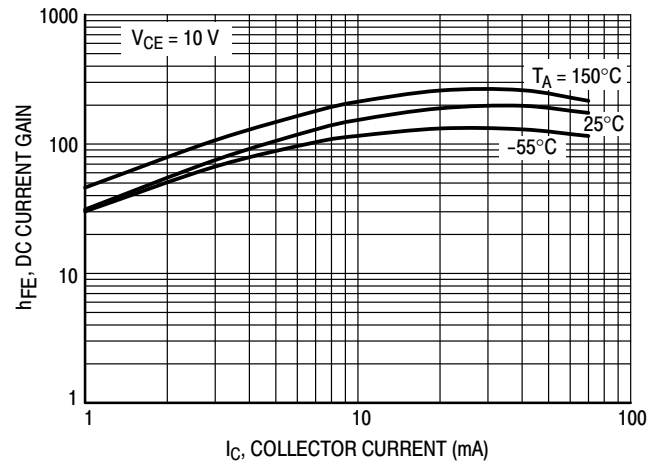


Figure 8. DC Current Gain

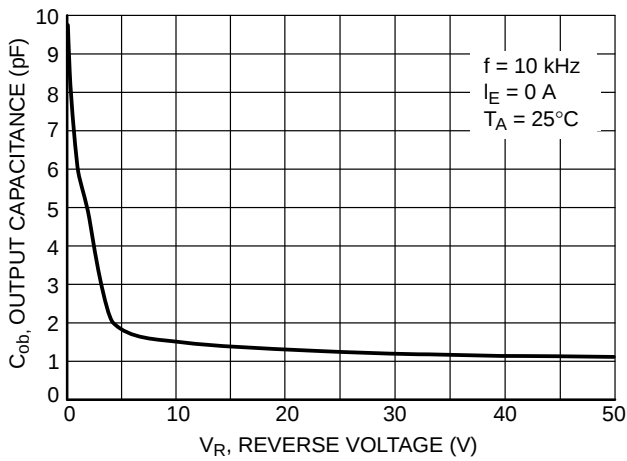


Figure 9. Output Capacitance

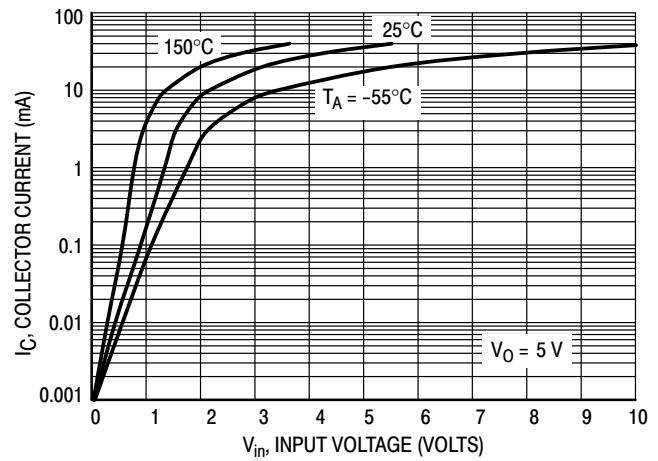


Figure 10. Output Current vs. Input Voltage

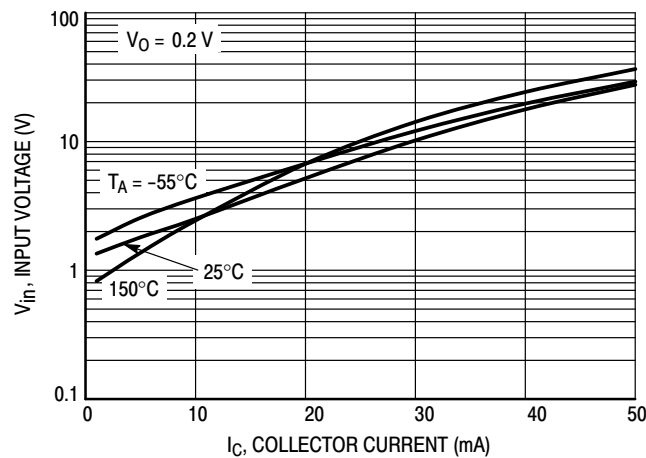


Figure 11. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – NPN TRANSISTOR  
NSBC124EPDP6

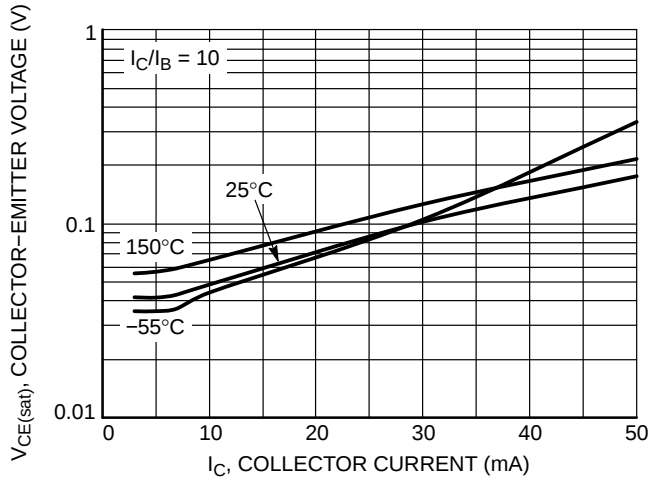


Figure 12.  $V_{CE(sat)}$  vs.  $I_C$

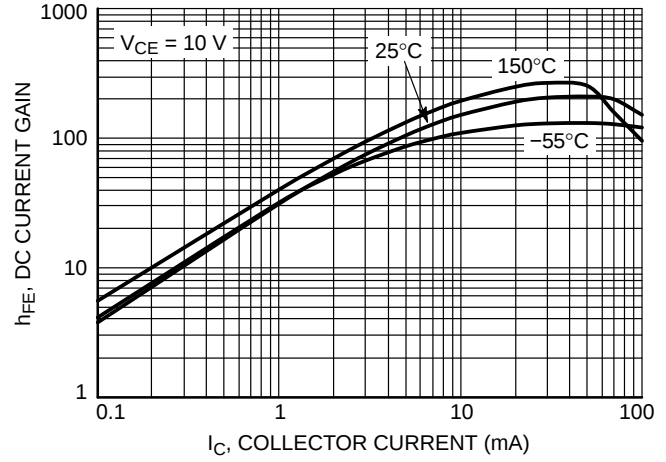


Figure 13. DC Current Gain

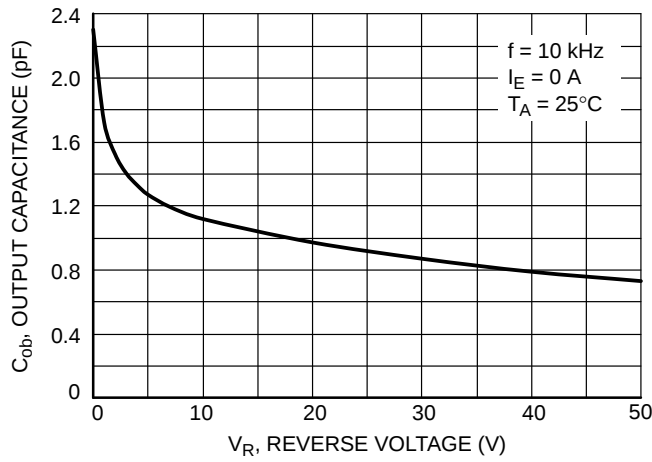


Figure 14. Output Capacitance

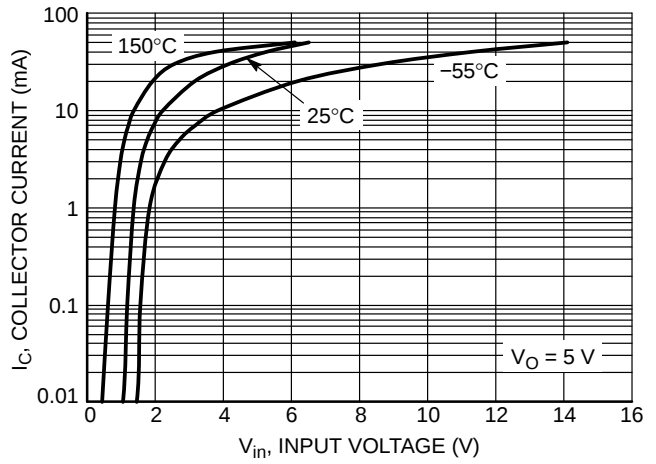


Figure 15. Output Current vs. Input Voltage

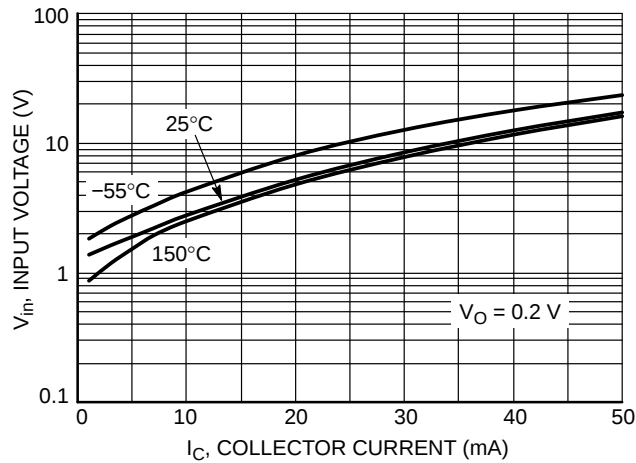


Figure 16. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – PNP TRANSISTOR  
NSBC124EPDP6

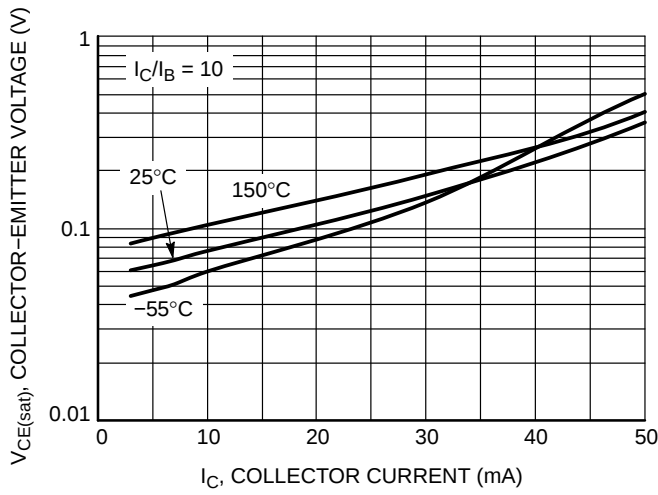


Figure 17.  $V_{CE(sat)}$  vs.  $I_C$

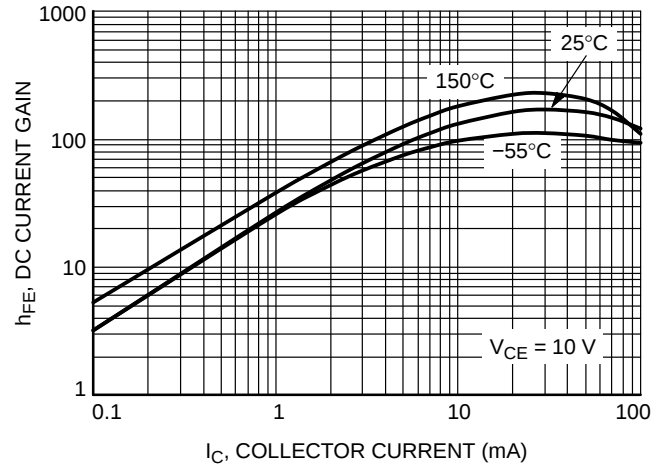


Figure 18. DC Current Gain

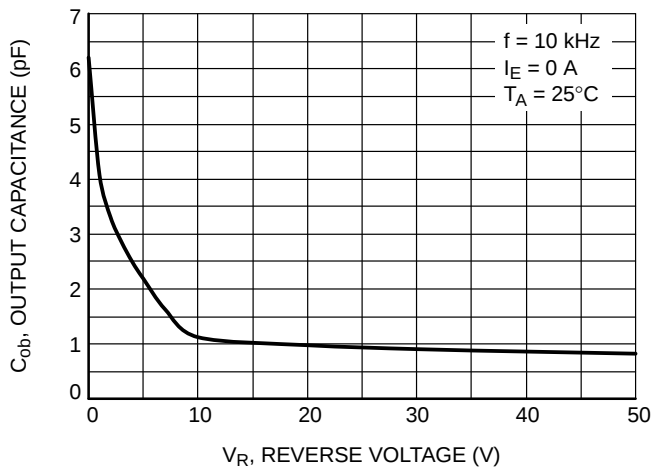


Figure 19. Output Capacitance

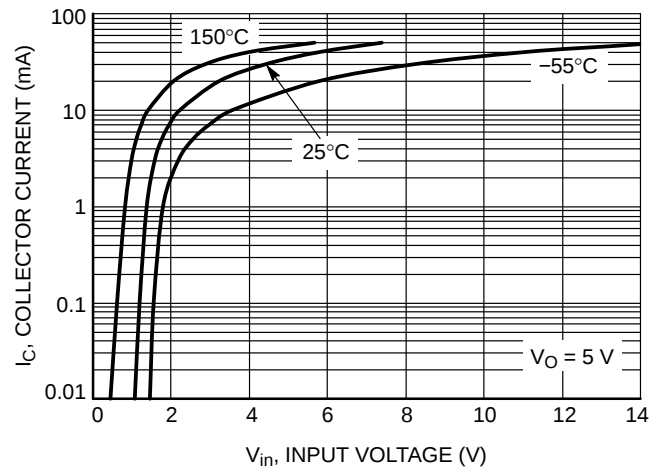


Figure 20. Output Current vs. Input Voltage

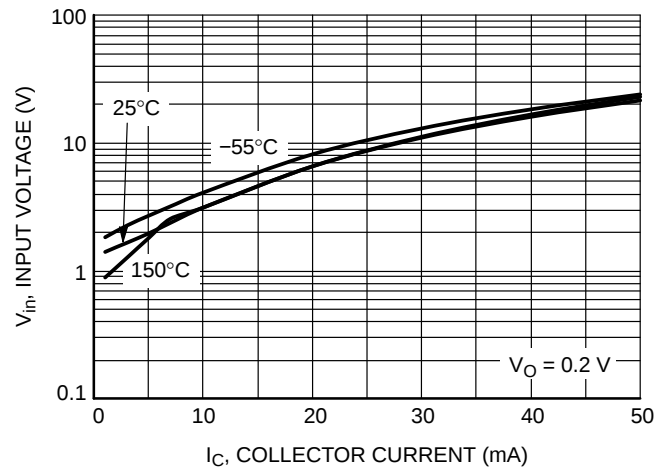


Figure 21. Input Voltage vs. Output Current

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

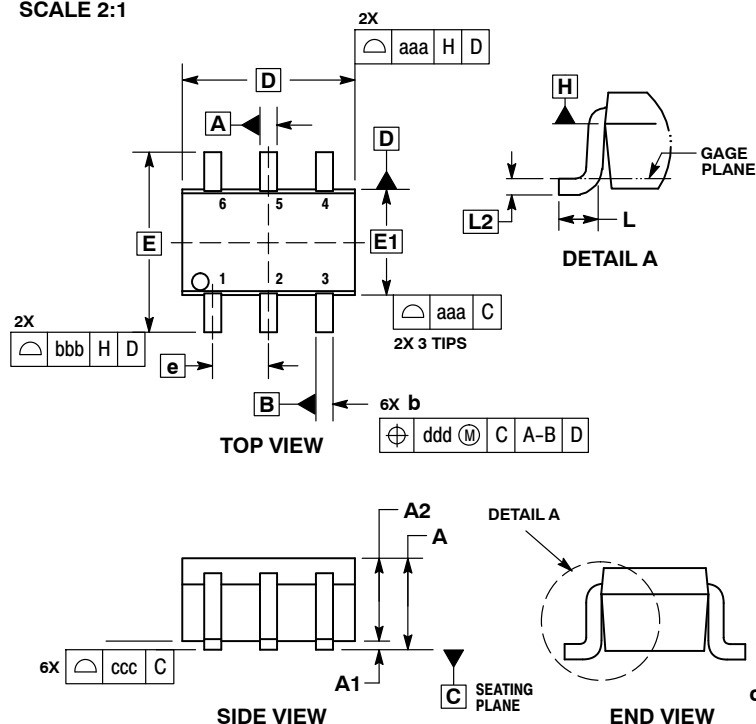
ON Semiconductor®



SCALE 2:1

SC-88/SC70-6/SOT-363  
CASE 419B-02  
ISSUE Y

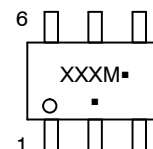
DATE 11 DEC 2012



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
  4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
  5. DATUMS A AND B ARE DETERMINED AT DATUM H.
  6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
  7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

| DIM | MILLIMETERS |      |      | INCHES    |       |       |
|-----|-------------|------|------|-----------|-------|-------|
|     | MIN         | NOM  | MAX  | MIN       | NOM   | MAX   |
| A   | ---         | ---  | 1.10 | ---       | ---   | 0.043 |
| A1  | 0.00        | ---  | 0.10 | 0.000     | ---   | 0.004 |
| A2  | 0.70        | 0.90 | 1.00 | 0.027     | 0.035 | 0.039 |
| b   | 0.15        | 0.20 | 0.25 | 0.006     | 0.008 | 0.010 |
| C   | 0.08        | 0.15 | 0.22 | 0.003     | 0.006 | 0.009 |
| D   | 1.80        | 2.00 | 2.20 | 0.070     | 0.078 | 0.086 |
| E   | 2.00        | 2.10 | 2.20 | 0.078     | 0.082 | 0.086 |
| E1  | 1.15        | 1.25 | 1.35 | 0.045     | 0.049 | 0.053 |
| e   | 0.65 BSC    |      |      | 0.026 BSC |       |       |
| L   | 0.26        | 0.36 | 0.46 | 0.010     | 0.014 | 0.018 |
| L2  | 0.15 BSC    |      |      | 0.006 BSC |       |       |
| aaa | 0.15        |      |      | 0.006     |       |       |
| bbb | 0.30        |      |      | 0.012     |       |       |
| ccc | 0.10        |      |      | 0.004     |       |       |
| ddd | 0.10        |      |      | 0.004     |       |       |

## GENERIC MARKING DIAGRAM\*



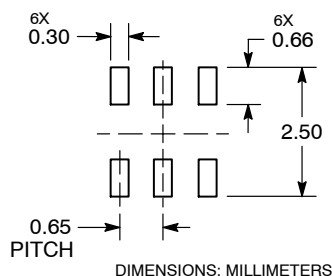
XXX = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

## RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## STYLES ON PAGE 2

|                         |                             |                                                                                                                                                                                     |
|-------------------------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DOCUMENT NUMBER:</b> | <b>98ASB42985B</b>          | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>SC-88/SC70-6/SOT-363</b> | <b>PAGE 1 OF 2</b>                                                                                                                                                                  |

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**SC-88/SC70-6/SOT-363**  
**CASE 419B-02**  
**ISSUE Y**

DATE 11 DEC 2012

|                                                                                                                   |                                                                                                               |                                                                                                                    |                                                                                                                    |                                                                                                                    |                                                                                                              |
|-------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|
| <b>STYLE 1:</b><br>PIN 1. EMITTER 2<br>2. BASE 2<br>3. COLLECTOR 1<br>4. EMITTER 1<br>5. BASE 1<br>6. COLLECTOR 2 | <b>STYLE 2:</b><br>CANCELLED                                                                                  | <b>STYLE 3:</b><br>CANCELLED                                                                                       | <b>STYLE 4:</b><br>PIN 1. CATHODE<br>2. CATHODE<br>3. COLLECTOR<br>4. EMITTER<br>5. BASE<br>6. ANODE               | <b>STYLE 5:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. COLLECTOR<br>4. EMITTER<br>5. BASE<br>6. CATHODE                 | <b>STYLE 6:</b><br>PIN 1. ANODE 2<br>2. N/C<br>3. CATHODE 1<br>4. ANODE 1<br>5. N/C<br>6. CATHODE 2          |
| <b>STYLE 7:</b><br>PIN 1. SOURCE 2<br>2. DRAIN 2<br>3. GATE 1<br>4. SOURCE 1<br>5. DRAIN 1<br>6. GATE 2           | <b>STYLE 8:</b><br>CANCELLED                                                                                  | <b>STYLE 9:</b><br>PIN 1. EMITTER 2<br>2. EMITTER 1<br>3. COLLECTOR 1<br>4. BASE 1<br>5. BASE 2<br>6. COLLECTOR 2  | <b>STYLE 10:</b><br>PIN 1. SOURCE 2<br>2. SOURCE 1<br>3. GATE 1<br>4. DRAIN 1<br>5. DRAIN 2<br>6. GATE 2           | <b>STYLE 11:</b><br>PIN 1. CATHODE 2<br>2. CATHODE 2<br>3. ANODE 1<br>4. CATHODE 1<br>5. CATHODE 1<br>6. ANODE 2   | <b>STYLE 12:</b><br>PIN 1. ANODE 2<br>2. ANODE 2<br>3. CATHODE 1<br>4. ANODE 1<br>5. ANODE 1<br>6. CATHODE 2 |
| <b>STYLE 13:</b><br>PIN 1. ANODE<br>2. N/C<br>3. COLLECTOR<br>4. EMITTER<br>5. BASE<br>6. CATHODE                 | <b>STYLE 14:</b><br>PIN 1. VREF<br>2. GND<br>3. GND<br>4. IOUT<br>5. VEN<br>6. VCC                            | <b>STYLE 15:</b><br>PIN 1. ANODE 1<br>2. ANODE 2<br>3. ANODE 3<br>4. CATHODE 3<br>5. CATHODE 2<br>6. CATHODE 1     | <b>STYLE 16:</b><br>PIN 1. BASE 1<br>2. EMITTER 2<br>3. COLLECTOR 2<br>4. BASE 2<br>5. EMITTER 1<br>6. COLLECTOR 1 | <b>STYLE 17:</b><br>PIN 1. BASE 1<br>2. EMITTER 1<br>3. COLLECTOR 2<br>4. BASE 2<br>5. EMITTER 2<br>6. COLLECTOR 1 | <b>STYLE 18:</b><br>PIN 1. VIN1<br>2. VCC<br>3. VOUT2<br>4. VIN2<br>5. GND<br>6. VOUT1                       |
| <b>STYLE 19:</b><br>PIN 1. IOUT<br>2. GND<br>3. GND<br>4. V CC<br>5. V EN<br>6. V REF                             | <b>STYLE 20:</b><br>PIN 1. COLLECTOR<br>2. COLLECTOR<br>3. BASE<br>4. EMITTER<br>5. COLLECTOR<br>6. COLLECTOR | <b>STYLE 21:</b><br>PIN 1. ANODE 1<br>2. N/C<br>3. ANODE 2<br>4. CATHODE 2<br>5. N/C<br>6. CATHODE 1               | <b>STYLE 22:</b><br>PIN 1. D1 (i)<br>2. GND<br>3. D2 (i)<br>4. D2 (c)<br>5. VBUS<br>6. D1 (c)                      | <b>STYLE 23:</b><br>PIN 1. Vn<br>2. CH1<br>3. Vp<br>4. N/C<br>5. CH2<br>6. N/C                                     | <b>STYLE 24:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. CATHODE<br>5. CATHODE<br>6. CATHODE       |
| <b>STYLE 25:</b><br>PIN 1. BASE 1<br>2. CATHODE<br>3. COLLECTOR 2<br>4. BASE 2<br>5. EMITTER<br>6. COLLECTOR 1    | <b>STYLE 26:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. DRAIN 2<br>4. SOURCE 2<br>5. GATE 2<br>6. DRAIN 1      | <b>STYLE 27:</b><br>PIN 1. BASE 2<br>2. BASE 1<br>3. COLLECTOR 1<br>4. EMITTER 1<br>5. EMITTER 2<br>6. COLLECTOR 2 | <b>STYLE 28:</b><br>PIN 1. DRAIN<br>2. DRAIN<br>3. GATE<br>4. SOURCE<br>5. DRAIN<br>6. DRAIN                       | <b>STYLE 29:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. COLLECTOR<br>4. EMITTER<br>5. BASE/ANODE<br>6. CATHODE          | <b>STYLE 30:</b><br>PIN 1. SOURCE 1<br>2. DRAIN 2<br>3. DRAIN 2<br>4. SOURCE 2<br>5. GATE 1<br>6. DRAIN 1    |

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

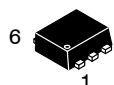
|                         |                             |                                                                                                                                                                                     |
|-------------------------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DOCUMENT NUMBER:</b> | <b>98ASB42985B</b>          | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>SC-88/SC70-6/SOT-363</b> | <b>PAGE 2 OF 2</b>                                                                                                                                                                  |

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 4:1

### SOT-563, 6 LEAD

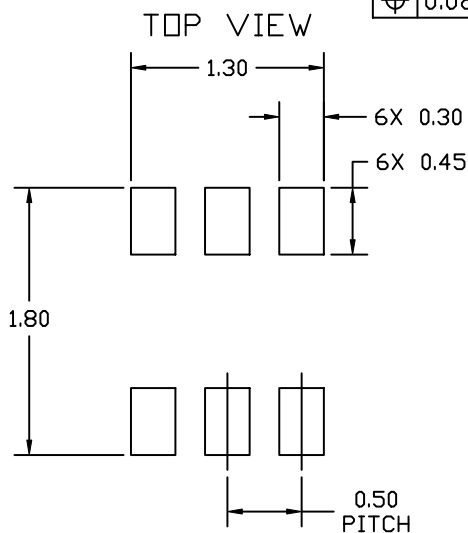
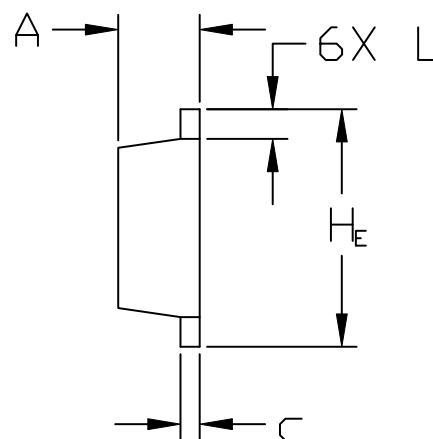
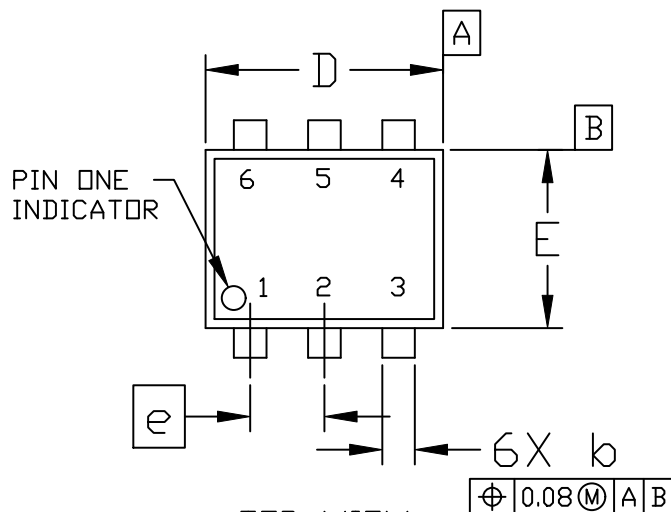
CASE 463A

ISSUE H

DATE 26 JAN 2021

#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.



SIDE VIEW

| DIM            | MILLIMETERS |      |      |
|----------------|-------------|------|------|
|                | MIN.        | NOM. | MAX. |
| A              | 0.50        | 0.55 | 0.60 |
| b              | 0.17        | 0.22 | 0.27 |
| c              | 0.08        | 0.13 | 0.18 |
| D              | 1.50        | 1.60 | 1.70 |
| E              | 1.10        | 1.20 | 1.30 |
| e              | 0.50 BSC    |      |      |
| L              | 0.10        | 0.20 | 0.30 |
| H <sub>E</sub> | 1.50        | 1.60 | 1.70 |

#### RECOMMENDED MOUNTING FOOTPRINT\*

- \* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                  |                 |                                                                                                                                                                                  |
|------------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98AON11126D     | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | SOT-563, 6 LEAD | PAGE 1 OF 2                                                                                                                                                                      |

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**SOT-563, 6 LEAD**  
CASE 463A  
ISSUE H

DATE 26 JAN 2021

STYLE 1:  
PIN 1. EMITTER 1  
2. BASE 1  
3. COLLECTOR 2  
4. EMITTER 2  
5. BASE 2  
6. COLLECTOR 1

STYLE 2:  
PIN 1. EMITTER 1  
2. EMITTER 2  
3. BASE 2  
4. COLLECTOR 2  
5. BASE 1  
6. COLLECTOR 1

STYLE 3:  
PIN 1. CATHODE 1  
2. CATHODE 1  
3. ANODE/ANODE 2  
4. CATHODE 2  
5. CATHODE 2  
6. ANODE/ANODE 1

STYLE 4:  
PIN 1. COLLECTOR  
2. COLLECTOR  
3. BASE  
4. EMITTER  
5. COLLECTOR  
6. COLLECTOR

STYLE 5:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE  
4. ANODE  
5. CATHODE  
6. CATHODE

STYLE 6:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. CATHODE  
5. CATHODE  
6. CATHODE

STYLE 7:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. CATHODE  
5. ANODE  
6. CATHODE

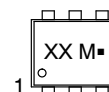
STYLE 8:  
PIN 1. DRAIN  
2. DRAIN  
3. GATE  
4. SOURCE  
5. DRAIN  
6. DRAIN

STYLE 9:  
PIN 1. SOURCE 1  
2. GATE 1  
3. DRAIN 2  
4. SOURCE 2  
5. GATE 2  
6. DRAIN 1

STYLE 10:  
PIN 1. CATHODE 1  
2. N/C  
3. CATHODE 2  
4. ANODE 2  
5. N/C  
6. ANODE 1

STYLE 11:  
PIN 1. EMITTER 2  
2. BASE 2  
3. COLLECTOR 1  
4. EMITTER 1  
5. BASE 1  
6. COLLECTOR 2

**GENERIC  
MARKING DIAGRAM\***



XX = Specific Device Code  
M = Month Code  
■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

|                         |                        |                                                                                                                                                                                     |
|-------------------------|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DOCUMENT NUMBER:</b> | <b>98AON11126D</b>     | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>SOT-563, 6 LEAD</b> | <b>PAGE 2 OF 2</b>                                                                                                                                                                  |

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

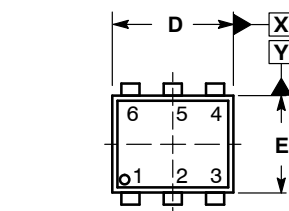
ON Semiconductor®



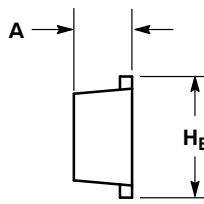
SCALE 4:1

**SOT-963**  
CASE 527AD-01  
ISSUE E

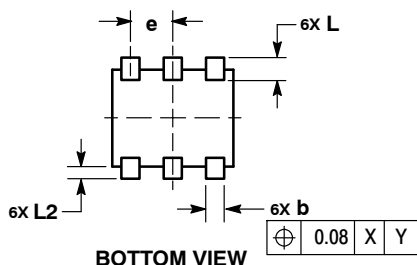
DATE 09 FEB 2010



TOP VIEW



SIDE VIEW



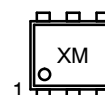
BOTTOM VIEW

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM            | MILLIMETERS |      |      |
|----------------|-------------|------|------|
|                | MIN         | NOM  | MAX  |
| A              | 0.34        | 0.37 | 0.40 |
| b              | 0.10        | 0.15 | 0.20 |
| C              | 0.07        | 0.12 | 0.17 |
| D              | 0.95        | 1.00 | 1.05 |
| E              | 0.75        | 0.80 | 0.85 |
| e              | 0.35 BSC    |      |      |
| H <sub>E</sub> | 0.95        | 1.00 | 1.05 |
| L              | 0.19 REF    |      |      |
| L2             | 0.05        | 0.10 | 0.15 |

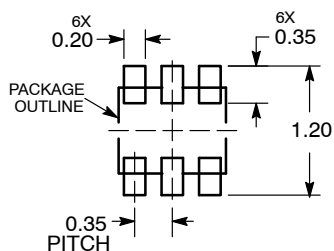
## GENERIC MARKING DIAGRAM\*



X = Specific Device Code  
M = Month Code

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

## RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

STYLE 1:  
PIN 1. EMITTER 1  
2. BASE 1  
3. COLLECTOR 2  
4. EMITTER 2  
5. BASE 2  
6. COLLECTOR 1

STYLE 2:  
PIN 1. EMITTER 1  
2. EMITTER 2  
3. BASE 2  
4. COLLECTOR 2  
5. BASE 1  
6. COLLECTOR 1

STYLE 3:  
PIN 1. CATHODE 1  
2. CATHODE 1  
3. ANODE/ANODE 2  
4. CATHODE 2  
5. CATHODE 2  
6. ANODE/ANODE 1

STYLE 4:  
PIN 1. COLLECTOR  
2. COLLECTOR  
3. BASE  
4. EMITTER  
5. COLLECTOR  
6. COLLECTOR

STYLE 5:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE  
4. ANODE  
5. CATHODE  
6. CATHODE

STYLE 6:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. CATHODE  
5. CATHODE  
6. CATHODE

STYLE 7:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. CATHODE  
5. ANODE  
6. CATHODE

STYLE 8:  
PIN 1. DRAIN  
2. DRAIN  
3. GATE  
4. SOURCE  
5. DRAIN  
6. DRAIN

STYLE 9:  
PIN 1. SOURCE 1  
2. GATE 1  
3. DRAIN 2  
4. SOURCE 2  
5. GATE 2  
6. DRAIN 1

STYLE 10:  
PIN 1. CATHODE 1  
2. N/C  
3. CATHODE 2  
4. ANODE 2  
5. N/C  
6. ANODE 1

DOCUMENT NUMBER: 98AON26456D

DESCRIPTION: SOT-963, 1X1, 0.35P

Electronic versions are uncontrolled except when accessed directly from the Document Repository.  
Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative