

BUL642D2

High Speed, High Gain Bipolar NPN Transistor with Integrated Collector-Emitter and Built-in Efficient Antisaturation Network

The BUL642D2 is a state-of-the-art High Speed High Gain Bipolar Transistor (H2BIP). Tight dynamic characteristics and lot to lot minimum spread (150 ns on storage time) make it ideally suitable for Light Ballast Application. A new development process brings avalanche energy capability, making the device extremely rugged.

Features

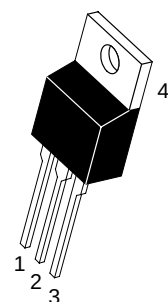
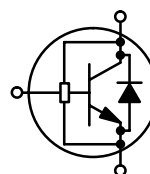
- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ $I_C = 300 \text{ mA}/5 \text{ V}$
- Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread
- Integrated Collector-Emitter Free Wheeling Diode
- Fully Characterized Dynamic V_{CEsat}
- "Six Sigma" Process Providing Tight and Reproducible Parameter Spreads
- Avalanche Energy 20 mJ Typical Capability
- Pb-Free Package is Available*



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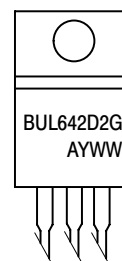
<http://onsemi.com>

**3 AMPERES
825 VOLTS
75 WATTS
POWER TRANSISTOR**



TO-220AB
CASE 221A
STYLE 1

MARKING DIAGRAM



BUL642D2 = Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
BUL642D2	TO-220	50 Units/Rail
BUL642D2G	TO-220 (Pb-Free)	50 Units/Rail

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

BUL642D2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	V_{CEO}	440	Vdc
Collector-Base Breakdown Voltage	V_{CES}	825	Vdc
Emitter-Base Voltage	V_{EBO}	11	Vdc
Collector Current – Continuous – Peak (Note 1)	I_C I_{CM}	3.0 8.0	Adc
Base Current – Continuous – Peak (Note 1)	I_B I_{BM}	2.0 4.0	Adc
*Total Device Dissipation @ $T_C = 25^\circ\text{C}$ *Derate above 25°C	P_D	75 0.6	W W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

TYPICAL GAIN

Rating	Symbol	Value	Unit
Typical Gain @ $I_C = 1\text{ A}$, $V_{CE} = 2\text{ V}$	h_{FE}	45	–
Typical A, $V_{CE} = 1\text{ V}$	h_{FE}	50	–

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.6	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8 in. from Case for 5 seconds	T_L	260	$^\circ\text{C}$

1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle = 10%

BUL642D2

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I _C = 200 mA, L = 25 mH)		V _{CEO(sus)}	440	–	–	Vdc
Collector–Base Breakdown Voltage (I _{CBO} = 1 mA)		V _{CBO}	825	–	–	Vdc
Emitter–Base Breakdown Voltage (I _{EBO} = 1 mA)		V _{EBO}	11	–	–	Vdc
Collector Cutoff Current (V _{CE} = Rated V _{CEO} , I _B = 0)	@ T _C = 25°C @ T _C = 125°C	I _{CEO}	– –	– –	200 1000	μAdc
Collector Cutoff Current (V _{CE} = Rated V _{CES} , V _{EB} = 0)	@ T _C = 25°C @ T _C = 125°C	I _{CES}	– –	– –	100 1000	μAdc
Emitter–Cutoff Current (V _{EB} = 10 Vdc, I _C = 0)		I _{EBO}	–	–	100	μAdc

ON CHARACTERISTICS

Base-Emitter Saturation Voltage ($I_C = 0.5\text{ Adc}$, $I_B = 100\text{ mAdc}$ ($I_C = 1\text{ Adc}$, $I_B = 0.2\text{ Adc}$)	$V_{BE(sat)}$	– –	– –	1.1 1.5	Vdc
Collector-Emitter Saturation Voltage ($I_C = 0.5\text{ Adc}$, $I_B = 50\text{ mAdc}$ ($I_C = 2\text{ Adc}$, $I_B = 0.2\text{ Adc}$)	$V_{CE(sat)}$	– –	– –	0.5 1.5	Vdc
DC Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 1\text{ Vdc}$ ($I_C = 0.5\text{ Adc}$, $V_{CE} = 3\text{ Vdc}$)	h_{FE}	16 18	– –	– –	–

DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage:	$I_C = 0.5\text{ Adc}$ $I_{B1} = 50\text{ mAdc}$ $V_{CC} = 125\text{ Vdc}$	@ $1\text{ }\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$	$V_{CE(dsat)}$	– –	2.0 5.0	– –	V
		@ $3\text{ }\mu\text{s}$	@ $T_C = 25^\circ\text{C}$		– –	0.2 1.3	– –	
	$I_C = 1\text{ Adc}$ $I_{B1} = 100\text{ mAdc}$ $V_{CC} = 300\text{ Vdc}$	@ $1\text{ }\mu\text{s}$	@ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$		– –	4.5 10	– –	
		@ $3\text{ }\mu\text{s}$	@ $T_C = 25^\circ\text{C}$		– –	1.0 3.0	– –	

DYNAMIC CHARACTERISTICS

Current Gain Bandwidth $I_C = 0.5\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1\text{ MHz}$	f_T	–	13	–	MHz
Output Capacitance @ $V_{cb} = 10\text{ V}$, $I_E = 0$, $f = 1\text{ MHz}$	C_{ob}	–	70	150	pF
Input Capacitance @ $V_{EB} = 8\text{ V}$, $f = 1\text{ MHz}$	C_{ib}	–	500	1000	pF

DIODE CHARACTERISTICS

Forward Diode Voltage ($I_{EC} = 0.5\text{ Adc}$) ($I_{EC} = 1.0\text{ Adc}$)	V_{EC}	– –	0.8 1.0	1.5 2.0	V
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SWITCHING CHARACTERISTICS: Resistive Load ($D.C. \leq 10\%$, Pulse Width = $70\text{ }\mu\text{s}$)

Delay Time	$I_C = 0.5\text{ Adc}$	t_d	–	60	400	ns
Rise Time	$I_{B1} = 45\text{ mA}$	t_r	–	160	1100	ns
Storage Time	$I_{B2} = 500\text{ mA}$	t_s	–	0.5	1400	μs
Fall Time	$V_{CC} = 125\text{ V}$	t_f	–	0.4	600	ns

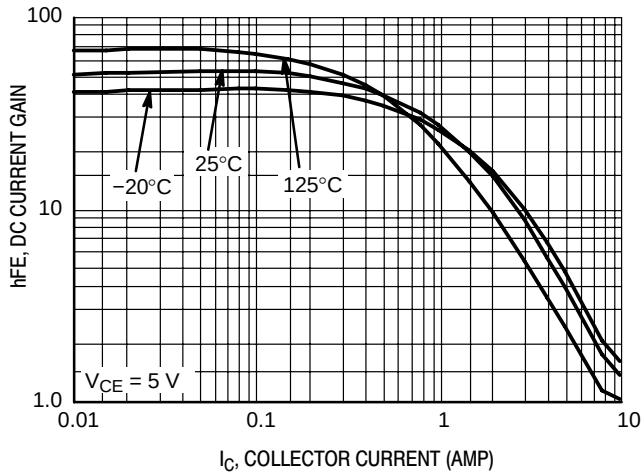


Figure 1. DC Current Gain

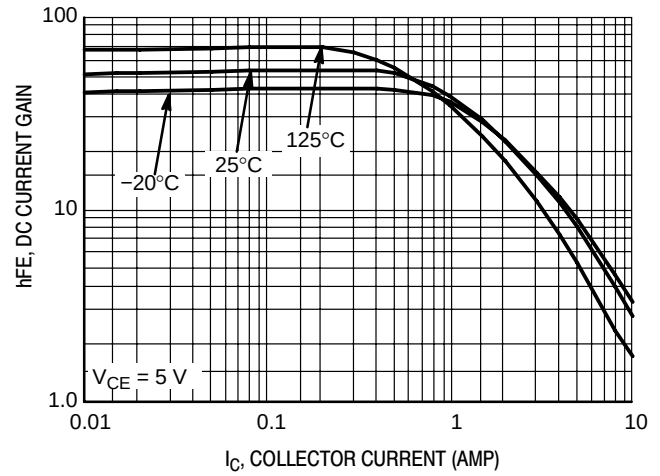


Figure 2. DC Current Gain

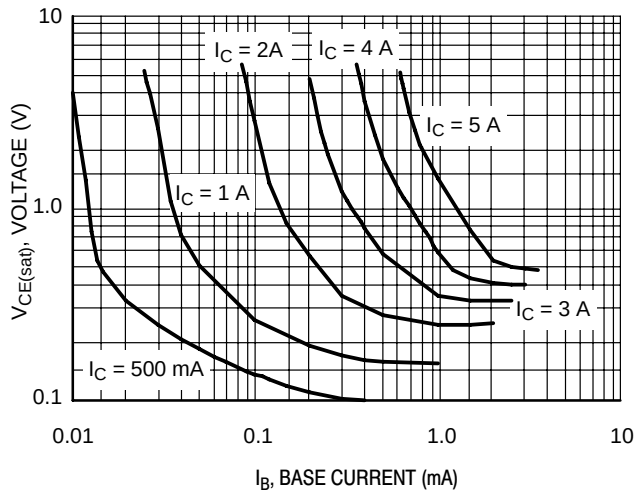


Figure 3. Collector Saturation Region

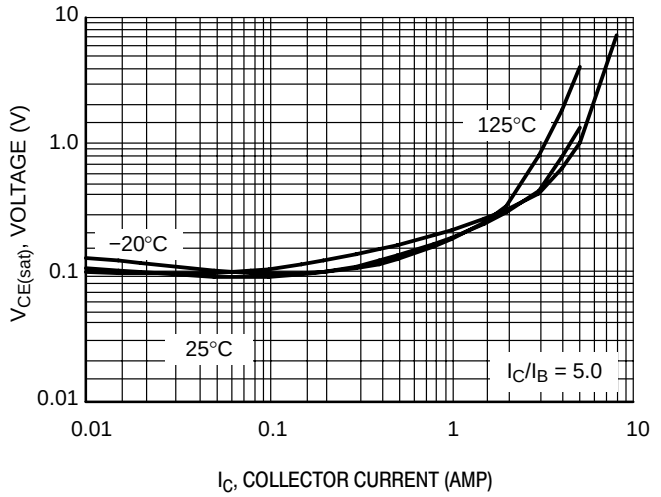


Figure 4. Collector-Emitter Saturation Voltage

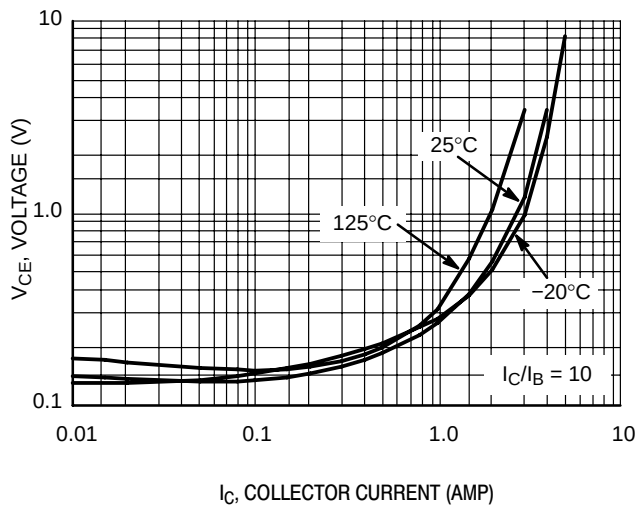


Figure 5. Collector-Emitter Saturation Voltage

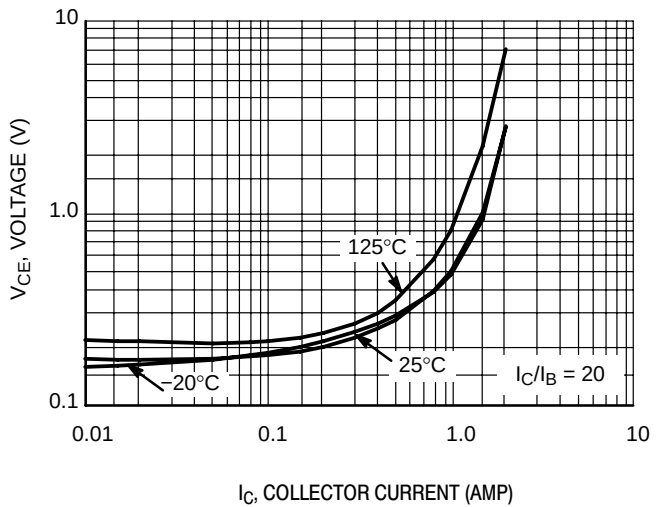


Figure 6. Collector-Emitter Saturation Voltage

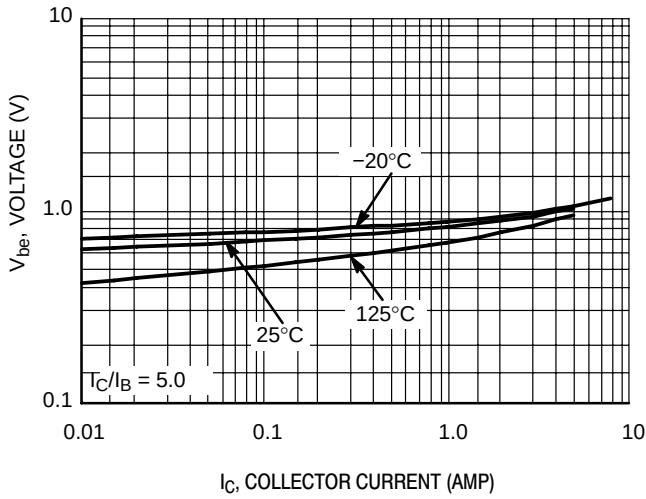


Figure 7. Base-Emitter Saturation Voltage

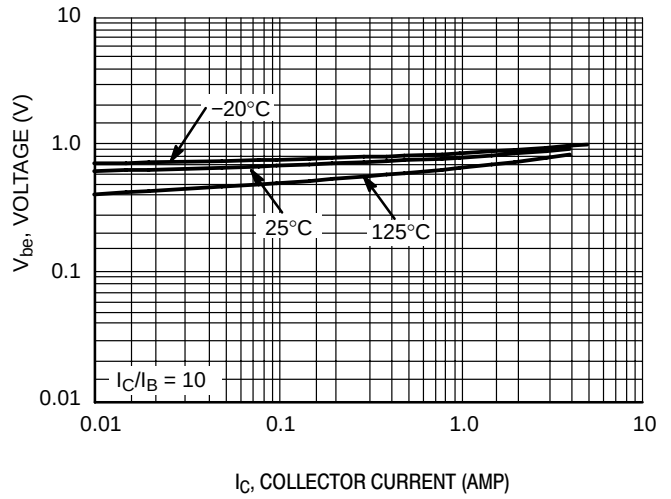


Figure 8. Base-Emitter Saturation Voltage

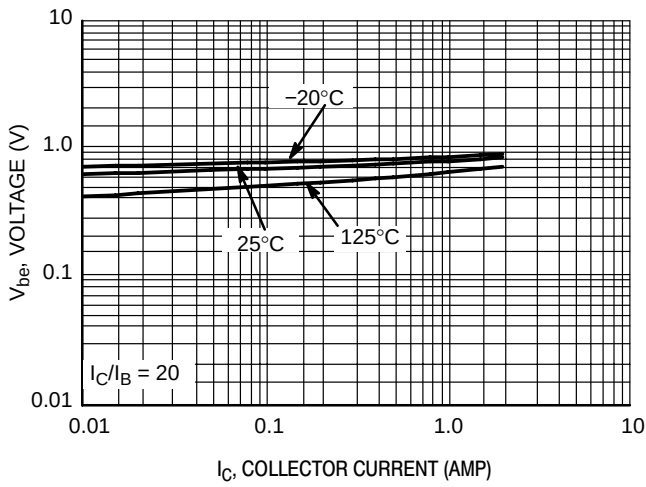


Figure 9. Base-Emitter Saturation Voltage

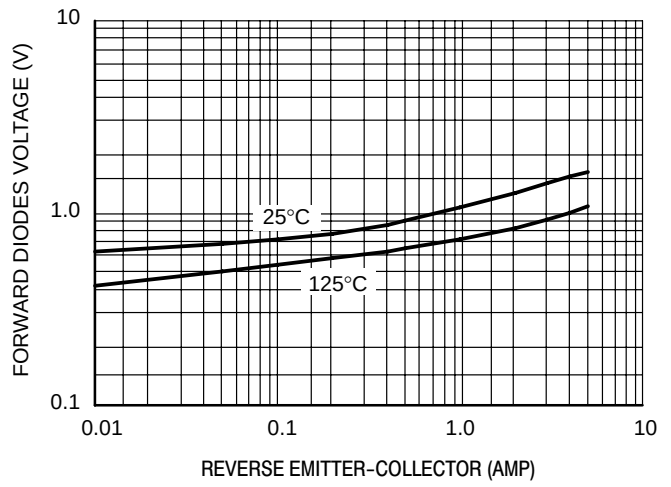


Figure 10. Forward Diode Voltage

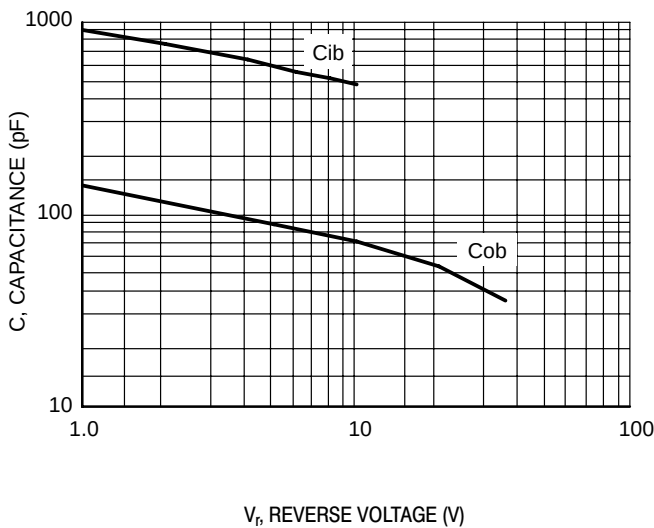


Figure 11. Capacitance

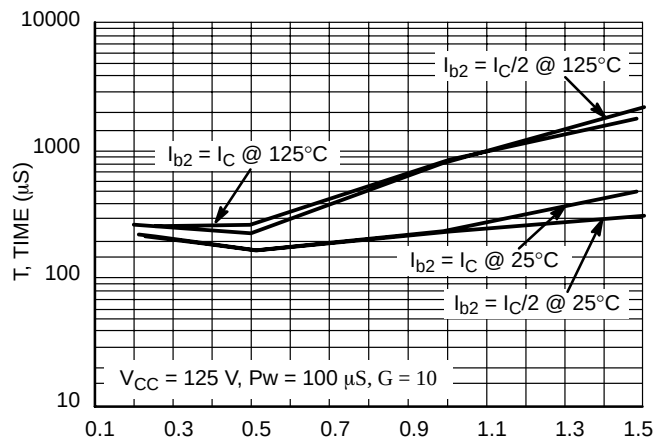


Figure 12. Resistive Switch Time, Storage Time T_{ON}

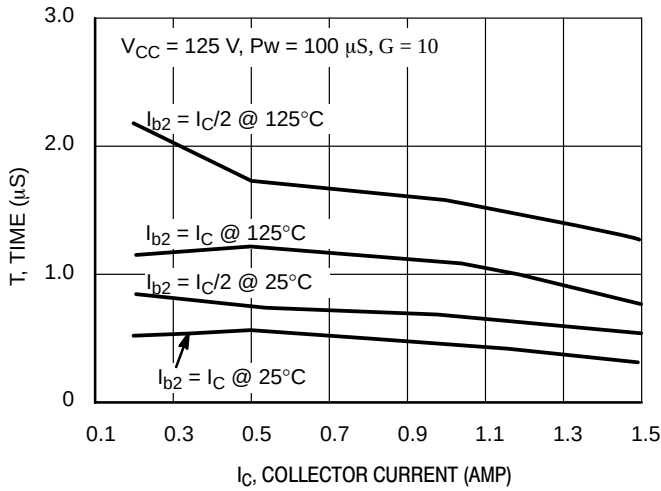


Figure 13. Resistive Switch Time, Storage Time

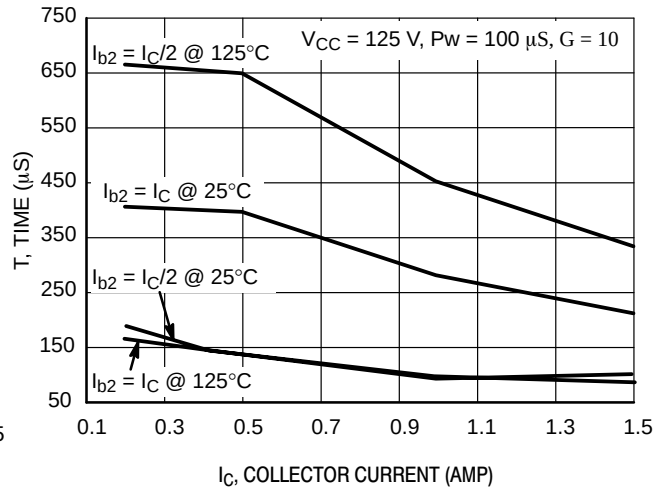


Figure 14. Resistive Switch Time, Fall Time

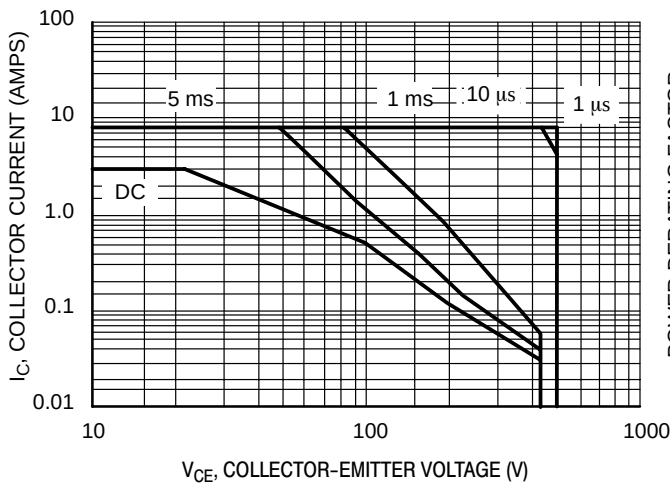


Figure 15.

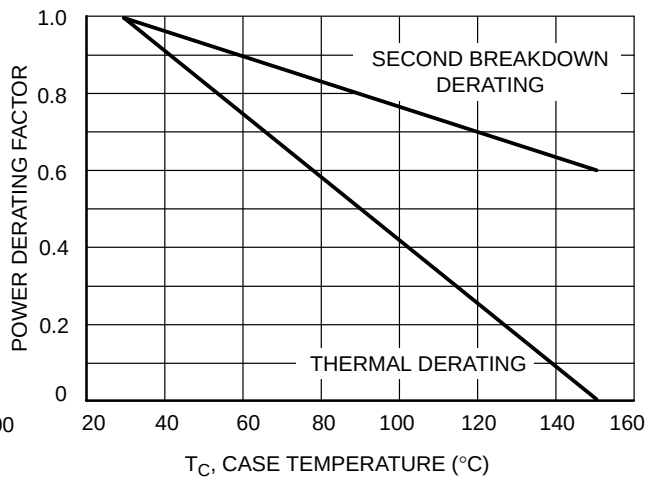


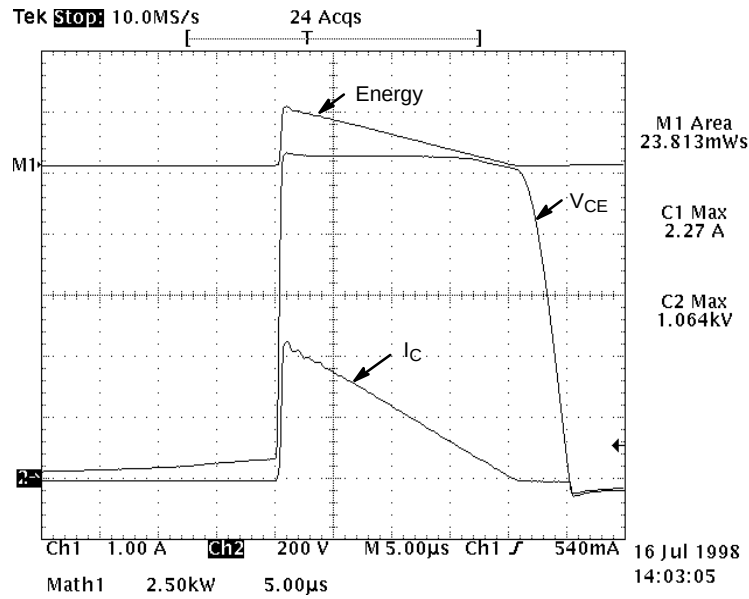
Figure 16. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on $T_C = 25^\circ\text{C}$; $T_{j(pk)}$ is variable depending on power level. Second breakdown pulse limits do not derate like

thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{j(pk)}$ may be calculated from the data in Figure 18. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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Figure 17. Typical Avalanche Energy Test/Waveforms

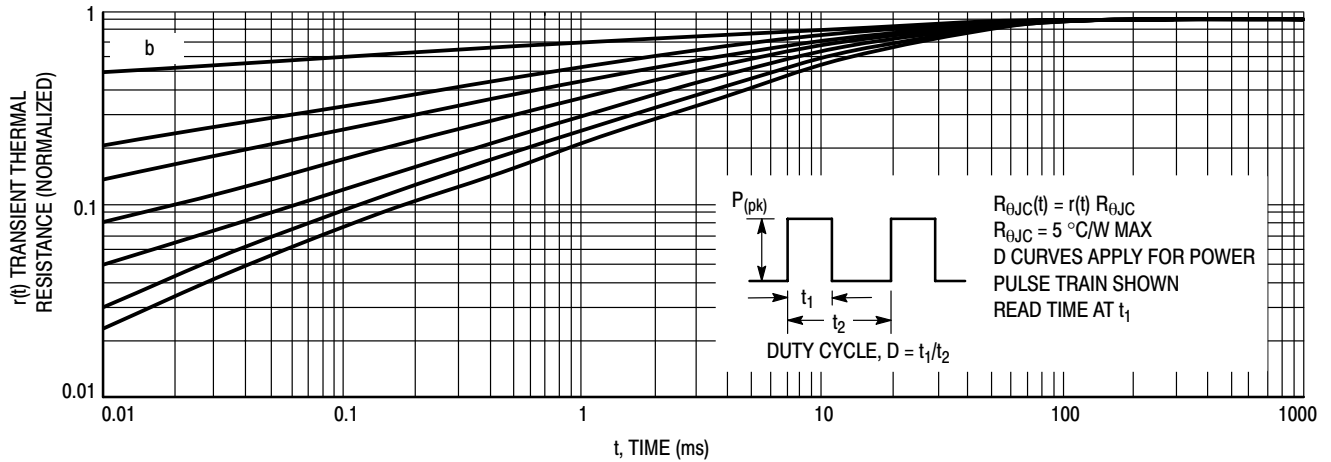
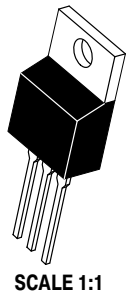


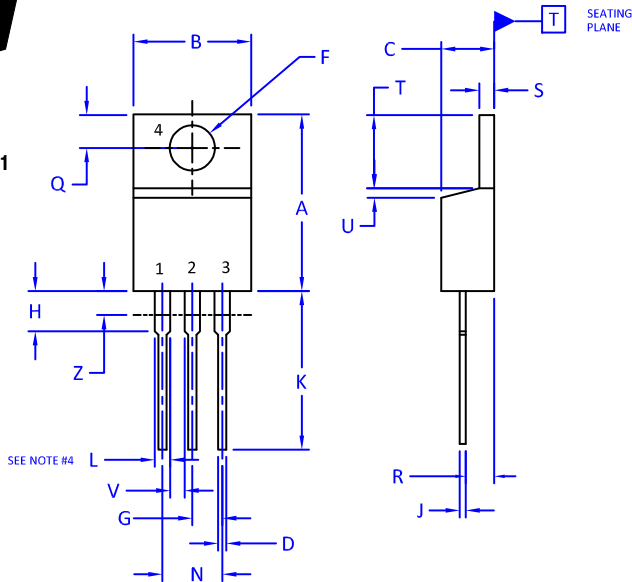
Figure 18. Thermal Response

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TO-220 CASE 221A ISSUE AK

DATE 13 JAN 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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