

# 2N4921G, 2N4922G, 2N4923G

## Medium-Power Plastic NPN Silicon Transistors

These high-performance plastic devices are designed for driver circuits, switching, and amplifier applications.

### Features

- Low Saturation Voltage
- Excellent Power Dissipation
- Excellent Safe Operating Area
- Complement to PNP 2N4920G
- These Devices are Pb-Free and are RoHS Compliant\*\*

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage 2N4921G 2N4922G 2N4923G	$V_{CEO}$	40 60 80	Vdc
Collector-Emitter Voltage 2N4921G 2N4922G 2N4923G	$V_{CB}$	40 60 80	Vdc
Emitter Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current - Continuous (Note 1)	$I_C$	1.0	Adc
Collector Current - Peak (Note 1)	$I_{CM}$	3.0	Adc
Base Current - Continuous	$I_B$	1.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	30 0.24	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The 1.0 A maximum  $I_C$  value is based upon JEDEC current gain requirements. The 3.0 A maximum value is based upon actual current handling capability of the device (see Figures 5 and 6).

### THERMAL CHARACTERISTICS (Note 2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	4.16	$^\circ\text{C}/\text{W}$

2. Recommend use of thermal compound for lowest thermal resistance.

\*Indicates JEDEC Registered Data.

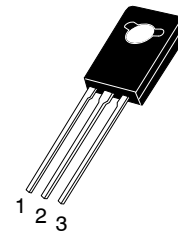
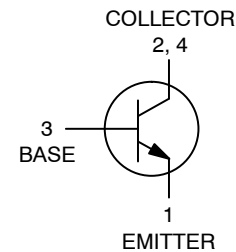
\*\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

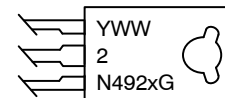
[www.onsemi.com](http://www.onsemi.com)

**1.0 AMPERE  
GENERAL PURPOSE  
POWER TRANSISTORS  
40-80 VOLTS, 30 WATTS**



**TO-225  
CASE 77-09  
STYLE 1**

### MARKING DIAGRAM



Y = Year  
WW = Work Week  
2N492x = Device Code  
x = 1, 2, or 3  
G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping
2N4921G	TO-225 (Pb-Free)	500 Units / Box
2N4922G	TO-225 (Pb-Free)	500 Units / Box
2N4923G	TO-225 (Pb-Free)	500 Units / Box

## 2N4921G, 2N4922G, 2N4923G

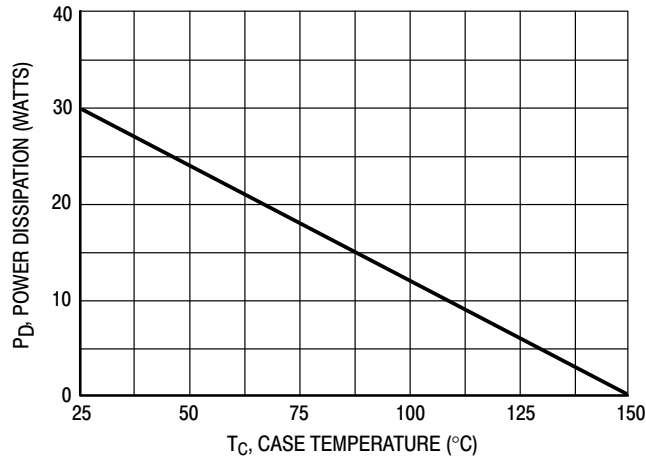
### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Sustaining Voltage (Note 3) ( $I_C = 0.1\text{ Adc}$ , $I_B = 0$ ) 2N4921G 2N4922G 2N4923G	$V_{CEO(sus)}$	40 60 80	- - -	Vdc
Collector Cutoff Current ( $V_{CE} = 20\text{ Vdc}$ , $I_B = 0$ ) 2N4921G ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ ) 2N4922G ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ ) 2N4923G	$I_{CEO}$	- - -	0.5 0.5 0.5	mAdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )	$I_{CEX}$	- -	0.1 0.5	mAdc
Collector Cutoff Current ( $V_{CB} = \text{Rated } V_{CB}$ , $I_E = 0$ )	$I_{CBO}$	-	0.1	mAdc
Emitter Cutoff Current ( $V_{EB} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	-	1.0	mAdc
<b>ON CHARACTERISTICS</b>				
DC Current Gain (Note 3) ( $I_C = 50\text{ mAdc}$ , $V_{CE} = 1.0\text{ Vdc}$ ) ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 1.0\text{ Vdc}$ ) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 1.0\text{ Vdc}$ )	$h_{FE}$	40 30 10	- 150 -	-
Collector-Emitter Saturation Voltage (Note 3) ( $I_C = 1.0\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ )	$V_{CE(sat)}$	-	0.6	Vdc
Base-Emitter Saturation Voltage (Note 3) ( $I_C = 1.0\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ )	$V_{BE(sat)}$	-	1.3	Vdc
Base-Emitter On Voltage (Note 3) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 1.0\text{ Vdc}$ )	$V_{BE(on)}$	-	1.3	Vdc
<b>SMALL-SIGNAL CHARACTERISTICS</b>				
Current-Gain - Bandwidth Product ( $I_C = 250\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$f_T$	3.0	-	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 100\text{ kHz}$ )	$C_{ob}$	-	100	pF
Small-Signal Current Gain ( $I_C = 250\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	25	-	-

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

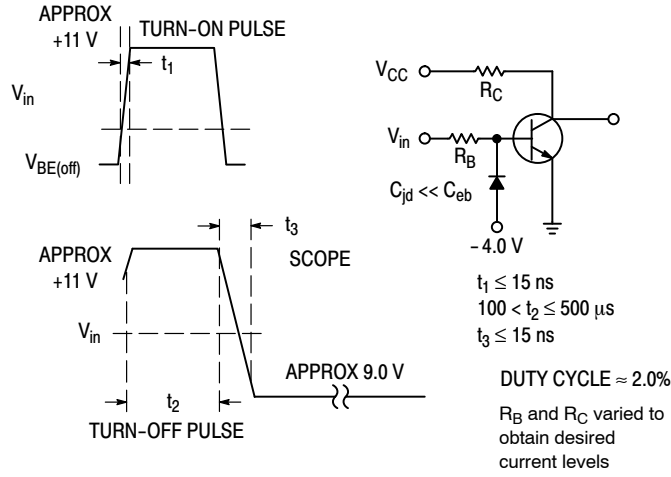
3. Pulse Test:  $PW \approx 300\ \mu\text{s}$ , Duty Cycle  $\approx 2.0\%$ .

## 2N4921G, 2N4922G, 2N4923G

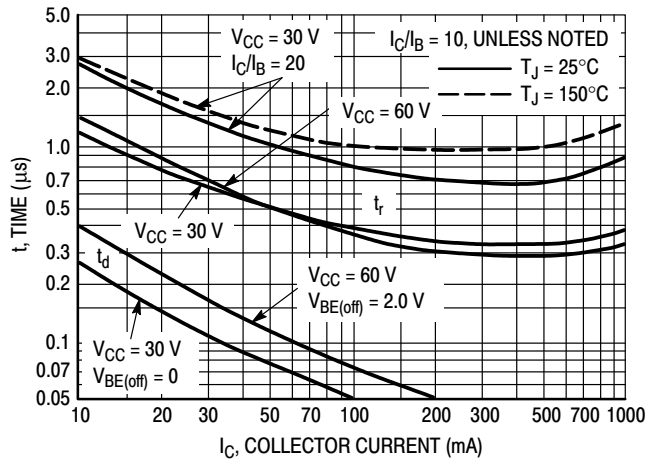


**Figure 1. Power Derating**

Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



**Figure 2. Switching Time Equivalent Circuit**



**Figure 3. Turn-On Time**

2N4921G, 2N4922G, 2N4923G

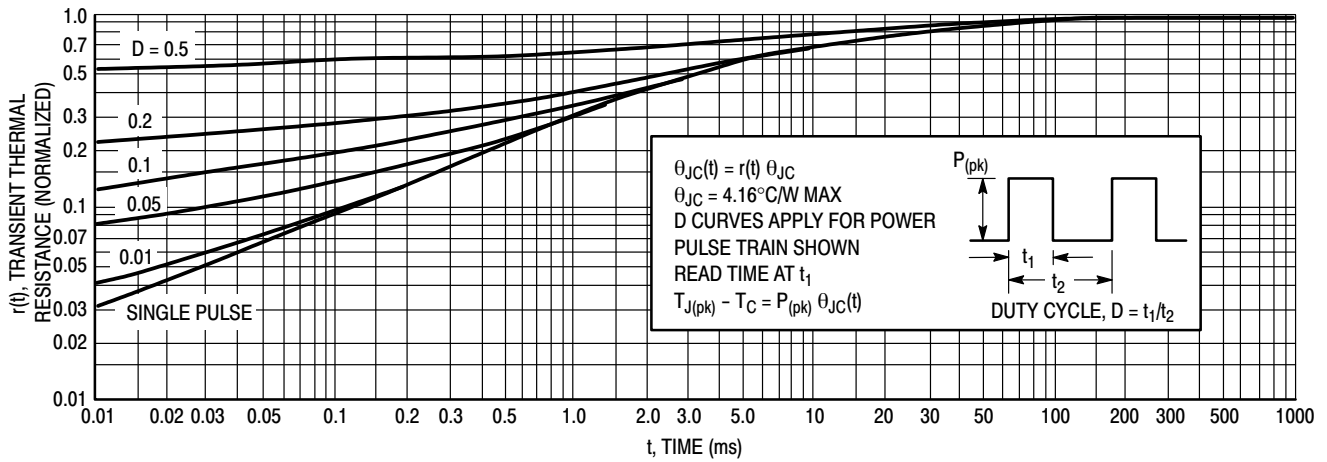


Figure 4. Thermal Response

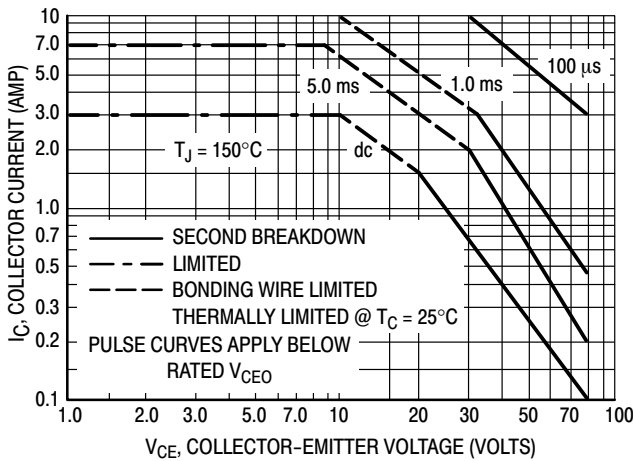


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

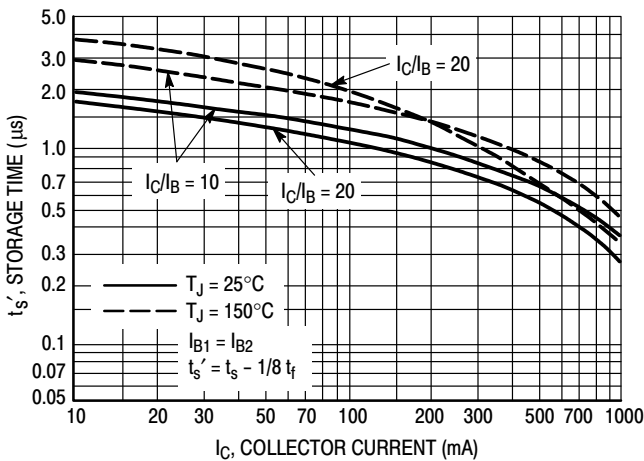


Figure 6. Storage Time

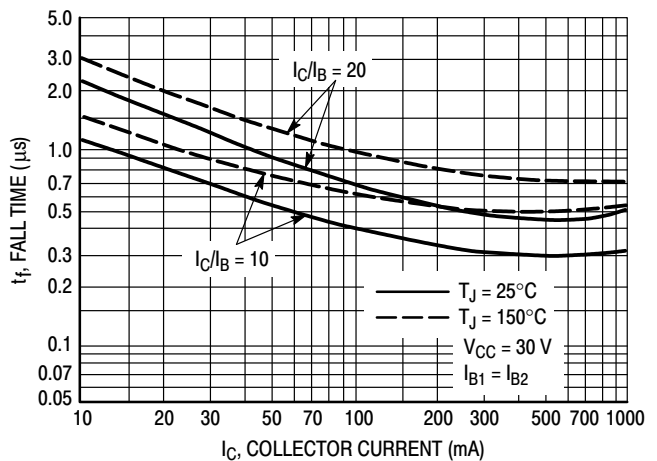


Figure 7. Fall Time

2N4921G, 2N4922G, 2N4923G

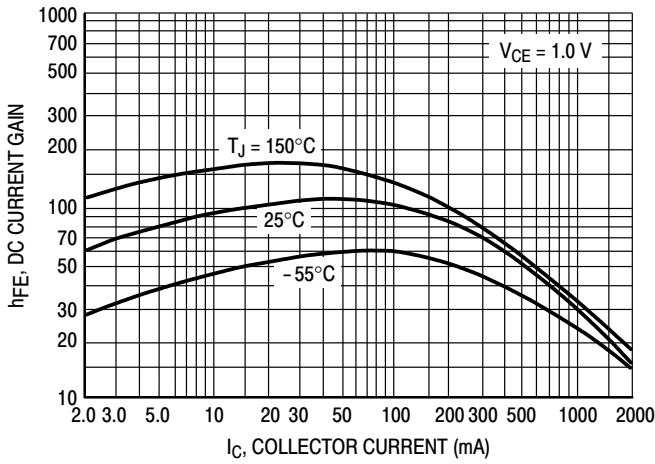


Figure 8. Current Gain

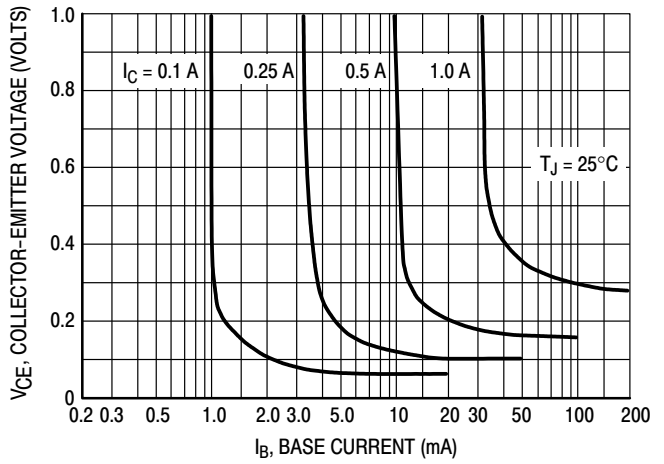


Figure 9. Collector Saturation Region

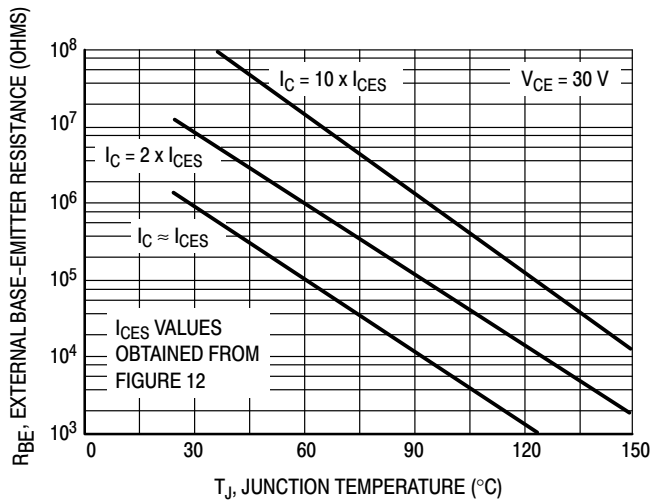


Figure 10. Effects of Base-Emitter Resistance

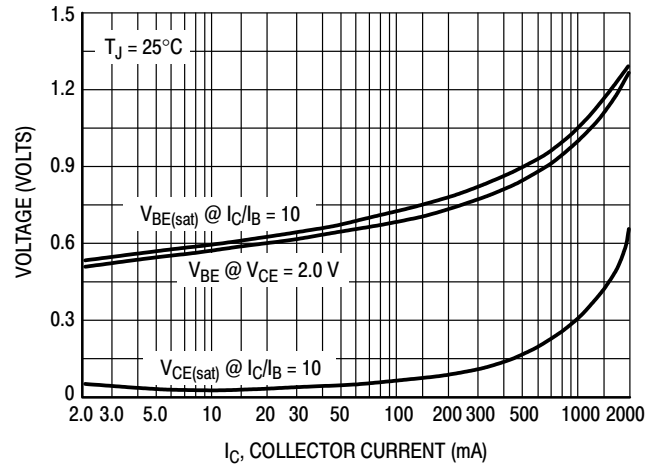


Figure 11. "On" Voltage

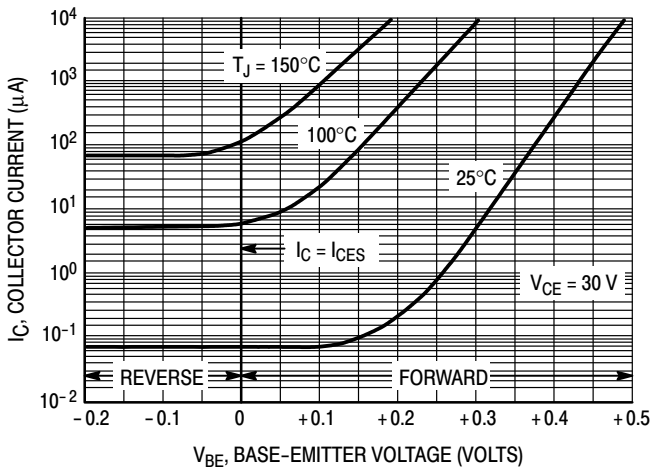


Figure 12. Collector Cut-Off Region

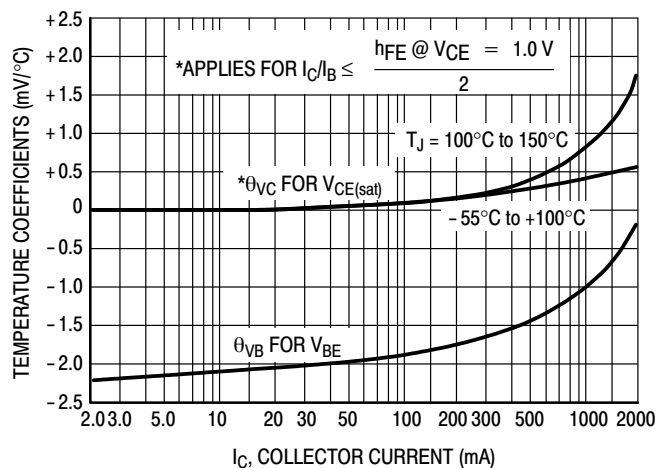
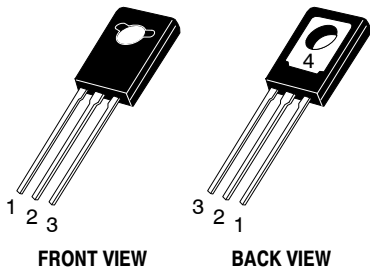


Figure 13. Temperature Coefficients

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

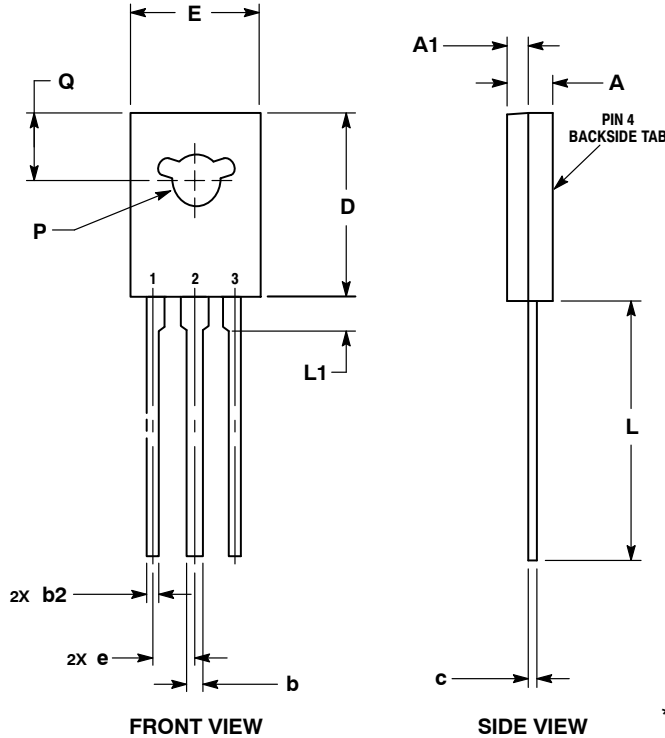
ON Semiconductor®



**TO-225**  
CASE 77-09  
ISSUE AD

DATE 25 MAR 2015

SCALE 1:1

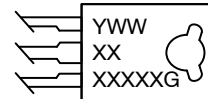


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. NUMBER AND SHAPE OF LUGS OPTIONAL.

DIM	MILLIMETERS	
	MIN	MAX
A	2.40	3.00
A1	1.00	1.50
b	0.60	0.90
b2	0.51	0.88
c	0.39	0.63
D	10.60	11.10
E	7.40	7.80
e	2.04	2.54
L	14.50	16.63
L1	1.27	2.54
P	2.90	3.30
Q	3.80	4.20

**GENERIC MARKING DIAGRAM\***



- Y = Year
- WW = Work Week
- XXXXX = Device Code
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "μ", may or may not be present.

- |   |   |   |   |   |
|---|---|---|---|---|
| <p>STYLE 1:<br/>PIN 1. EMITTER<br/>2., 4. COLLECTOR<br/>3. BASE</p> | <p>STYLE 2:<br/>PIN 1. CATHODE<br/>2., 4. ANODE<br/>3. GATE</p> | <p>STYLE 3:<br/>PIN 1. BASE<br/>2., 4. COLLECTOR<br/>3. EMITTER</p> | <p>STYLE 4:<br/>PIN 1. ANODE 1<br/>2., 4. ANODE 2<br/>3. GATE</p> | <p>STYLE 5:<br/>PIN 1. MT 1<br/>2., 4. MT 2<br/>3. GATE</p>     |
| <p>STYLE 6:<br/>PIN 1. CATHODE<br/>2., 4. GATE<br/>3. ANODE</p>     | <p>STYLE 7:<br/>PIN 1. MT 1<br/>2., 4. GATE<br/>3. MT 2</p>     | <p>STYLE 8:<br/>PIN 1. SOURCE<br/>2., 4. GATE<br/>3. DRAIN</p>      | <p>STYLE 9:<br/>PIN 1. GATE<br/>2., 4. DRAIN<br/>3. SOURCE</p>    | <p>STYLE 10:<br/>PIN 1. SOURCE<br/>2., 4. DRAIN<br/>3. GATE</p> |

<b>DOCUMENT NUMBER:</b>	<b>98ASB42049B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TO-225</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative