

NTMFS4841N

MOSFET – Power, Single, N-Channel, SO-8FL 30 V, 57 A

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These are Pb-Free Devices

Applications

- Refer to Application Note AND8195/D
- CPU Power Delivery
- DC-DC Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

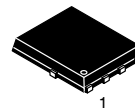
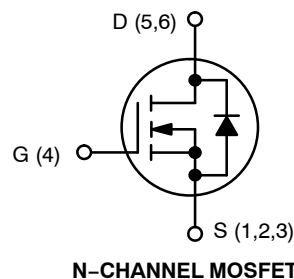
Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	30	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Current R _{θJA} (Note 1) Steady State	Steady State	T _A = 25°C	I _D	13.1	A
		T _A = 85°C		9.5	
		T _A = 25°C	P _D	2.17	W
		T _A = 85°C		1.13	
		T _A = 25°C	I _D	19.9	A
		T _A = 85°C		14.4	
		T _A = 25°C	P _D	5	W
		T _A = 85°C		2.6	
		T _A = 25°C	I _D	8.3	A
		T _A = 85°C		6	
		T _A = 25°C	P _D	0.87	W
		T _A = 85°C		0.45	
		T _C = 25°C	I _D	57	A
		T _C = 85°C		41	
		T _C = 25°C	P _D	41.7	W
		T _C = 85°C		21.7	
Pulsed Drain Current	t _p =10μs	T _A = 25°C	I _{DM}	171	A
Operating Junction and Storage Temperature			T _J , T _{STG}	-55 to +150	°C
Source Current (Body Diode)			I _S	35	A
Drain to Source dV/dt			dV/dt	6	V/ns



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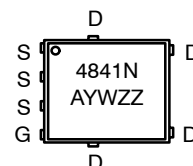
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	7.0 m Ω @ 10 V	57 A
	11.4 m Ω @ 4.5 V	



SO-8 FLAT LEAD
CASE 488AA
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4841NT1G	SO-8FL (Pb-Free)	1500 / Tape & Reel
NTMFS4841NT3G	SO-8FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 24\text{ V}$, $V_{GS} = 10\text{ V}$, $I_L = 19\text{ A}_{pk}$, $L = 1.0\text{ mH}$, $R_G = 25\ \Omega$)	EAS	180	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	3	°C/W
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	57.7	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	143.4	
Junction-to-Ambient – $t = 10$ sec	$R_{\theta JA}$	25	

1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			25		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.5		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.6		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V to } 11.5\text{ V}$	$I_D = 30\text{ A}$	4.7	7.0	m Ω
			$I_D = 15\text{ A}$	4.6		
		$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$	9.2	11.4	
			$I_D = 15\text{ A}$	8.5		
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		16		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 12\text{ V}$		1436		pF
Output Capacitance	C_{OSS}			348		
Reverse Transfer Capacitance	C_{RSS}			177		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		11.5	17	nC
Threshold Gate Charge	$Q_{G(TH)}$			2.0		
Gate-to-Source Charge	Q_{GS}			5.0		
Gate-to-Drain Charge	Q_{GD}			5.1		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		25.4		nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\text{ }\Omega$		13.5		ns
Rise Time	t_r			66.5		
Turn-Off Delay Time	$t_{d(OFF)}$			15.5		
Fall Time	t_f			7.5		

3. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
4. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		8.1		ns
Rise Time	t_r			24.2		
Turn-Off Delay Time	$t_{d(OFF)}$			22.8		
Fall Time	t_f			5.7		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 30\text{ A}$	$T_J = 25^\circ\text{C}$		0.9	1.2	V
			$T_J = 125^\circ\text{C}$		0.8		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 30\text{ A}$			20.5		ns
Charge Time	t_a				11.6		
Discharge Time	t_b				8.9		
Reverse Recovery Charge	Q_{RR}				10.7		nC

PACKAGE PARASITIC VALUES

Source Inductance	L_S	$T_A = 25^\circ\text{C}$		0.93		nH
Drain Inductance	L_D			0.005		
Gate Inductance	L_G			1.84		
Gate Resistance	R_G			3.2		Ω

3. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

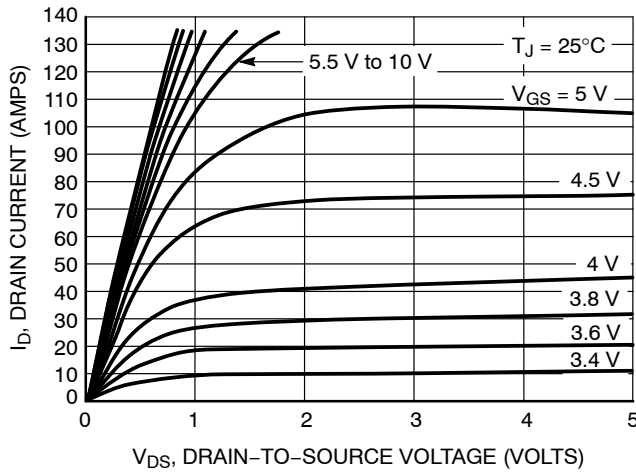


Figure 1. On-Region Characteristics

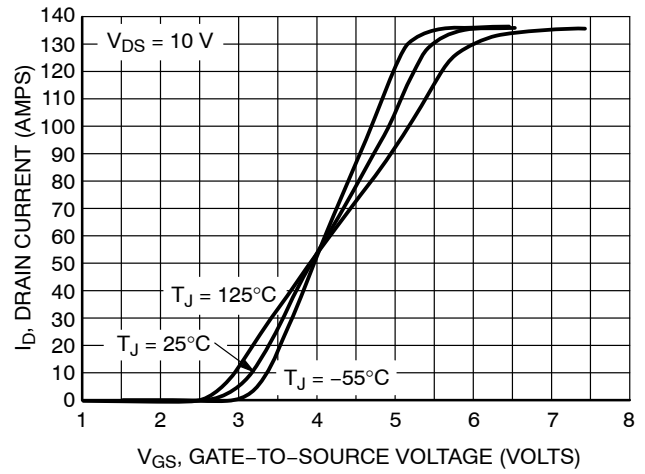


Figure 2. Transfer Characteristics

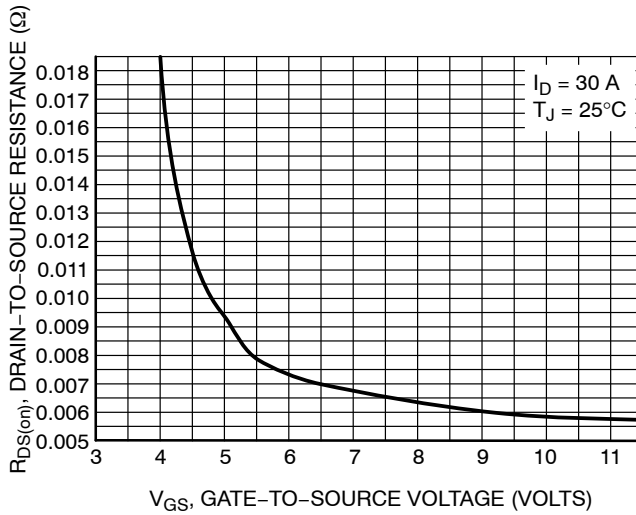


Figure 3. On-Resistance vs. Gate-to-Source Voltage

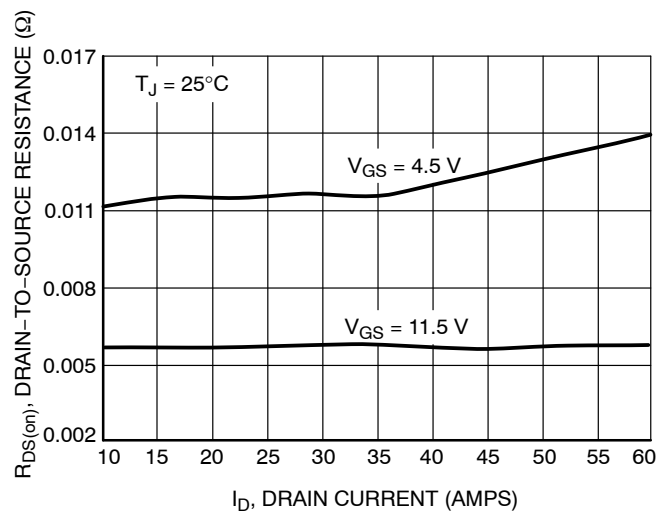


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

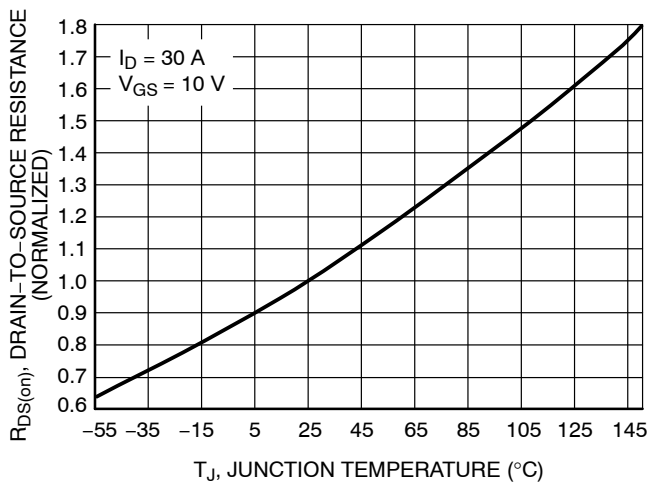


Figure 5. On-Resistance Variation with Temperature

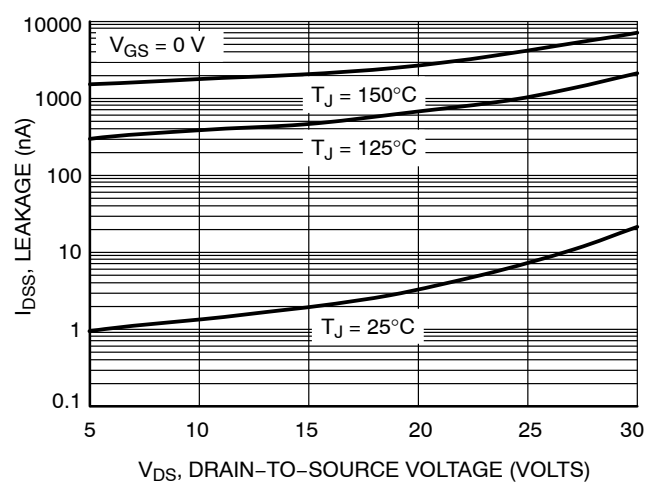
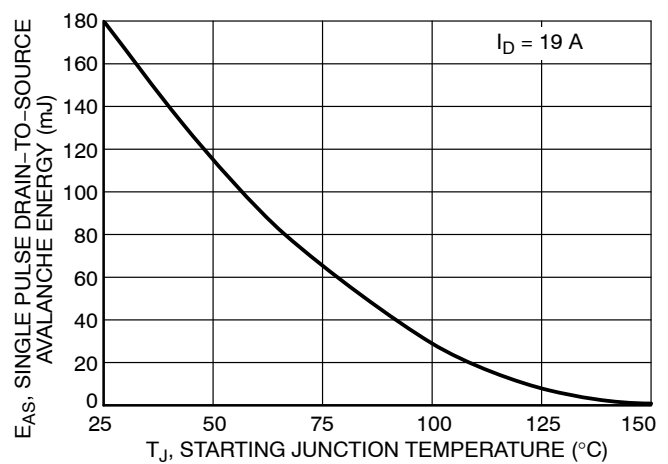
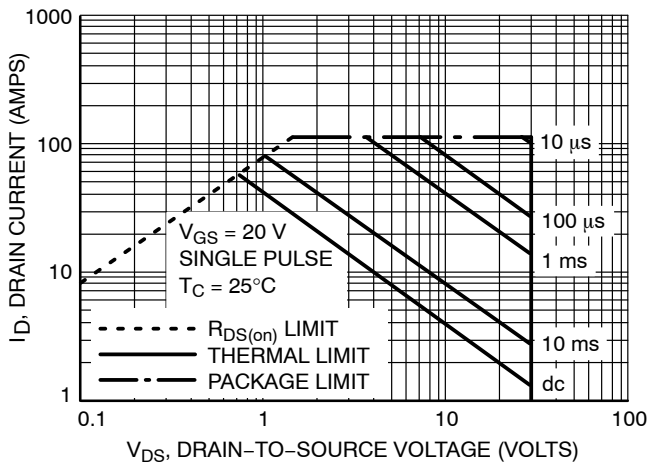
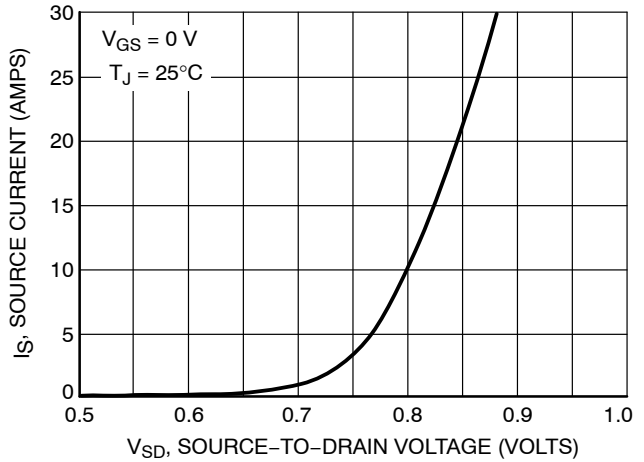
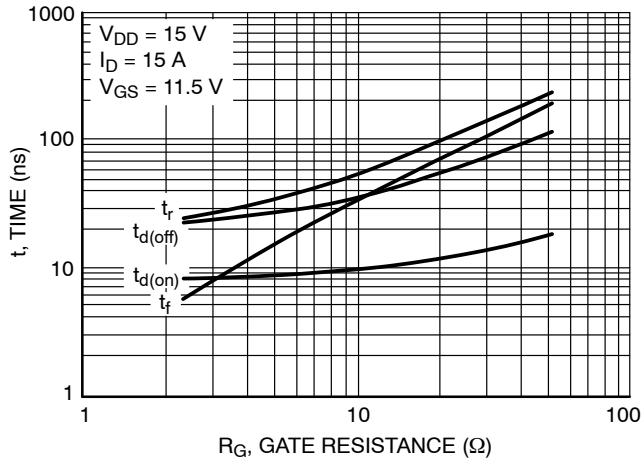
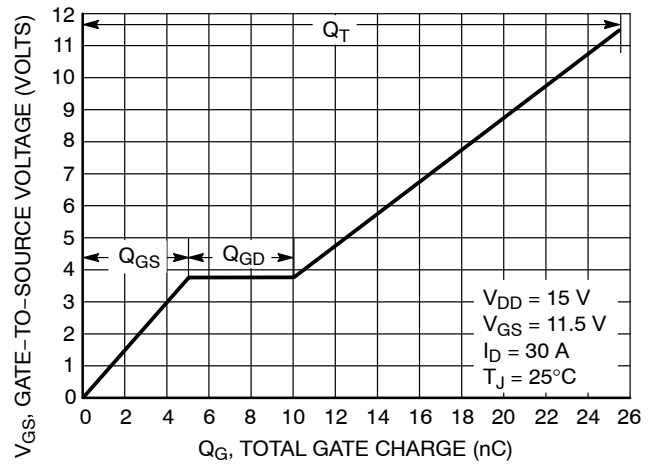
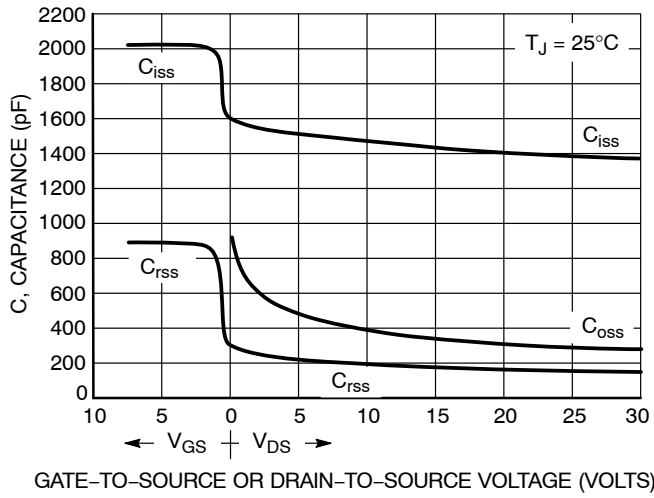


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES



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TYPICAL PERFORMANCE CURVES

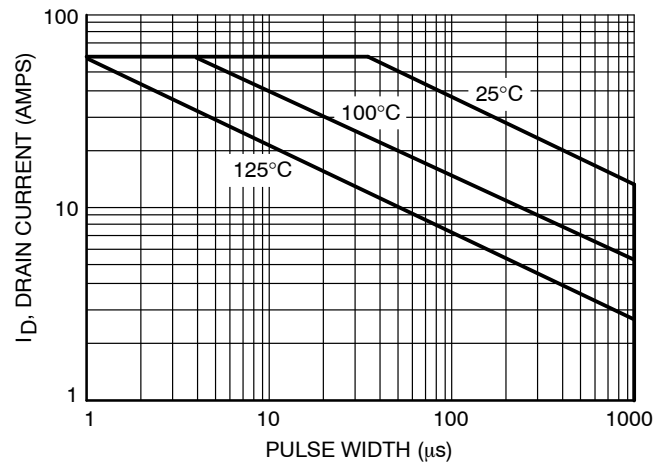


Figure 13. EAS vs. Pulse Width

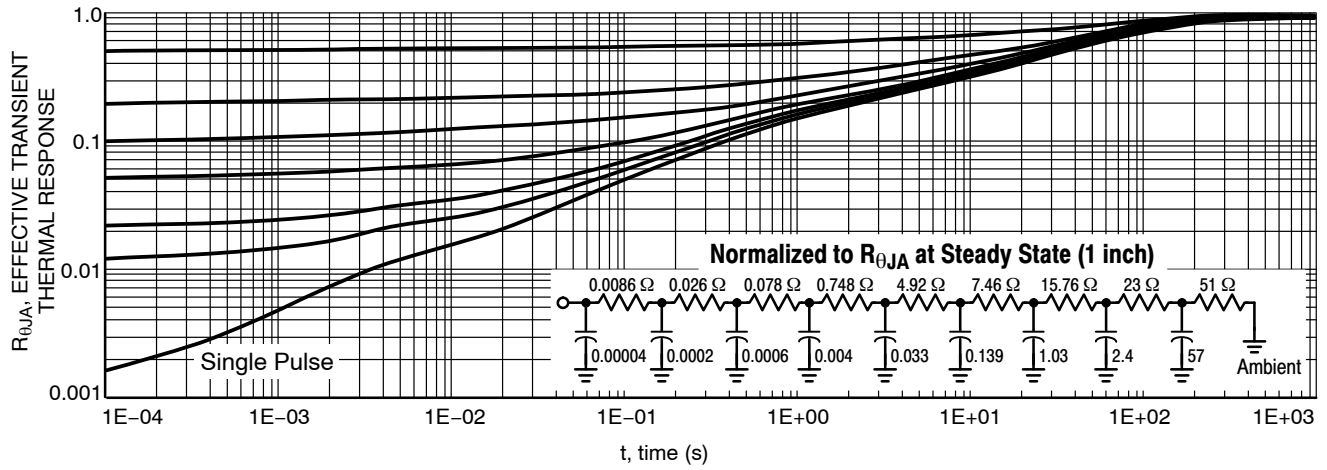
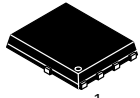


Figure 14. FET Thermal Response

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

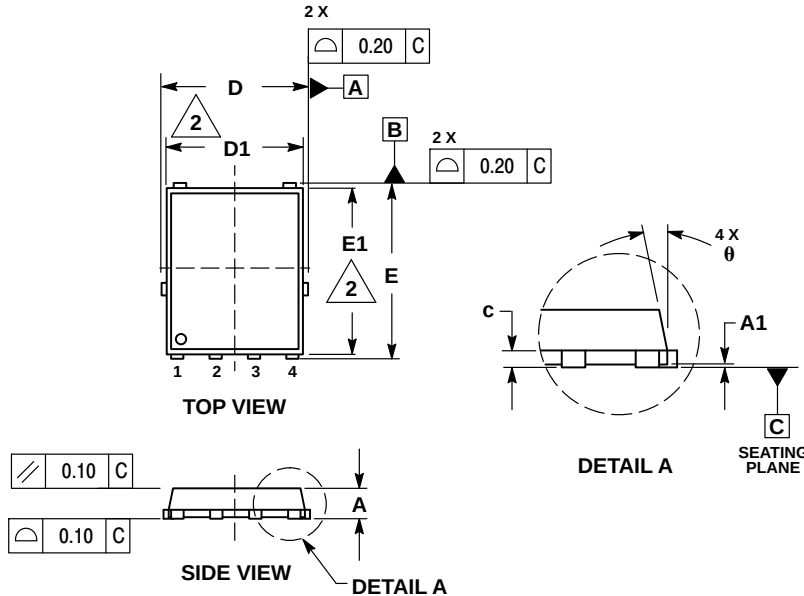
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SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018

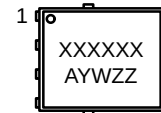


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

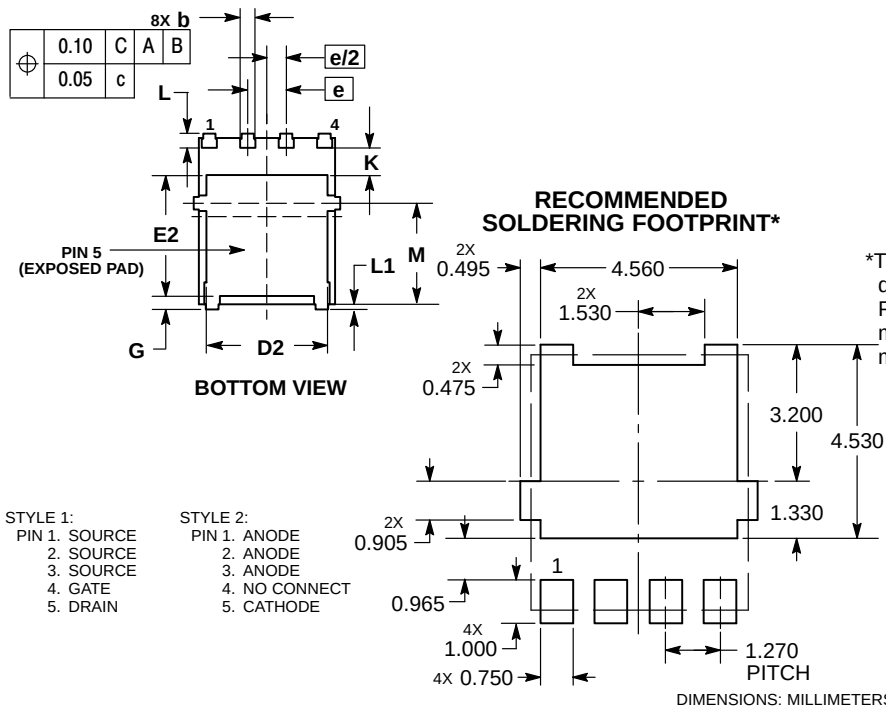
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
theta	0°	---	12°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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