

# NDD01N60, NDT01N60

## N-Channel Power MOSFET 600 V, 8.5 Ω

### Features

- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

| Parameter  | Symbol                            | NDD         | NDT  | Unit |
|--|-----------------------------------|-------------|------|------|
| Drain-to-Source Voltage  | V <sub>DSS</sub>                  | 600         |      | V    |
| Continuous Drain Current R <sub>θJC</sub><br>Steady State, T <sub>C</sub> = 25°C (Note 1)  | I <sub>D</sub>                    | 1.5         | 0.4  | A    |
| Continuous Drain Current R <sub>θJC</sub><br>Steady State, T <sub>C</sub> = 100°C (Note 1) | I <sub>D</sub>                    | 1.0         | 0.25 | A    |
| Pulsed Drain Current, t <sub>p</sub> = 10 μs   | I <sub>DM</sub>                   | 6.0         | 1.5  | A    |
| Power Dissipation – R <sub>θJC</sub><br>Steady State, T <sub>C</sub> = 25°C                | P <sub>D</sub>                    | 46          | 2.5  | W    |
| Gate-to-Source Voltage   | V <sub>GS</sub>                   | ±30         |      | V    |
| Single Pulse Drain-to-Source<br>Avalanche Energy (I <sub>PK</sub> = 1.0 A)                 | EAS                               | 13          |      | mJ   |
| Peak Diode Recovery (Note 2)   | dv/dt                             | 4.5         |      | V/ns |
| Source Current (Body Diode)  | I <sub>S</sub>                    | 1.5         | 0.4  | A    |
| Lead Temperature for Soldering<br>Leads  | T <sub>L</sub>                    | 260         |      | °C   |
| Operating Junction and Storage<br>Temperature  | T <sub>J</sub> , T <sub>STG</sub> | -55 to +150 |      | °C   |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Limited by maximum junction temperature
2. I<sub>S</sub> = 1.5 A, di/dt ≤ 100 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>

### THERMAL RESISTANCE

| Parameter   | Symbol           | Value | Unit |
|---|------------------|-------|------|
| Junction-to-Case (Drain)  | R <sub>θJC</sub> | 2.7   | °C/W |
| Junction-to-Ambient<br>(Note 4) NDD01N60<br>(Note 3) NDD01N60-1<br>(Note 4) NDT01N60<br>(Note 5) NDT01N60 | R <sub>θJA</sub> | 38    | °C/W |
|   |                  | 96    |      |
|   |                  | 58    |      |
|   |                  | 141   |      |

3. Insertion mounted.
4. Surface-mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq. [2 oz] including traces).
5. Surface-mounted on FR4 board using minimum recommended pad size (Cu area = 0.026" sq. [2 oz]).

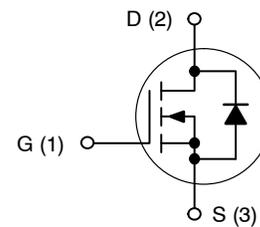


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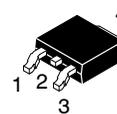
<http://onsemi.com>

| V <sub>(BR)DSS</sub> | R <sub>DS(ON)</sub> MAX |
|----------------------|-------------------------|
| 600 V                | 8.5 Ω @ 10 V            |

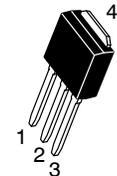
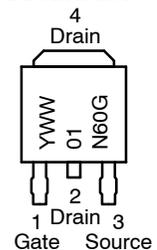
### N-Channel MOSFET



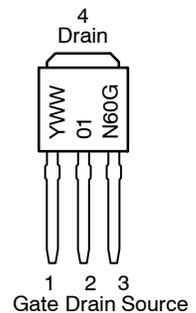
### MARKING DIAGRAMS



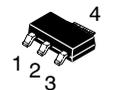
**DPAK  
CASE 369C  
STYLE 2**



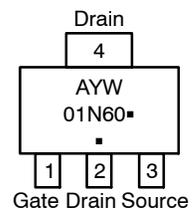
**IPAK  
CASE 369D  
STYLE 2**



Y = Year  
WW = Work Week  
G = Pb-Free Package



**SOT-223  
CASE 318E  
STYLE 3**



A = Assembly Location  
Y = Year  
W = Work Week  
01N60 = Specific Device Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# NDD01N60, NDT01N60

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|----------------|--------|-----------------|-----|-----|-----|------|
|----------------|--------|-----------------|-----|-----|-----|------|

### OFF CHARACTERISTICS

|   |                                      |  |                        |     |      |       |
|---|--------------------------------------|--|------------------------|-----|------|-------|
| Drain-to-Source Breakdown Voltage                         | V <sub>(BR)DSS</sub>                 | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA   | 600                    |     |      | V     |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | V <sub>(BR)DSS</sub> /T <sub>J</sub> | Reference to 25°C, I <sub>D</sub> = 1 mA       |                        | 660 |      | mV/°C |
| Drain-to-Source Leakage Current                           | I <sub>DSS</sub>                     | V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V | T <sub>J</sub> = 25°C  |     | 1    | μA    |
|   |                                      |  | T <sub>J</sub> = 125°C |     | 50   |       |
| Gate-to-Source Leakage Current                            | I <sub>GSS</sub>                     | V <sub>GS</sub> = ±20 V                        |                        |     | ±100 | nA    |

### ON CHARACTERISTICS (Note 6)

|  |                                     |  |     |     |     |       |
|--|-------------------------------------|--|-----|-----|-----|-------|
| Gate Threshold Voltage                     | V <sub>GS(TH)</sub>                 | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 50 μA | 2.2 | 3.3 | 3.7 | V     |
| Negative Threshold Temperature Coefficient | V <sub>GS(TH)</sub> /T <sub>J</sub> |  |     | 7.0 |     | mV/°C |
| Static Drain-to-Source On Resistance       | R <sub>DS(on)</sub>                 | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.2 A             |     | 8.0 | 8.5 | Ω     |
| Forward Transconductance                   | g <sub>FS</sub>                     | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 0.2 A             |     | 0.9 |     | S     |

### CHARGES, CAPACITANCES & GATE RESISTANCES

|                                       |                  |   |  |     |  |    |
|---------------------------------------|------------------|---|--|-----|--|----|
| Input Capacitance (Note 7)            | C <sub>iss</sub> | V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz                |  | 160 |  | pF |
| Output Capacitance (Note 7)           | C <sub>oss</sub> |   |  | 22  |  |    |
| Reverse Transfer Capacitance (Note 7) | C <sub>rss</sub> |   |  | 4.0 |  |    |
| Total Gate Charge (Note 7)            | Q <sub>g</sub>   | V <sub>DS</sub> = 300 V, I <sub>D</sub> = 0.4 A, V <sub>GS</sub> = 10 V |  | 7.2 |  | nC |
| Gate-to-Source Charge (Note 7)        | Q <sub>gs</sub>  |   |  | 1.2 |  |    |
| Gate-to-Drain Charge (Note 7)         | Q <sub>gd</sub>  |   |  | 3.1 |  |    |
| Plateau Voltage                       | V <sub>GP</sub>  |   |  | 4.5 |  |    |
| Gate Resistance                       | R <sub>g</sub>   |   |  | 6.7 |  | Ω  |

### SWITCHING CHARACTERISTICS (Note 8)

|                     |                     |  |  |      |  |    |
|---------------------|---------------------|--|--|------|--|----|
| Turn-on Delay Time  | t <sub>d(on)</sub>  | V <sub>DD</sub> = 300 V, I <sub>D</sub> = 0.4 A,<br>V <sub>GS</sub> = 10 V, R <sub>G</sub> = 0 Ω |  | 8.0  |  | ns |
| Rise Time           | t <sub>r</sub>      |  |  | 5.1  |  |    |
| Turn-off Delay Time | t <sub>d(off)</sub> |  |  | 16.5 |  |    |
| Fall Time           | t <sub>f</sub>      |  |  | 21.3 |  |    |

### DRAIN-SOURCE DIODE CHARACTERISTICS

|                         |                 |  |                        |      |     |    |
|-------------------------|-----------------|--|------------------------|------|-----|----|
| Diode Forward Voltage   | V <sub>SD</sub> | I <sub>S</sub> = 0.4 A, V <sub>GS</sub> = 0 V  | T <sub>J</sub> = 25°C  | 0.78 | 1.6 | V  |
|                         |                 |  | T <sub>J</sub> = 125°C | 0.63 |     |    |
| Reverse Recovery Time   | t <sub>rr</sub> | V <sub>GS</sub> = 0 V, V <sub>DD</sub> = 30 V<br>I <sub>S</sub> = 1.0 A, d <sub>i</sub> /d <sub>t</sub> = 100 A/μs |                        | 179  |     | ns |
| Charge Time             | t <sub>a</sub>  |  |                        | 37   |     |    |
| Discharge Time          | t <sub>b</sub>  |  |                        | 141  |     |    |
| Reverse Recovery Charge | Q <sub>rr</sub> |  |                        | 288  |     |    |

6. Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

7. Guaranteed by design.

8. Switching characteristics are independent of operating junction temperatures.

### ORDERING INFORMATION

| Device      | Package                            | Shipping <sup>†</sup> |
|-------------|------------------------------------|-----------------------|
| NDD01N60-1G | IPAK<br>(Pb-Free, Halogen-Free)    | 75 Units / Rail       |
| NDD01N60T4G | DPAK<br>(Pb-Free, Halogen-Free)    | 2500 / Tape & Reel    |
| NDT01N60T1G | SOT-223<br>(Pb-Free, Halogen-Free) | 1000 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NDD01N60, NDT01N60

## TYPICAL CHARACTERISTICS

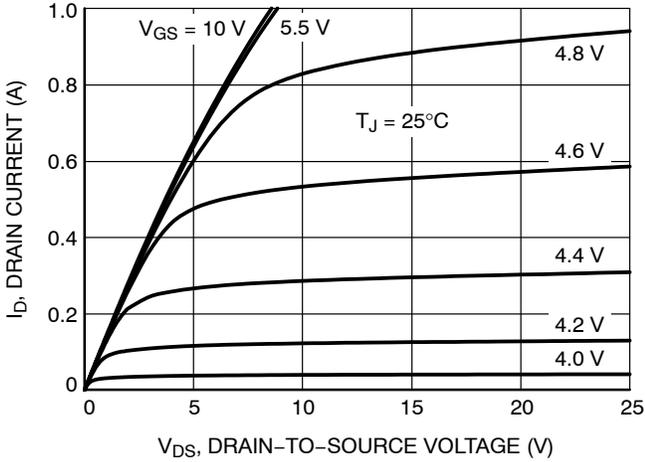


Figure 1. On-Region Characteristics

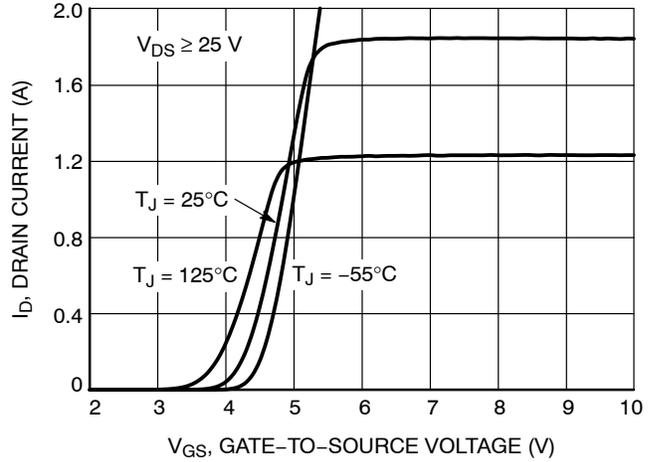


Figure 2. Transfer Characteristics

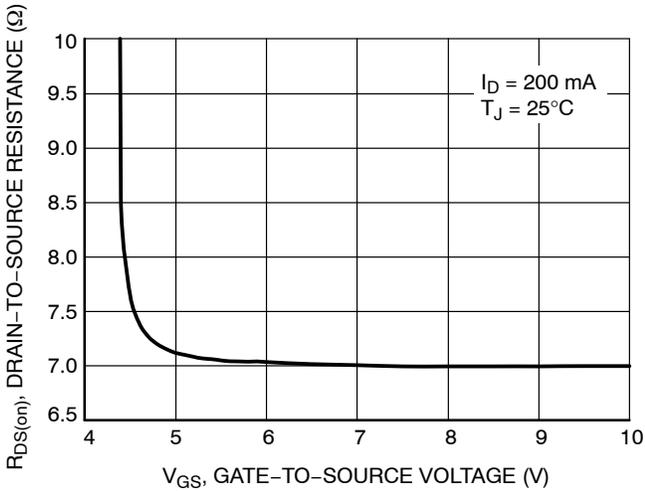


Figure 3. On-Resistance vs. Gate Voltage

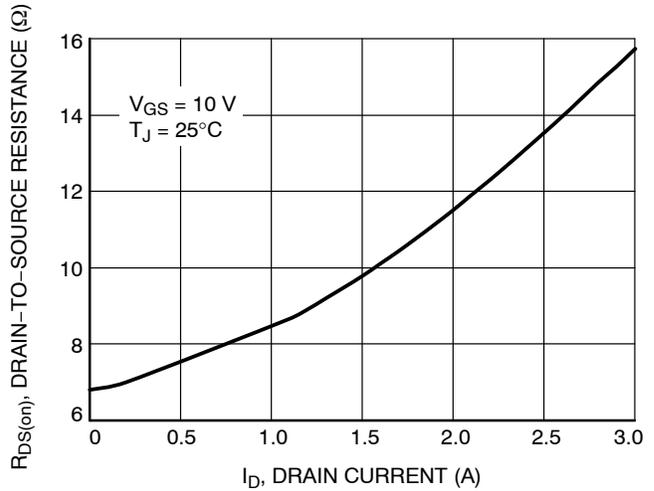


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

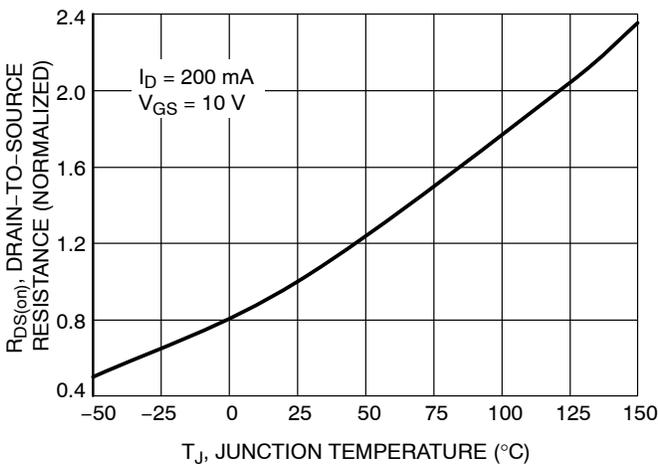


Figure 5. On-Resistance Variation with Temperature

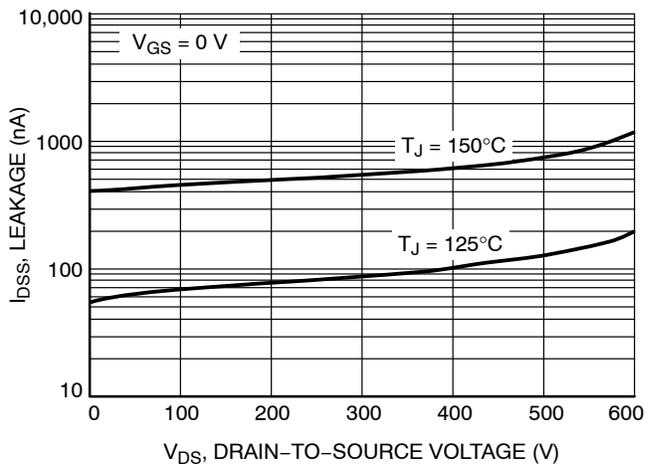


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NDD01N60, NDT01N60

## TYPICAL CHARACTERISTICS

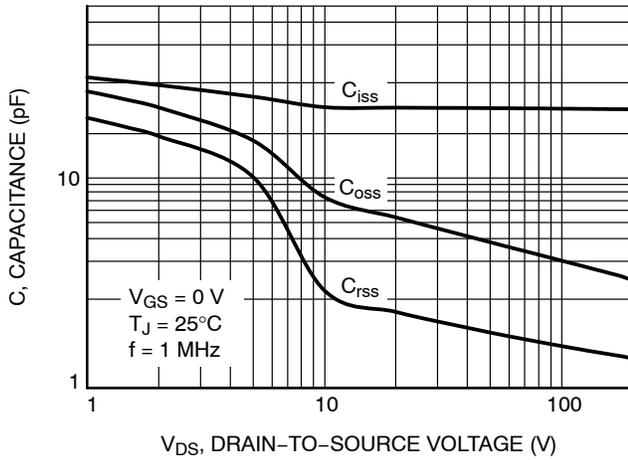


Figure 7. Capacitance Variation

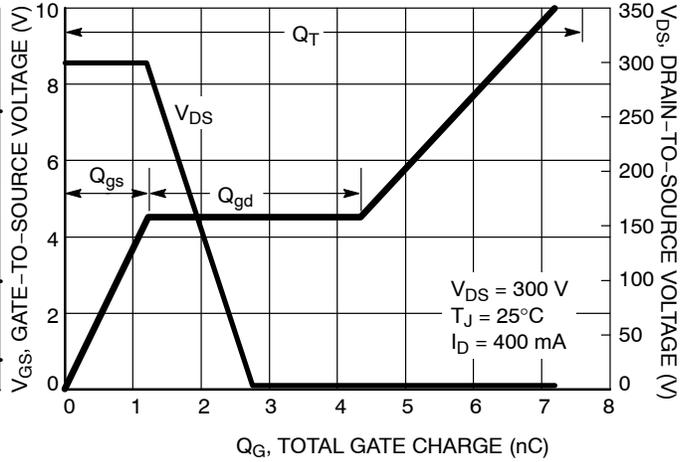


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

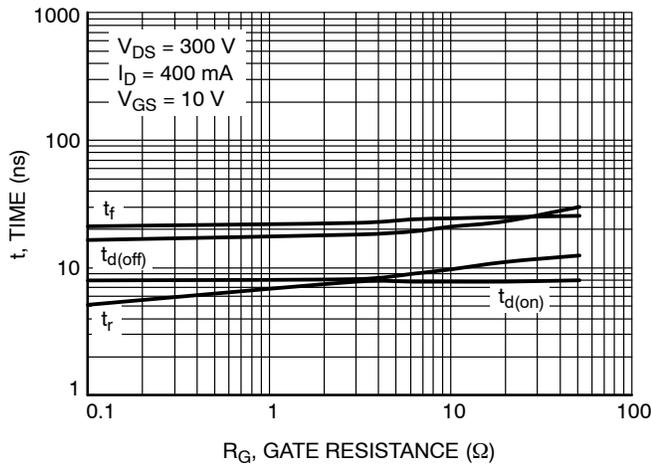


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

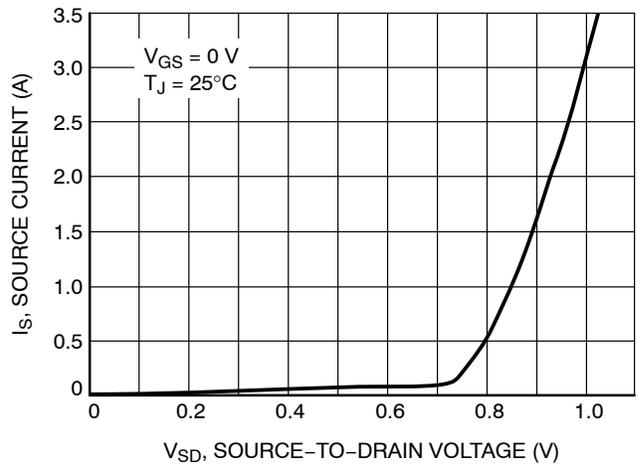


Figure 10. Diode Forward Voltage vs. Current

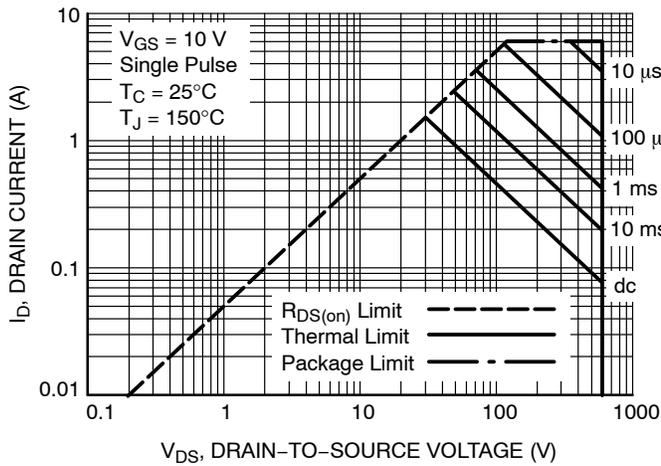


Figure 11. Maximum Rated Forward Biased Safe Operating Area NDD01N60

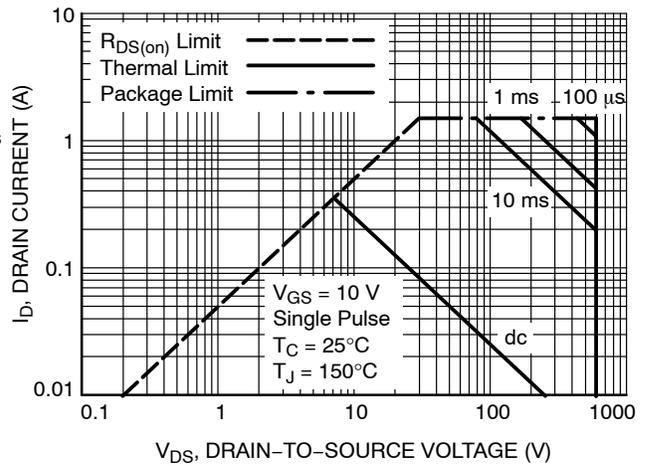


Figure 12. Maximum Rated Forward Biased Safe Operating Area NDT01N60

# NDD01N60, NDT01N60

## TYPICAL CHARACTERISTICS

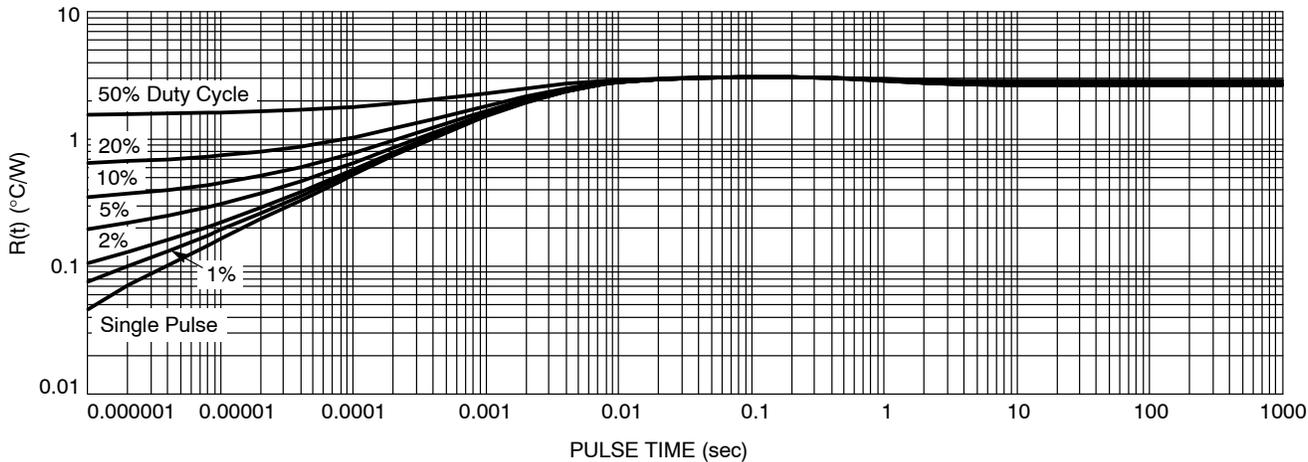


Figure 13. Thermal Impedance (Junction-to-Case) for NDD01N60

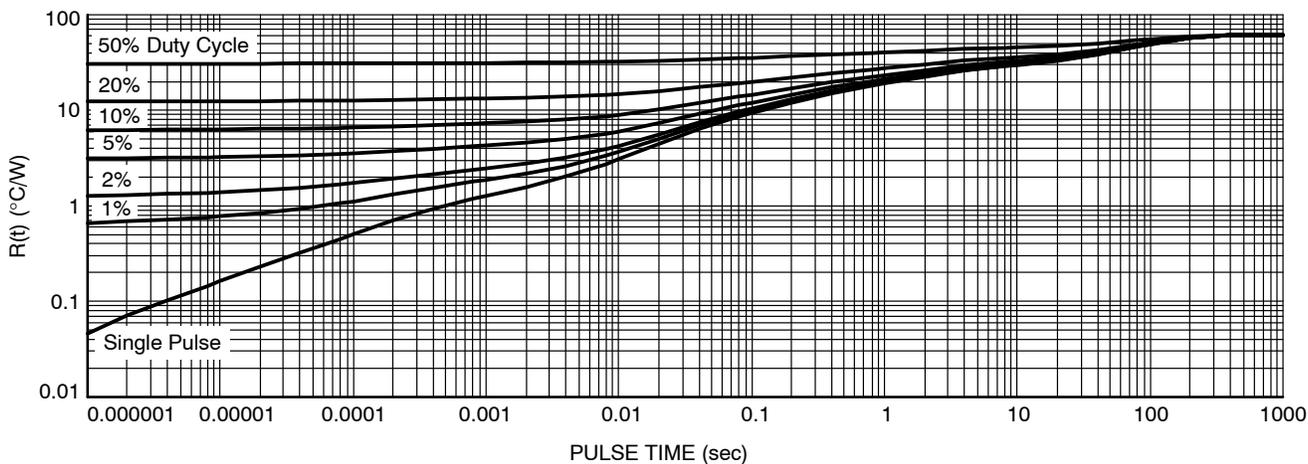


Figure 14. Thermal Impedance (Junction-to-Ambient) for NDT01N60

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

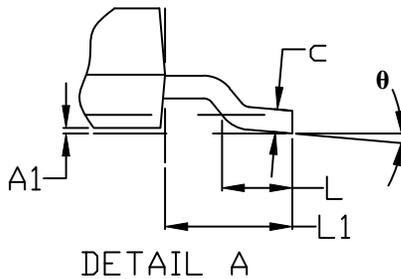
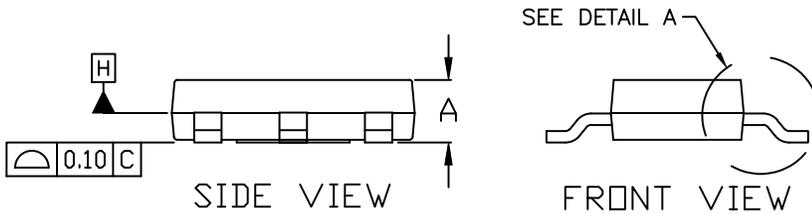
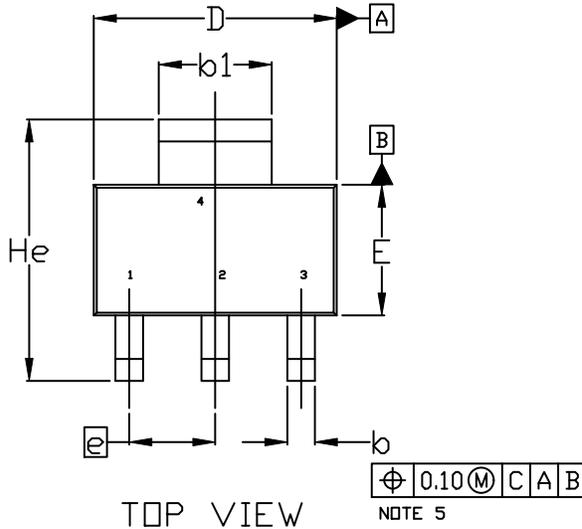
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SCALE 1:1

SOT-223 (TO-261)  
CASE 318E-04  
ISSUE R

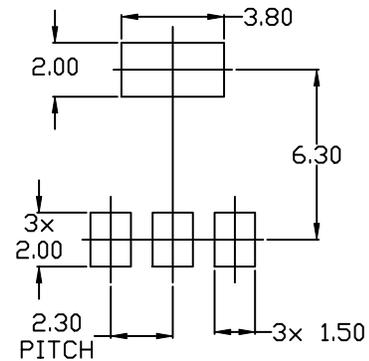
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

| MILLIMETERS |          |      |      |
|-------------|----------|------|------|
| DIM         | MIN.     | NOM. | MAX. |
| A           | 1.50     | 1.63 | 1.75 |
| A1          | 0.02     | 0.06 | 0.10 |
| b           | 0.60     | 0.75 | 0.89 |
| b1          | 2.90     | 3.06 | 3.20 |
| c           | 0.24     | 0.29 | 0.35 |
| D           | 6.30     | 6.50 | 6.70 |
| E           | 3.30     | 3.50 | 3.70 |
| e           | 2.30 BSC |      |      |
| L           | 0.20     | ---  | ---  |
| L1          | 1.50     | 1.75 | 2.00 |
| He          | 6.70     | 7.00 | 7.30 |
| θ           | 0°       | ---  | 10°  |



|                  |                  |  |
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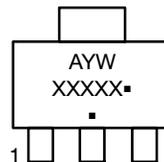
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**SOT-223 (TO-261)**  
**CASE 318E-04**  
**ISSUE R**

DATE 02 OCT 2018

- |  |   |   |   |   |
|--|---|---|---|---|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. NC<br>4. CATHODE        | <b>STYLE 3:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN           | <b>STYLE 4:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE<br>4. DRAIN   | <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. GATE<br>3. SOURCE<br>4. GATE    |
| <b>STYLE 6:</b><br>PIN 1. RETURN<br>2. INPUT<br>3. OUTPUT<br>4. INPUT        | <b>STYLE 7:</b><br>PIN 1. ANODE 1<br>2. CATHODE<br>3. ANODE 2<br>4. CATHODE | <b>STYLE 8:</b><br>CANCELLED  | <b>STYLE 9:</b><br>PIN 1. INPUT<br>2. GROUND<br>3. LOGIC<br>4. GROUND | <b>STYLE 10:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE |
| <b>STYLE 11:</b><br>PIN 1. MT 1<br>2. MT 2<br>3. GATE<br>4. MT 2             | <b>STYLE 12:</b><br>PIN 1. INPUT<br>2. OUTPUT<br>3. NC<br>4. OUTPUT         | <b>STYLE 13:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR |   |   |

**GENERIC  
 MARKING DIAGRAM\***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)  
 \*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                         |                         |  |
|-------------------------|-------------------------|--|
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| <b>DESCRIPTION:</b>     | <b>SOT-223 (TO-261)</b> | <b>PAGE 2 OF 2</b>   |

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

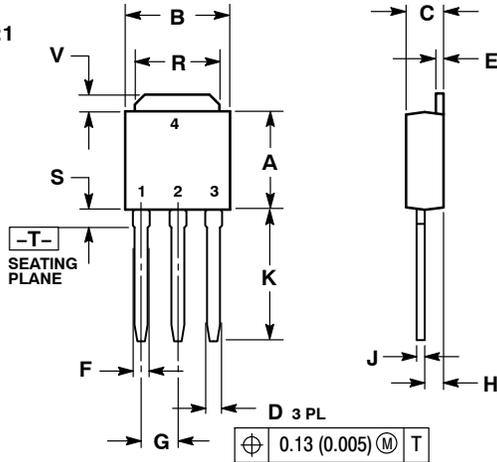
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### IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

SCALE 1:1



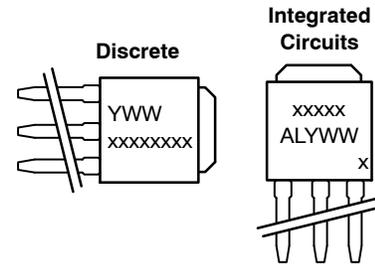
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES |       | MILLIMETERS |      |
|-----|--------|-------|-------------|------|
|     | MIN    | MAX   | MIN         | MAX  |
| A   | 0.235  | 0.245 | 5.97        | 6.35 |
| B   | 0.250  | 0.265 | 6.35        | 6.73 |
| C   | 0.086  | 0.094 | 2.19        | 2.38 |
| D   | 0.027  | 0.035 | 0.69        | 0.88 |
| E   | 0.018  | 0.023 | 0.46        | 0.58 |
| F   | 0.037  | 0.045 | 0.94        | 1.14 |
| G   | 0.090  | BSC   | 2.29        | BSC  |
| H   | 0.034  | 0.040 | 0.87        | 1.01 |
| J   | 0.018  | 0.023 | 0.46        | 0.58 |
| K   | 0.350  | 0.380 | 8.89        | 9.65 |
| R   | 0.180  | 0.215 | 4.45        | 5.45 |
| S   | 0.025  | 0.040 | 0.63        | 1.01 |
| V   | 0.035  | 0.050 | 0.89        | 1.27 |
| Z   | 0.155  | ---   | 3.93        | ---  |

- |  |   |  |  |
|--|---|--|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p> | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>      | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p> |
| <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>         | <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>        | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> |  |

### MARKING DIAGRAMS



- xxxxxxxx = Device Code
- A = Assembly Location
- IL = Wafer Lot
- Y = Year
- WW = Work Week

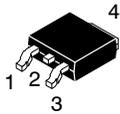
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|-------------------------|------------------------------------|--|
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| <b>DESCRIPTION:</b>     | <b>IPAK (DPAK INSERTION MOUNT)</b> | <b>PAGE 1 OF 1</b>   |

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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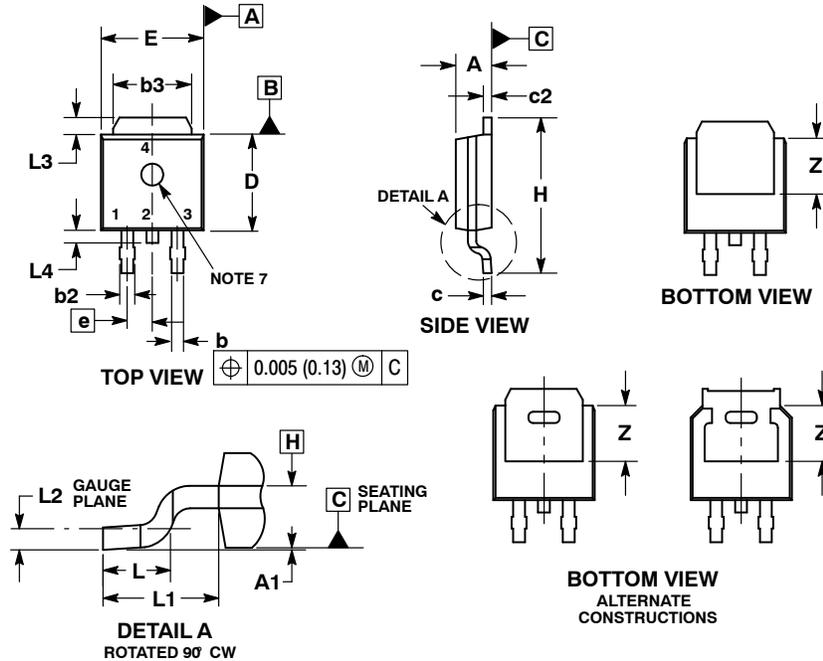
SCALE 1:1

### DPAK (SINGLE GAUGE)

#### CASE 369C

#### ISSUE F

DATE 21 JUL 2015

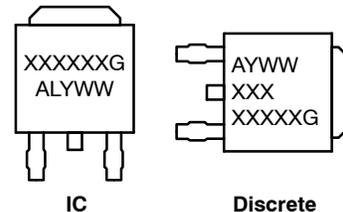


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.086     | 0.094 | 2.18        | 2.38  |
| A1  | 0.000     | 0.005 | 0.00        | 0.13  |
| b   | 0.025     | 0.035 | 0.63        | 0.89  |
| b2  | 0.028     | 0.045 | 0.72        | 1.14  |
| b3  | 0.180     | 0.215 | 4.57        | 5.46  |
| c   | 0.018     | 0.024 | 0.46        | 0.61  |
| c2  | 0.018     | 0.024 | 0.46        | 0.61  |
| D   | 0.235     | 0.245 | 5.97        | 6.22  |
| E   | 0.250     | 0.265 | 6.35        | 6.73  |
| e   | 0.090 BSC |       | 2.29 BSC    |       |
| H   | 0.370     | 0.410 | 9.40        | 10.41 |
| L   | 0.055     | 0.070 | 1.40        | 1.78  |
| L1  | 0.114 REF |       | 2.90 REF    |       |
| L2  | 0.020 BSC |       | 0.51 BSC    |       |
| L3  | 0.035     | 0.050 | 0.89        | 1.27  |
| L4  | ---       | 0.040 | ---         | 1.01  |
| Z   | 0.155     | ---   | 3.93        | ---   |

### GENERIC MARKING DIAGRAM\*

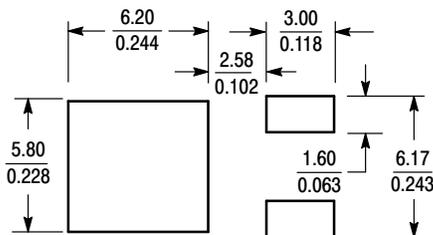


- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

- |  |  |   |   |  |
|--|--|---|---|--|
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| <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>                 | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 8:<br/>PIN 1. N/C<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>   | <p>STYLE 9:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. RESISTOR ADJUST<br/>4. CATHODE</p> | <p>STYLE 10:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p> |

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm / inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                  |                     |  |
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| DESCRIPTION:     | DPAK (SINGLE GAUGE) | PAGE 1 OF 1  |

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