

NTMFS4943N

Power MOSFET

30 V, 41 A, Single N-Channel, SO-8 FL

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- CPU Power Delivery
- DC-DC Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	30	V	
Gate-to-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	14	A
		$T_A = 100^{\circ}\text{C}$		8.7	
$T_A = 25^{\circ}\text{C}$		P_D	2.6	W	
Continuous Drain Current $R_{\theta JA} \leq 10\text{ s}$ (Note 1)		$T_A = 25^{\circ}\text{C}$	I_D	23	A
		$T_A = 100^{\circ}\text{C}$		14.3	
Power Dissipation $R_{\theta JA} \leq 10\text{ s}$ (Note 1)		$T_A = 25^{\circ}\text{C}$	P_D	6.83	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)		$T_A = 25^{\circ}\text{C}$	I_D	8.3	A
		$T_A = 100^{\circ}\text{C}$		5.2	
Power Dissipation $R_{\theta JA}$ (Note 2)		$T_A = 25^{\circ}\text{C}$	P_D	0.91	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)		$T_C = 25^{\circ}\text{C}$	I_D	41	A
	$T_C = 85^{\circ}\text{C}$	26			
Power Dissipation $R_{\theta JC}$ (Note 1)	$T_C = 25^{\circ}\text{C}$	P_D	22.3	W	
Pulsed Drain Current	$T_A = 25^{\circ}\text{C}$, $t_p = 10\text{ }\mu\text{s}$		I_{DM}	125	A
Current Limited by Package	$T_A = 25^{\circ}\text{C}$		I_{Dmax}	100	A
Operating Junction and Storage Temperature		T_J , T_{STG}	-55 to +150	$^{\circ}\text{C}$	
Source Current (Body Diode)		I_S	20	A	
Drain to Source DV/DT		dV/dt	8.0	V/ns	
Single Pulse Drain-to-Source Avalanche Energy $T_J = 25^{\circ}\text{C}$, $V_{DD} = 30\text{ V}$, $V_{GS} = 10\text{ V}$, $I_L = 25\text{ A}_{pk}$, $L = 0.1\text{ mH}$, $R_G = 25\text{ }\Omega$		E_{AS}	31	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^{\circ}\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

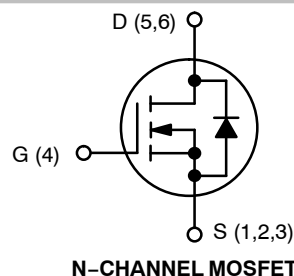
1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.



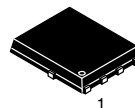
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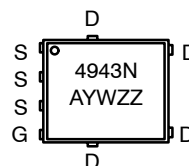
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	7.2 m Ω @ 10 V	41 A
	11 m Ω @ 4.5 V	



MARKING DIAGRAM



SO-8 FLAT LEAD
CASE 488AA
STYLE 1



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4943NT1G	SO-8 FL (Pb-Free)	1500 / Tape & Reel
NTMFS4943NT3G	SO-8 FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	5.6	°C/W
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	49.1	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	137.2	
Junction-to-Ambient – ($t \leq 10$ s) (Note 3)	$R_{\theta JA}$	18.3	

3. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.

4. Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage (transient)	$V_{(BR)DSS(t)}$	$V_{GS} = 0\text{ V}, I_{D(aval)} = 10.5\text{ A}, T_{case} = 25^\circ\text{C}, t_{transient} = 100\text{ ns}$	34			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			15		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.2	1.66	2.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 30\text{ A}$	5.8	7.2	m Ω
			$I_D = 15\text{ A}$	5.8		
		$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$	8.2	11	
			$I_D = 15\text{ A}$	8.2		
Forward Transconductance	g_{FS}	$V_{DS} = 1.5\text{ V}, I_D = 15\text{ A}$		32		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$		1401		pF
Output Capacitance	C_{OSS}			446		
Reverse Transfer Capacitance	C_{RSS}			16		
Capacitance Ratio	C_{RSS}/C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$		0.011	0.023	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		9.2		nC
Threshold Gate Charge	$Q_{G(TH)}$			2.7		
Gate-to-Source Charge	Q_{GS}			4.4		
Gate-to-Drain Charge	Q_{GD}			1.9		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		20.9		nC

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\text{ }\Omega$		11		ns
Rise Time	t_r			31		
Turn-Off Delay Time	$t_{d(OFF)}$			18		
Fall Time	t_f			3.0		

5. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		8.0		ns
Rise Time	t_r			21		
Turn-Off Delay Time	$t_{d(OFF)}$			21		
Fall Time	t_f			2.1		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 30 A	T _J = 25°C		0.9	1.1	V
			T _J = 125°C		0.8		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 30 A			23		ns
Charge Time	t _a				12.5		
Discharge Time	t _b				10.5		
Reverse Recovery Charge	Q _{RR}				10		nC

PACKAGE PARASITIC VALUES

Source Inductance	L_S	$T_A = 25^\circ\text{C}$		0.93		nH
Drain Inductance	L_D			0.005		nH
Gate Inductance	L_G			1.84		nH
Gate Resistance	R_G			1.1	2.0	Ω

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

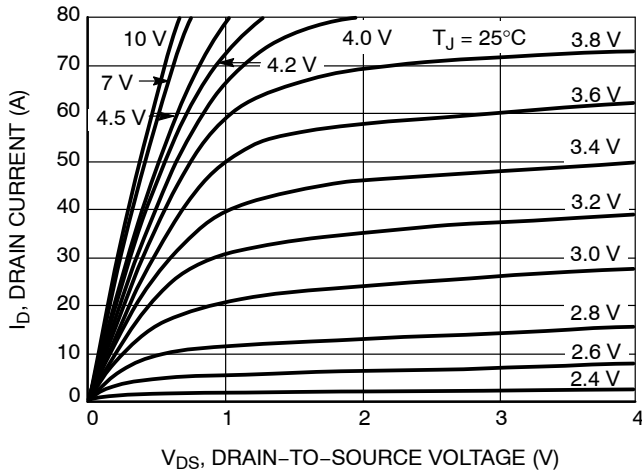


Figure 1. On-Region Characteristics

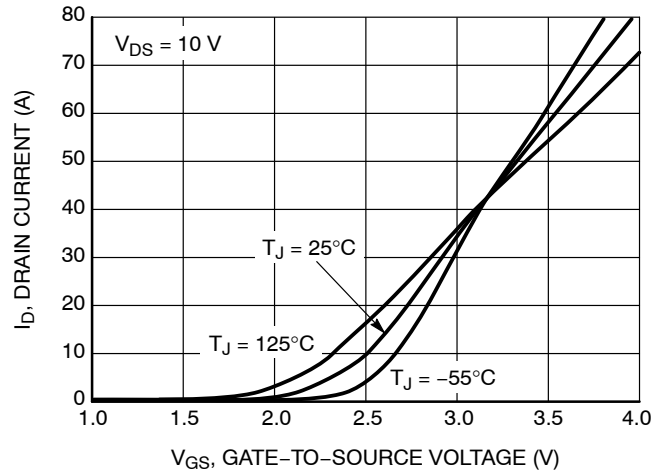


Figure 2. Transfer Characteristics

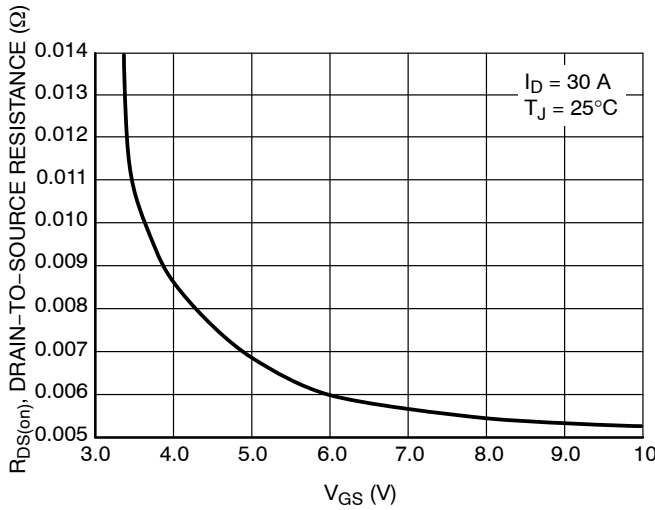


Figure 3. On-Resistance vs. V_{GS}

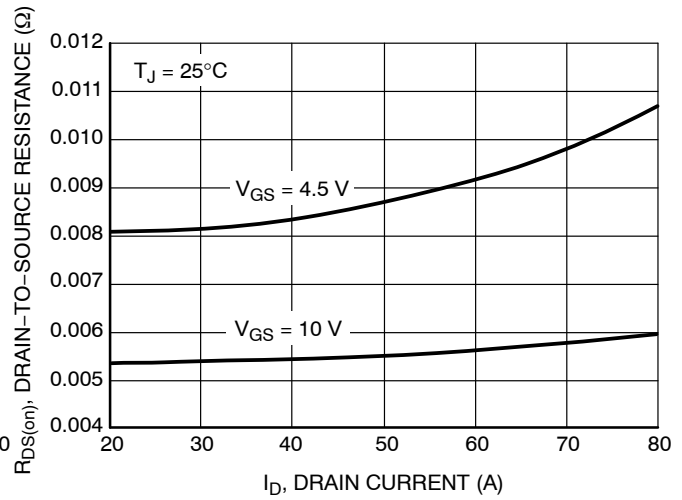


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

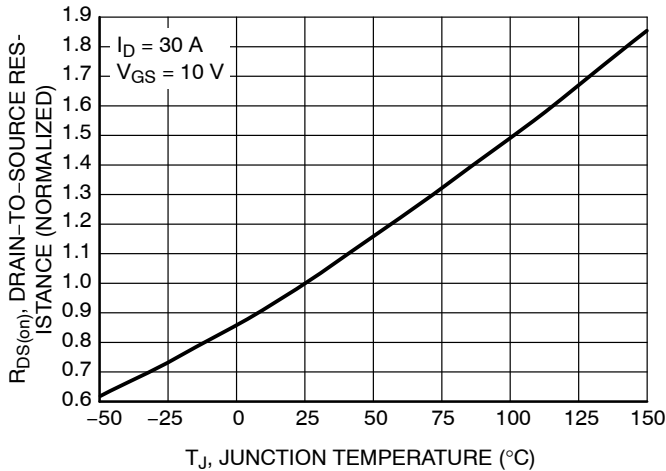


Figure 5. On-Resistance Variation with Temperature

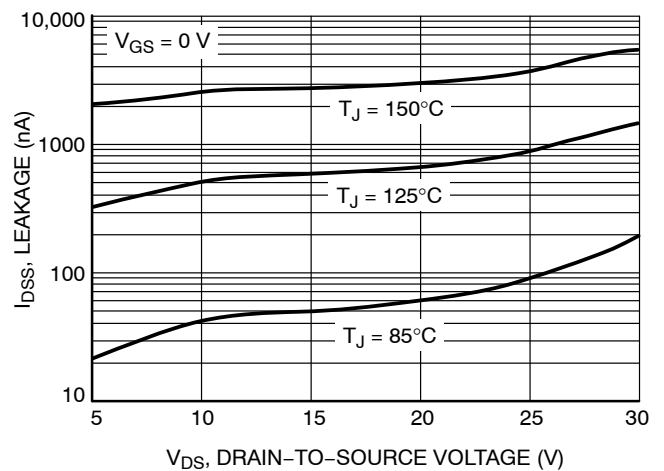


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

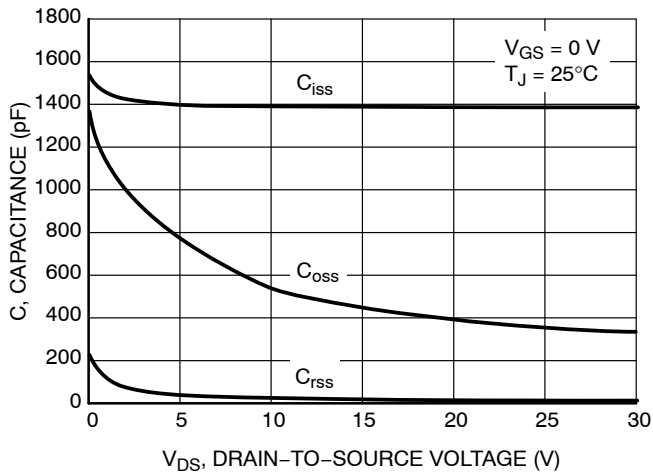


Figure 7. Capacitance Variation

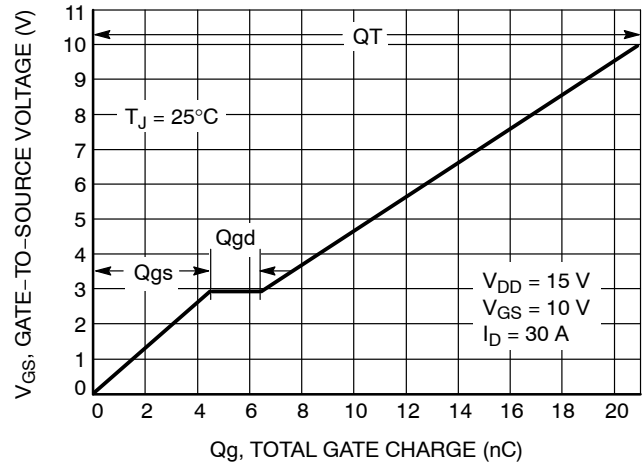


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

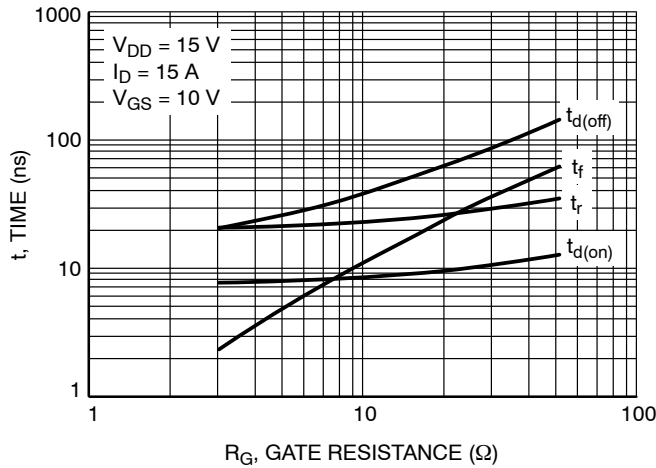


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

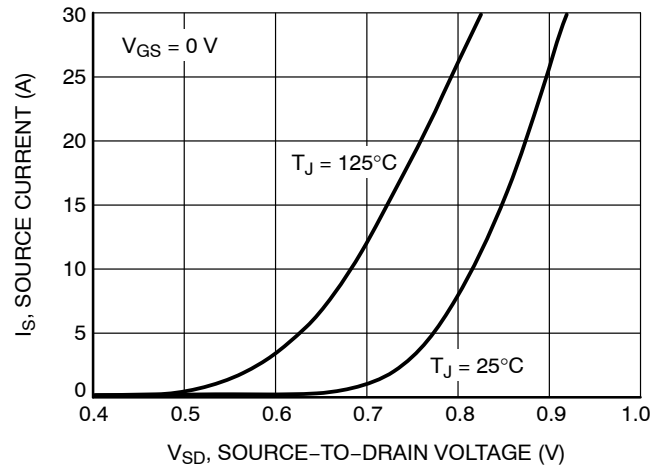


Figure 10. Diode Forward Voltage vs. Current

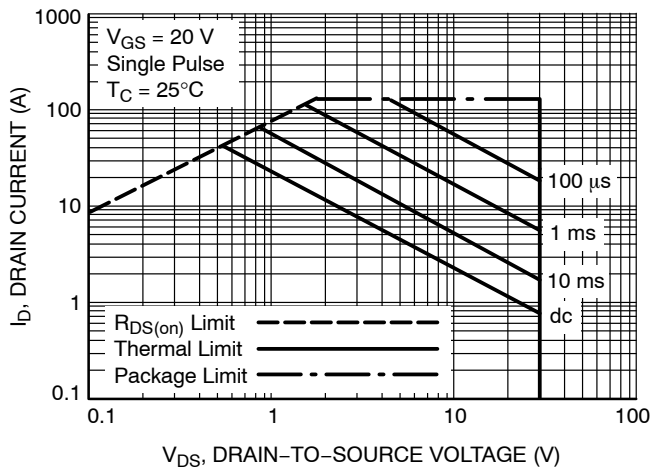


Figure 11. Maximum Rated Forward Biased Safe Operating Area

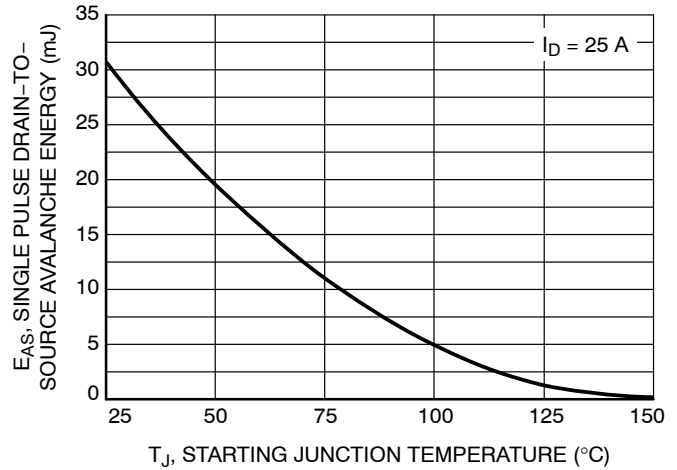


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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TYPICAL CHARACTERISTICS

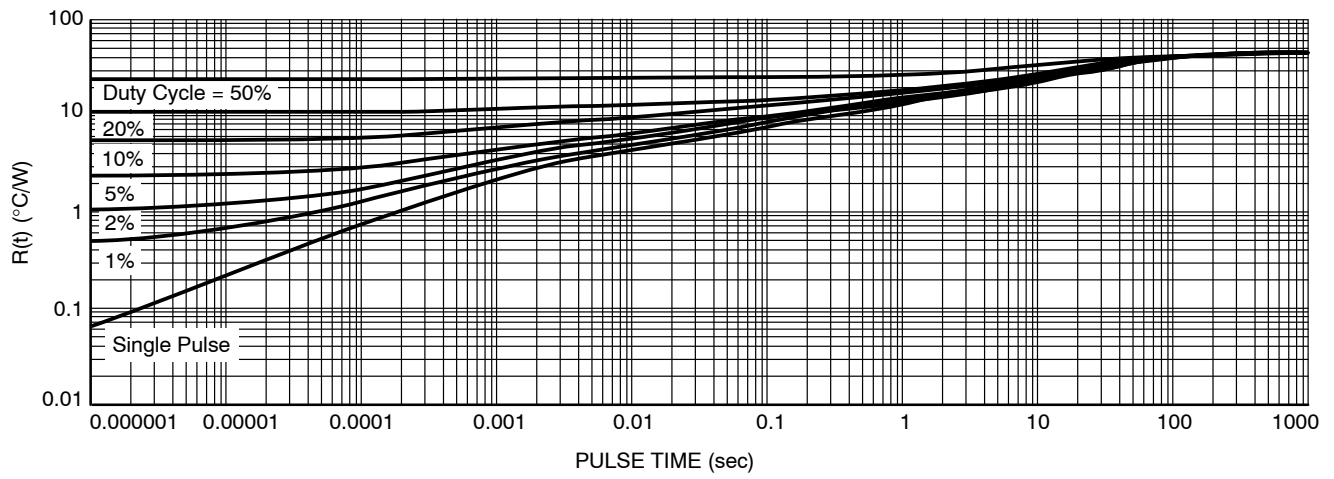


Figure 13. Thermal Response

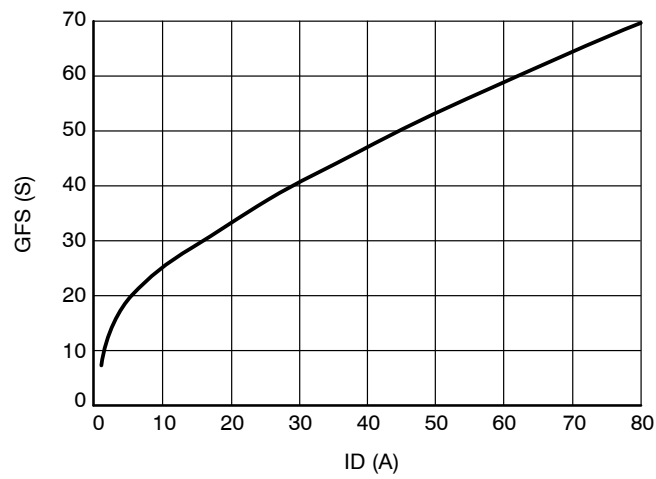
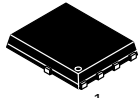


Figure 14. GFS vs. ID

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

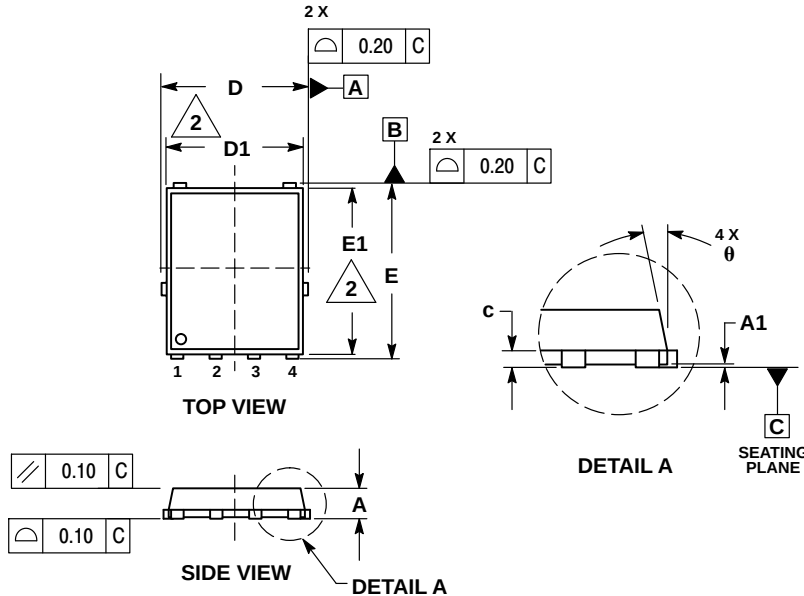
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SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018

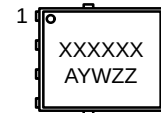


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

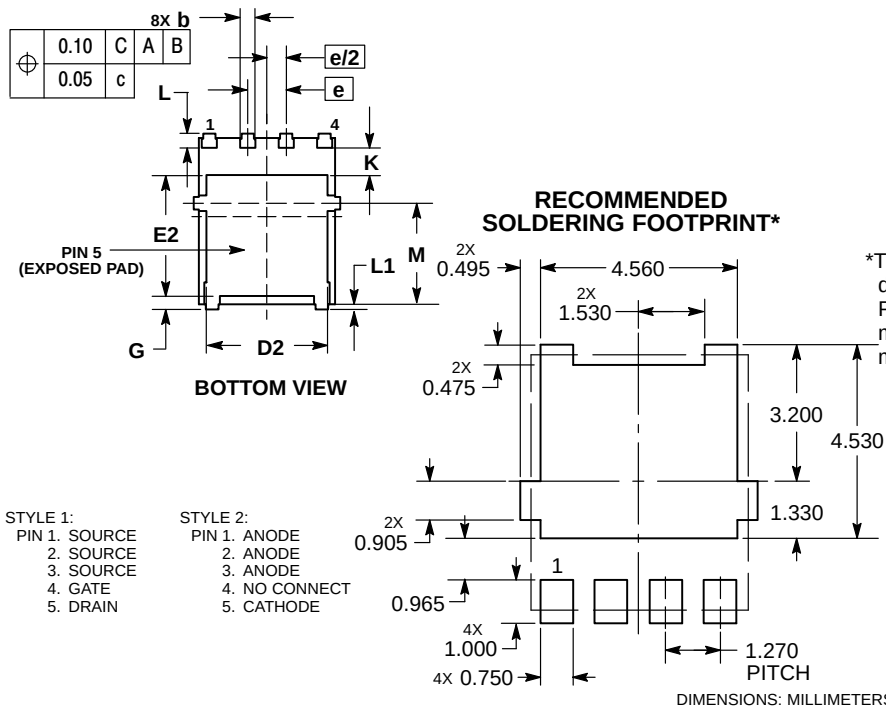
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
theta	0 °	---	12 °

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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