

NDF08N50Z

N-Channel Power MOSFET 500 V, 0.85 Ω

Features

- Low ON Resistance
- Low Gate Charge
- ESD Diode–Protected Gate
- 100% Avalanche Tested
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	NDF08N50Z	Unit
Drain–to–Source Voltage	V_{DS}	500	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	I_D	8.5	A
Continuous Drain Current $R_{\theta JC}$ $T_A = 100^\circ\text{C}$ (Note 1)	I_D	5.4	A
Pulsed Drain Current, $V_{GS} @ 10\text{ V}$	I_{DM}	34	A
Power Dissipation	P_D	35	W
Gate–to–Source Voltage	V_{GS}	± 30	V
Single Pulse Avalanche Energy, $I_D = 7.5\text{ A}$	E_{AS}	190	mJ
ESD (HBM) (JESD 22–A114)	V_{esd}	3500	V
RMS Isolation Voltage ($t = 0.3\text{ sec.}$, R.H. $\leq 30\%$, $T_A = 25^\circ\text{C}$) (Figure 14)	V_{ISO}	4500	V
Peak Diode Recovery (Note 2)	dV/dt	4.5	V/ns
MOSFET dV/dt	dV/dt	60	V/ns
Continuous Source Current (Body Diode)	I_S	7.5	A
Maximum Temperature for Soldering Leads	T_L	260	$^\circ\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

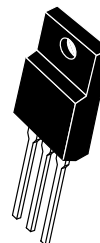
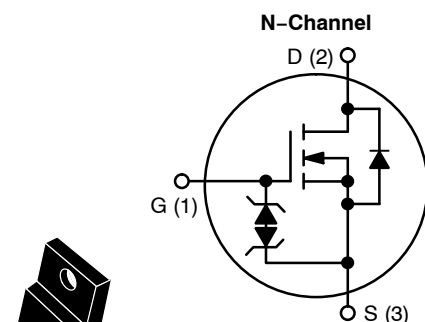
1. Limited by maximum junction temperature
2. $I_{SD} = 7.5\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, $T_J = +150^\circ\text{C}$



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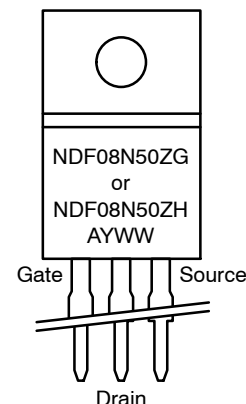
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V_{DSS}	$R_{DS(ON)} (MAX) @ 3.6\text{ A}$
500 V	0.85 Ω



NDF08N50ZG,
NDF08N50ZH
TO–220FP
CASE 221AH

MARKING DIAGRAM



A = Location Code
Y = Year
WW = Work Week
G, H = Pb–Free, Halogen–Free Package

ORDERING INFORMATION

Device	Package	Shipping
NDF08N50ZG	TO–220FP (Pb–Free, Halogen–Free)	50 Units / Rail
NDF08N50ZH	TO–220FP (Pb–Free, Halogen–Free)	50 Units / Rail

NDF08N50Z

THERMAL RESISTANCE

Parameter	Symbol	NDF08N50Z	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	3.6	°C/W
Junction-to-Ambient Steady State (Note 3)	$R_{\theta JA}$	50	

3. Insertion mounted

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	BV_{DSS}	500			V
Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_D = 1\text{ mA}$	$\Delta BV_{DSS} / \Delta T_J$		0.6		V/°C
Drain-to-Source Leakage Current	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	I_{DSS}			1	μA
					50	
Gate-to-Source Forward Leakage	$V_{GS} = \pm 20\text{ V}$	I_{GSS}			± 10	μA

ON CHARACTERISTICS (Note 4)

Static Drain-to-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 3.6\text{ A}$	$R_{DS(on)}$		0.69	0.85	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	$V_{GS(th)}$	3.0	3.9	4.5	V
Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 3.75\text{ A}$	g_{FS}		6.0		S

DYNAMIC CHARACTERISTICS

Input Capacitance (Note 5)	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	C_{iss}	730	912	1095	pF
Output Capacitance (Note 5)		C_{oss}	95	120	140	
Reverse Transfer Capacitance (Note 5)		C_{rss}	15	27	35	
Total Gate Charge (Note 5)	$V_{DD} = 250\text{ V}, I_D = 7.5\text{ A},$ $V_{GS} = 10\text{ V}$	Q_g	16	31	46	nC
Gate-to-Source Charge (Note 5)		Q_{gs}	3	6.2	9	
Gate-to-Drain ("Miller") Charge (Note 5)		Q_{gd}	8	17	25	
Plateau Voltage		V_{GP}		6.3		V
Gate Resistance		R_g		3.0		Ω

RESISTIVE SWITCHING CHARACTERISTICS

Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 7.5\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 5\text{ }\Omega$	$t_{d(on)}$		13		ns
Rise Time		t_r		23		
Turn-Off Delay Time		$t_{d(off)}$		31		
Fall Time		t_f		29		

SOURCE-DRAIN DIODE CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

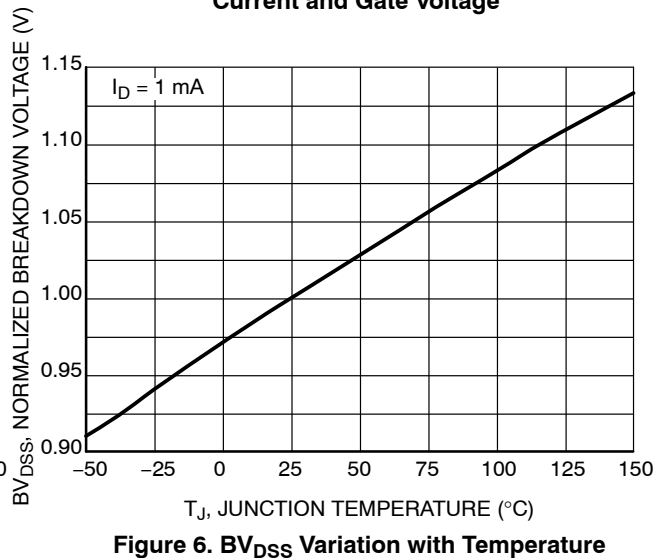
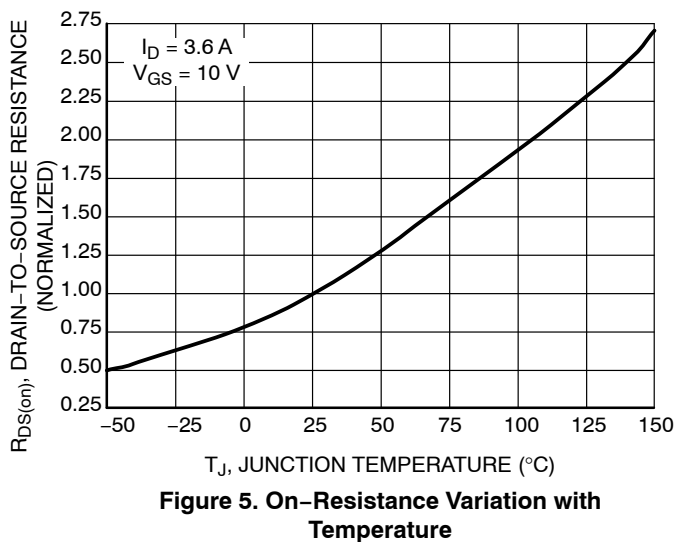
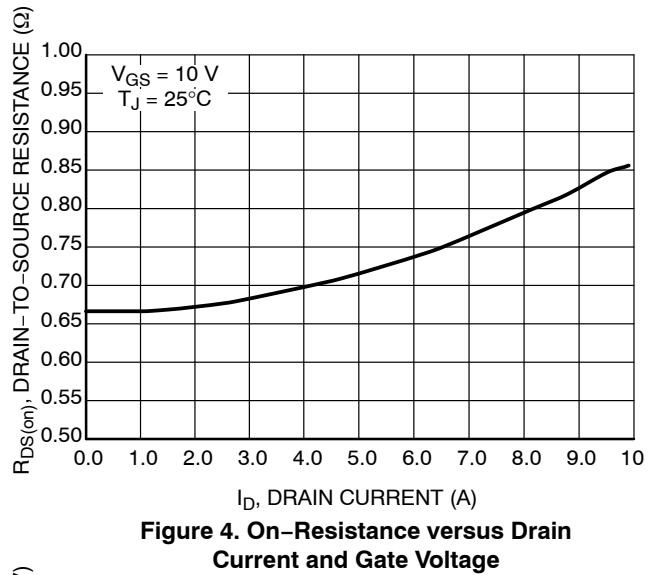
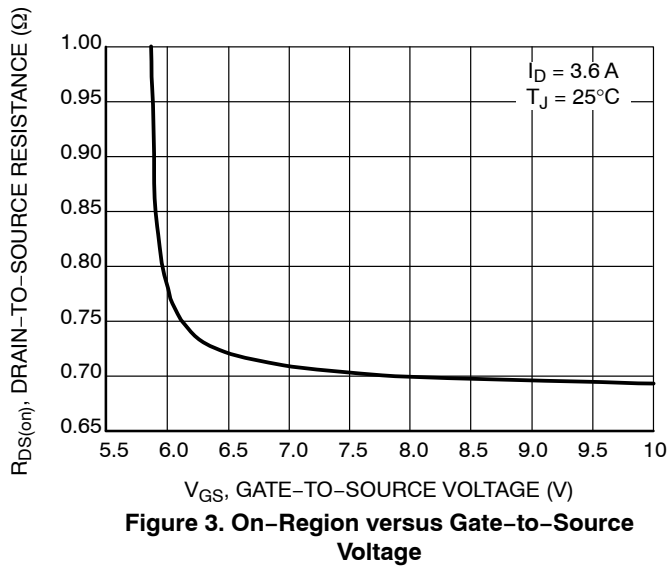
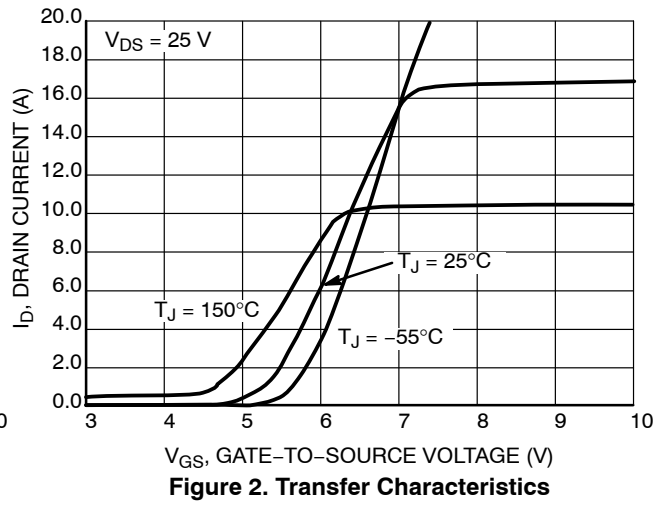
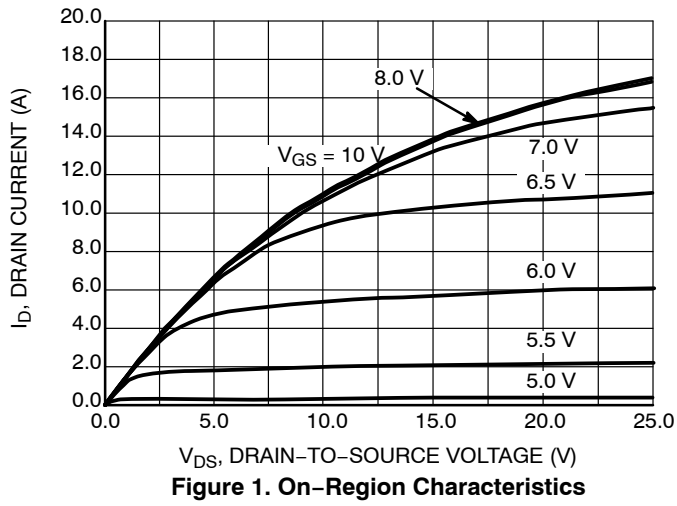
Diode Forward Voltage	$I_S = 7.5\text{ A}, V_{GS} = 0\text{ V}$	V_{SD}			1.6	V
Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}$ $I_S = 7.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	t_{rr}		295		ns
Reverse Recovery Charge		Q_{rr}		1.85		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Width $\leq 380\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

5. Guaranteed by design.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

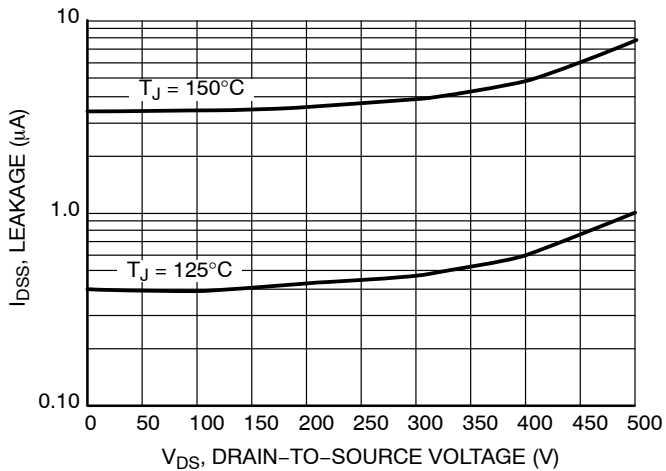


Figure 7. Drain-to-Source Leakage Current versus Voltage

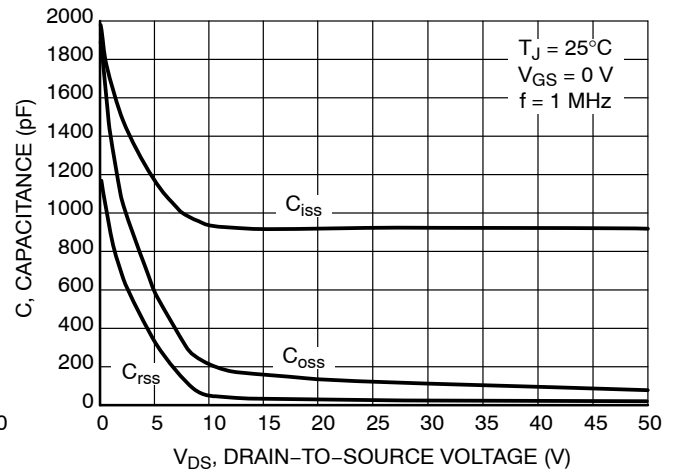


Figure 8. Capacitance Variation

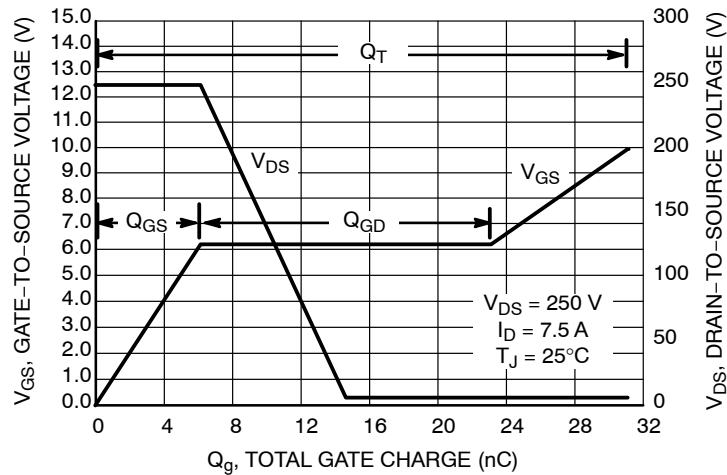


Figure 9. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

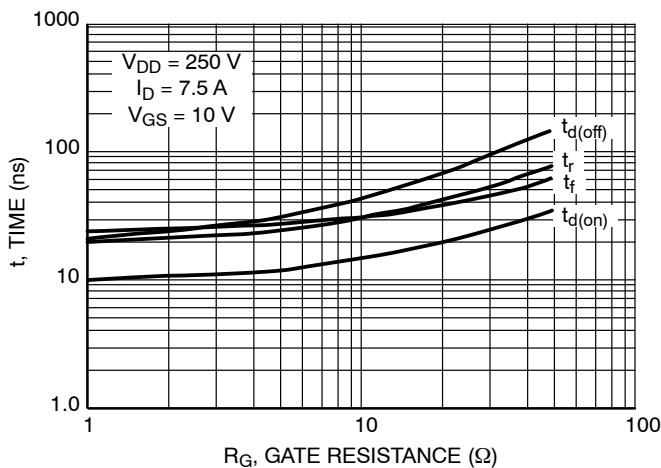


Figure 10. Resistive Switching Time Variation versus Gate Resistance

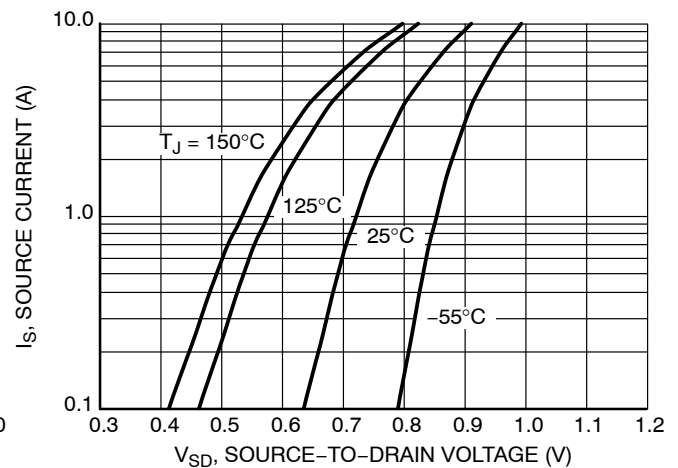


Figure 11. Diode Forward Voltage versus Current

NDF08N50Z

TYPICAL CHARACTERISTICS

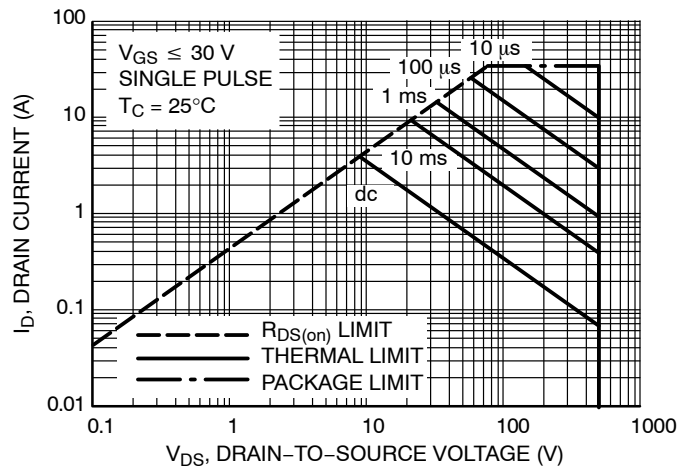


Figure 12. Maximum Rated Forward Biased Safe Operating Area NDF08N50Z

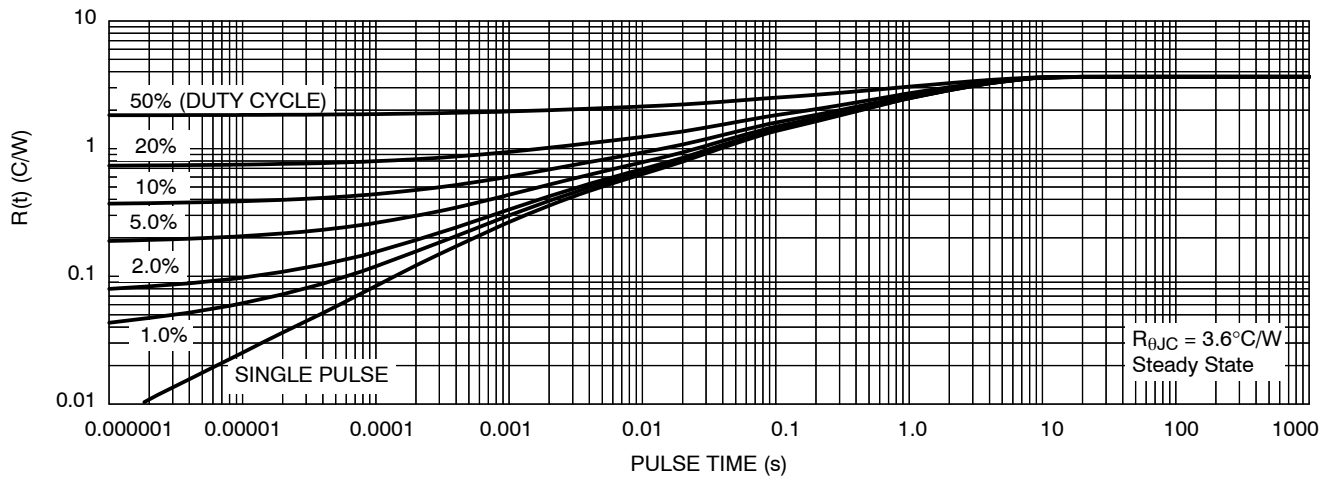


Figure 13. Thermal Impedance (Junction-to-Case) for NDF08N50Z

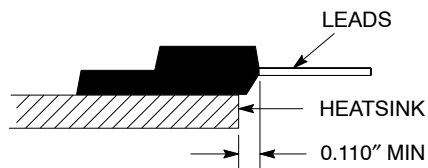


Figure 14. Isolation Test Diagram

Measurement made between leads and heatsink with all leads shorted together.

*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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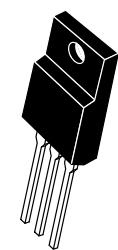


TO-220 FULLPACK, 3-LEAD

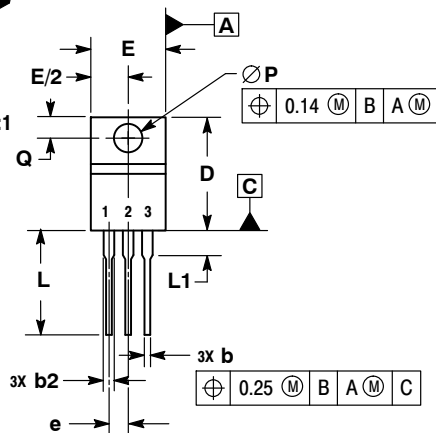
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ISSUE F

DATE 30 SEP 2014

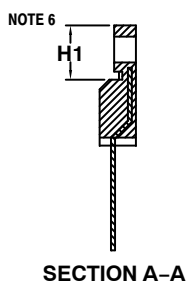
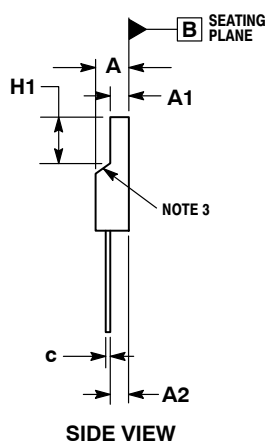
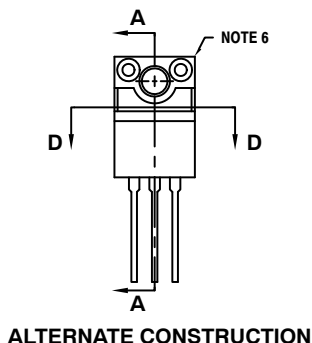


SCALE 1:1



FRONT VIEW

SECTION D-D

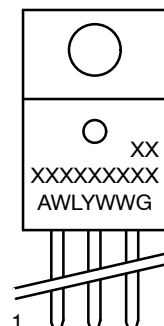


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR UNCONTROLLED IN THIS AREA.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE TO BE MEASURED AT OUTERMOST EXTREME OF THE PLASTIC BODY.
5. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 2.00.
6. CONTOURS AND FEATURES OF THE MOLDED PACKAGE BODY MAY VARY WITHIN THE ENVELOPE DEFINED BY DIMENSIONS A1 AND H1 FOR MANUFACTURING PURPOSES.

DIM	MIN	MAX
A	4.30	4.70
A1	2.50	2.90
A2	2.50	2.90
b	0.54	0.84
b2	1.10	1.40
c	0.49	0.79
D	14.70	15.30
E	9.70	10.30
e	2.54 BSC	
H1	6.60	7.10
L	12.50	14.73
L1	---	2.80
P	3.00	3.40
Q	2.80	3.20

GENERIC MARKING DIAGRAM*



A = Assembly Location
 WL = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
 Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLE 1:

- PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE

STYLE 2:

- PIN 1. CATHODE
2. ANODE
3. GATE

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DESCRIPTION: TO-220 FULLPACK, 3-LEAD

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