

# NTGS3443B

## MOSFET – Power, Single, P-Channel, TSOP-6 -20 V, -4.2 A

### Features

- Low  $R_{DS(on)}$  in TSOP-6 Package
- 2.5 V Gate Rating
- Fast Switching
- This is a Pb-Free Device

### Applications

- Optimized for Battery and Load Management Applications in Portable Equipment
- Li Ion Battery Linear Mode Charging
- High Side Load Switch
- HDD Switching Circuits, Camera Phone, etc.

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

| Parameter                                                         |                        |                       | Symbol                            | Value          | Unit |
|-------------------------------------------------------------------|------------------------|-----------------------|-----------------------------------|----------------|------|
| Drain-to-Source Voltage                                           |                        |                       | V <sub>DSS</sub>                  | −20            | V    |
| Gate-to-Source Voltage                                            |                        |                       | V <sub>GS</sub>                   | ± 12           | V    |
| Continuous Drain Current (Note 1)                                 | Steady State           | T <sub>A</sub> = 25°C | I <sub>D</sub>                    | −3.7           | A    |
|                                                                   |                        | T <sub>A</sub> = 85°C |                                   | −2.7           |      |
|                                                                   | t ≤ 5 s                | T <sub>A</sub> = 25°C |                                   | −4.2           |      |
| Power Dissipation (Note 1)                                        | Steady State           | T <sub>A</sub> = 25°C | P <sub>D</sub>                    | 1.25           | W    |
|                                                                   | t ≤ 5 s                |                       |                                   | 1.6            |      |
| Continuous Drain Current (Note 2)                                 | Steady State           | T <sub>A</sub> = 25°C | I <sub>D</sub>                    | −2.7           | A    |
|                                                                   |                        | T <sub>A</sub> = 85°C |                                   | −2.0           |      |
| Power Dissipation (Note 2)                                        |                        |                       | T <sub>A</sub> = 25°C             | P <sub>D</sub> | 0.7  |
| Pulsed Drain Current                                              | t <sub>p</sub> = 10 μs |                       | I <sub>DM</sub>                   | −15            | A    |
| Operating Junction and Storage Temperature                        |                        |                       | T <sub>J</sub> , T <sub>STG</sub> | −55 to 150     | °C   |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) |                        |                       | T <sub>L</sub>                    | 260            | °C   |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 in sq pad size.  
(Cu area = 1.127 in sq [2 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size.  
(Cu area = 0.0775 in sq)

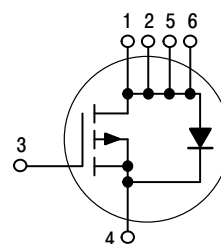


ON Semiconductor®

<http://onsemi.com>

| $V_{(BR)DSS}$ | $R_{DS(ON)} \text{ MAX}$ | $I_D \text{ MAX}$ |
|---------------|--------------------------|-------------------|
| -20 V         | 60 m $\Omega$ @ -4.5 V   | -3.7 A            |
|               | 90 m $\Omega$ @ -2.7 V   | -3.1 A            |
|               | 100 m $\Omega$ @ -2.5 V  | -3.0 A            |

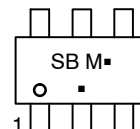
### P-Channel



### MARKING DIAGRAM

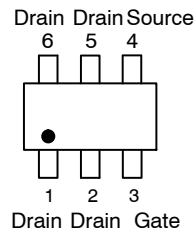


TSOP-6  
CASE 318G  
STYLE 1



SB = Device Code  
M = Date Code  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

### PIN ASSIGNMENT



### ORDERING INFORMATION

| Device       | Package             | Shipping†          |
|--------------|---------------------|--------------------|
| NTGS3443BT1G | TSOP-6<br>(Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTGS3443B

## THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter                                   | Symbol          | Value | Unit |
|---------------------------------------------|-----------------|-------|------|
| Junction-to-Ambient – Steady State (Note 3) | $R_{\theta JA}$ | 100   | °C/W |
| Junction-to-Ambient – $t \leq 5$ s (Note 3) | $R_{\theta JA}$ | 80    |      |
| Junction-to-Ambient – Steady State (Note 4) | $R_{\theta JA}$ | 190   |      |

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).  
4. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0775 in sq).

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

### OFF CHARACTERISTICS

|                                                           |                   |                                                                |     |     |           |               |
|-----------------------------------------------------------|-------------------|----------------------------------------------------------------|-----|-----|-----------|---------------|
| Drain-to-Source Breakdown Voltage                         | $V_{(BR)DSS}$     | $V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$           | -20 |     |           | V             |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | $I_D = -250\text{ }\mu\text{A}$ , Reference $25^\circ\text{C}$ |     | -15 |           | mV/°C         |
| Zero Gate Voltage Drain Current                           | $I_{DSS}$         | $V_{GS} = 0\text{ V}, V_{DS} = -20\text{ V}$                   |     |     | -1.0      | $\mu\text{A}$ |
|                                                           |                   |                                                                |     |     | -5.0      |               |
| Gate-to-Source Leakage Current                            | $I_{GSS}$         | $V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$                |     |     | $\pm 0.1$ | $\mu\text{A}$ |

### ON CHARACTERISTICS (Note 5)

|                                            |                  |                                                  |      |     |      |            |
|--------------------------------------------|------------------|--------------------------------------------------|------|-----|------|------------|
| Gate Threshold Voltage                     | $V_{GS(TH)}$     | $V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$ | -0.6 |     | -1.4 | V          |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ |                                                  |      | 3.3 |      | mV/°C      |
| Drain-to-Source On Resistance              | $R_{DS(on)}$     | $V_{GS} = -4.5\text{ V}, I_D = -3.7\text{ A}$    |      | 45  | 60   | m $\Omega$ |
|                                            |                  | $V_{GS} = -2.7\text{ V}, I_D = -3.1\text{ A}$    |      | 65  | 90   |            |
|                                            |                  | $V_{GS} = -2.5\text{ V}, I_D = -3.0\text{ A}$    |      | 70  | 100  |            |
| Forward Transconductance                   | $g_{FS}$         | $V_{DS} = -10\text{ V}, I_D = -3.7\text{ A}$     |      | 7.0 |      | S          |

### CHARGES, CAPACITANCES AND GATE RESISTANCE

|                              |              |                                                                      |  |     |    |          |
|------------------------------|--------------|----------------------------------------------------------------------|--|-----|----|----------|
| Input Capacitance            | $C_{ISS}$    | $V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = -10\text{ V}$       |  | 819 |    | pF       |
| Output Capacitance           | $C_{OSS}$    |                                                                      |  | 157 |    |          |
| Reverse Transfer Capacitance | $C_{RSS}$    |                                                                      |  | 103 |    |          |
| Total Gate Charge            | $Q_{G(TOT)}$ | $V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}; I_D = -3.7\text{ A}$ |  | 8.0 | 11 | nC       |
| Threshold Gate Charge        | $Q_{G(TH)}$  |                                                                      |  | 0.6 |    |          |
| Gate-to-Source Charge        | $Q_{GS}$     |                                                                      |  | 1.7 |    |          |
| Gate-to-Drain Charge         | $Q_{GD}$     |                                                                      |  | 2.4 |    |          |
| Gate Resistance              | $R_G$        |                                                                      |  | 11  |    | $\Omega$ |

### SWITCHING CHARACTERISTICS (Note 6)

|                     |              |                                                                                               |  |     |    |    |
|---------------------|--------------|-----------------------------------------------------------------------------------------------|--|-----|----|----|
| Turn-On Delay Time  | $t_{d(ON)}$  | $V_{GS} = -4.5\text{ V}, V_{DD} = -10\text{ V}, I_D = -1.0\text{ A}, R_G = 6.0\text{ }\Omega$ |  | 10  | 15 | ns |
| Rise Time           | $t_r$        |                                                                                               |  | 7.0 | 11 |    |
| Turn-Off Delay Time | $t_{d(OFF)}$ |                                                                                               |  | 47  | 70 |    |
| Fall Time           | $t_f$        |                                                                                               |  | 25  | 40 |    |

### DRAIN-SOURCE DIODE CHARACTERISTICS

|                       |          |                                                                                |                          |  |      |      |    |
|-----------------------|----------|--------------------------------------------------------------------------------|--------------------------|--|------|------|----|
| Forward Diode Voltage | $V_{SD}$ | $V_{GS} = 0\text{ V}, I_S = -1.7\text{ A}$                                     | $T_J = 25^\circ\text{C}$ |  | -0.8 | -1.2 | V  |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = -1.7\text{ A}$ |                          |  | 15   | 30   | ns |

5. Pulse Test: pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
6. Switching characteristics are independent of operating junction temperatures

TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

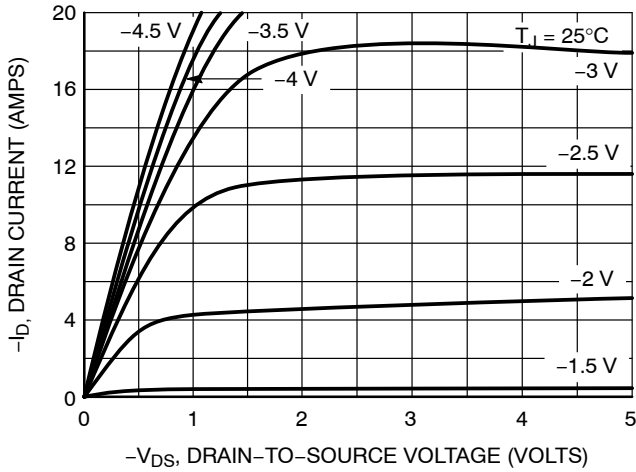


Figure 1. On-Region Characteristics

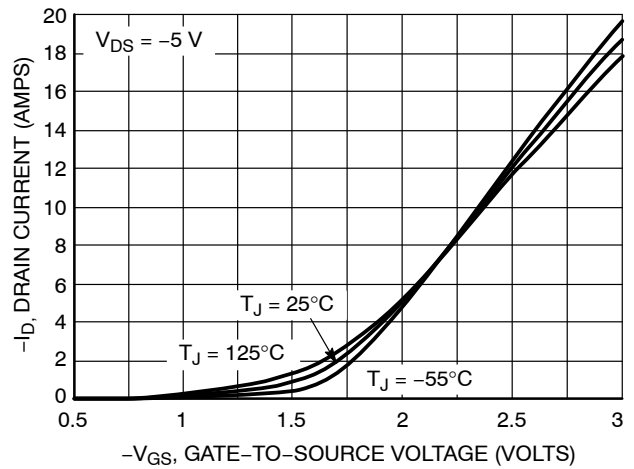


Figure 2. Transfer Characteristics

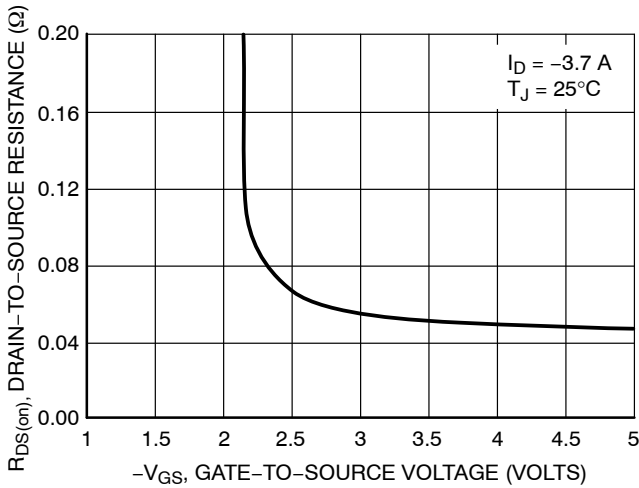


Figure 3. On-Resistance vs. Gate-to-Source Voltage

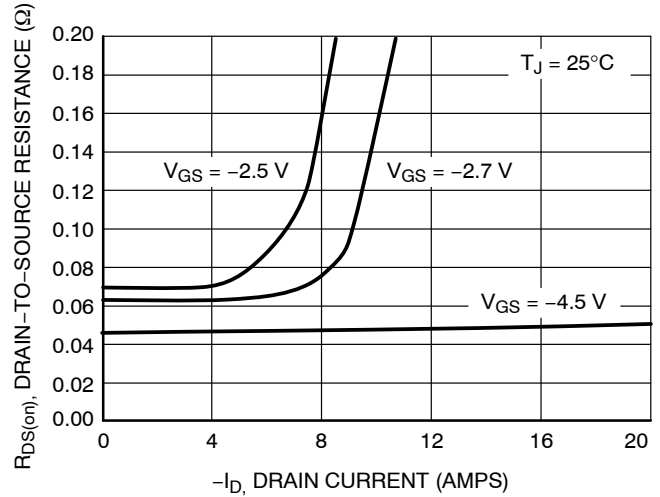


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

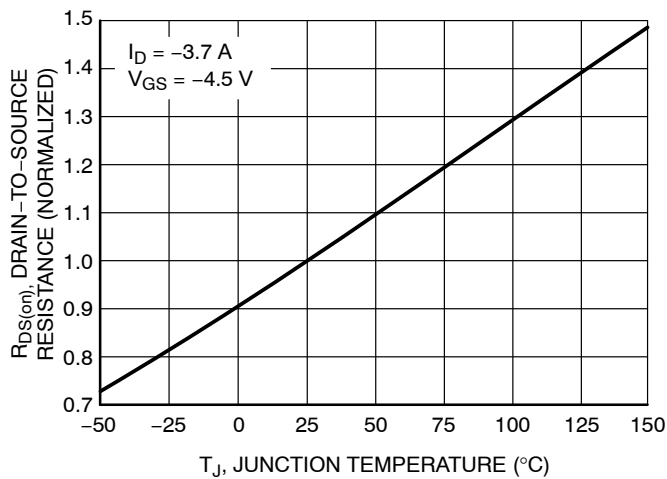


Figure 5. On-Resistance Variation with Temperature

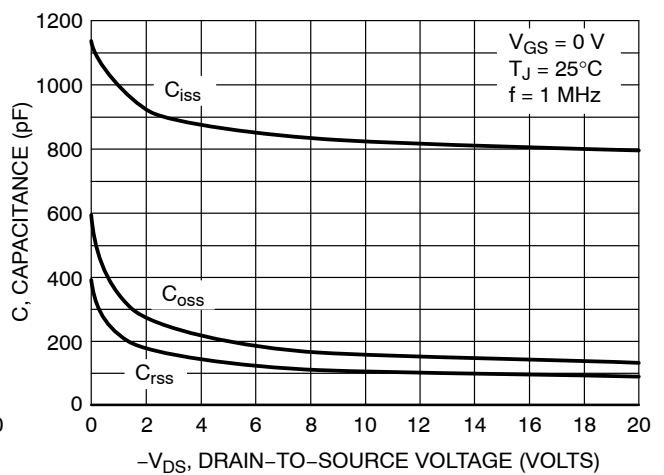
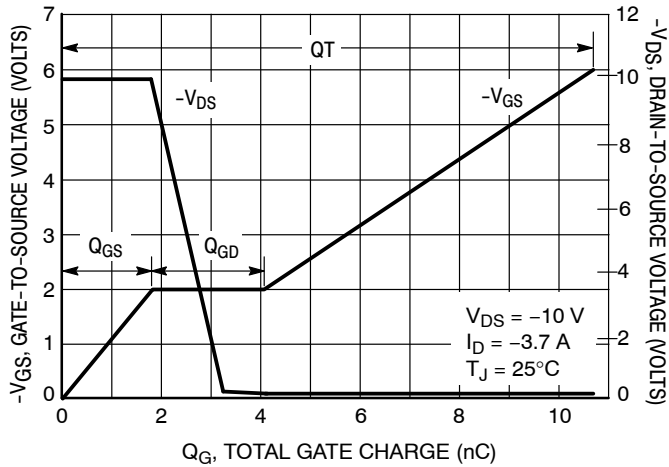


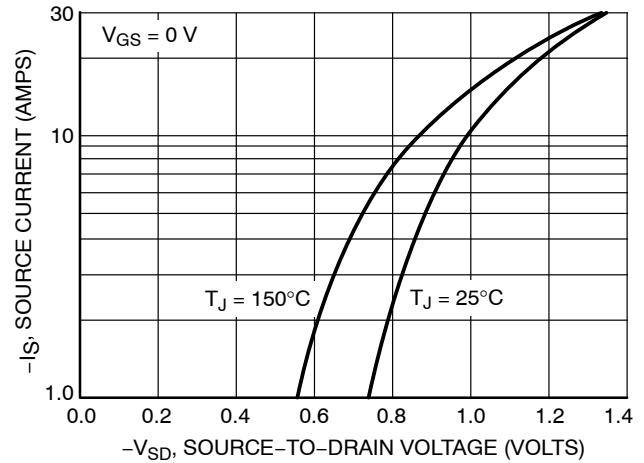
Figure 6. Capacitance Variation

# NTGS3443B

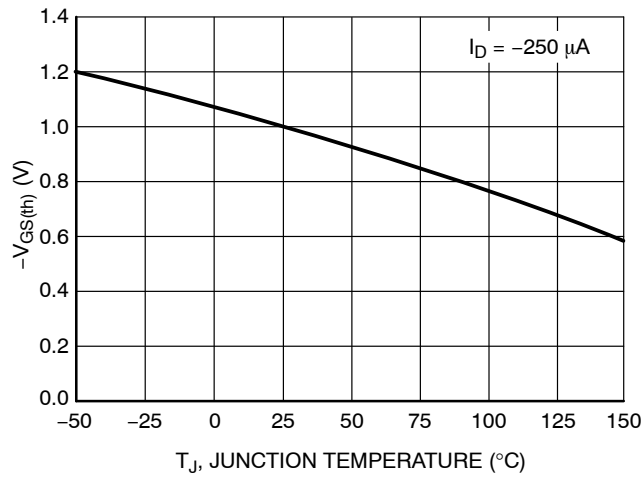
## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)



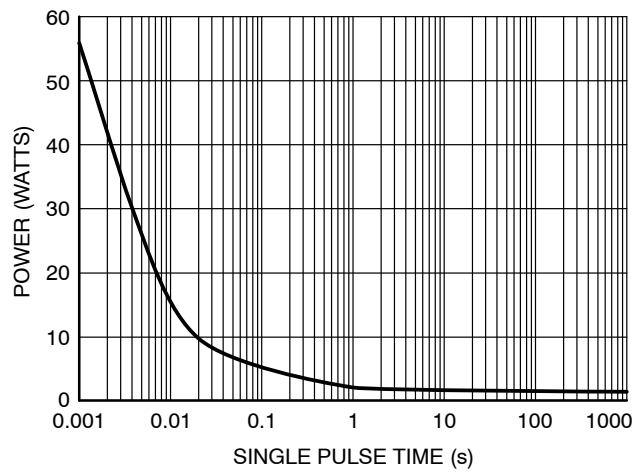
**Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



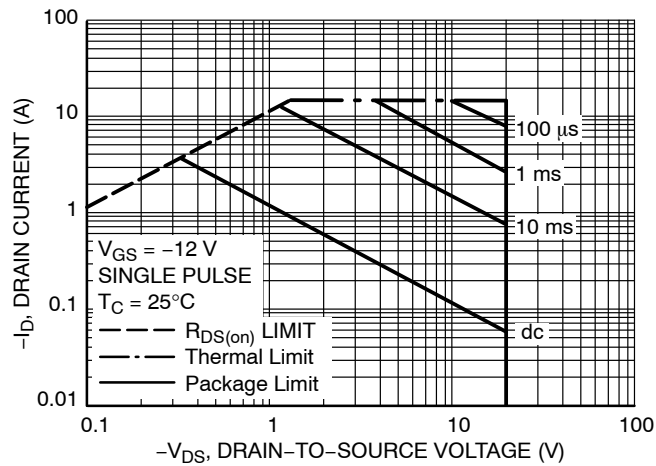
**Figure 8. Diode Forward Voltage vs. Current**



**Figure 9. Threshold Voltage**



**Figure 10. Single Pulse Maximum Power Dissipation**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

# NTGS3443B

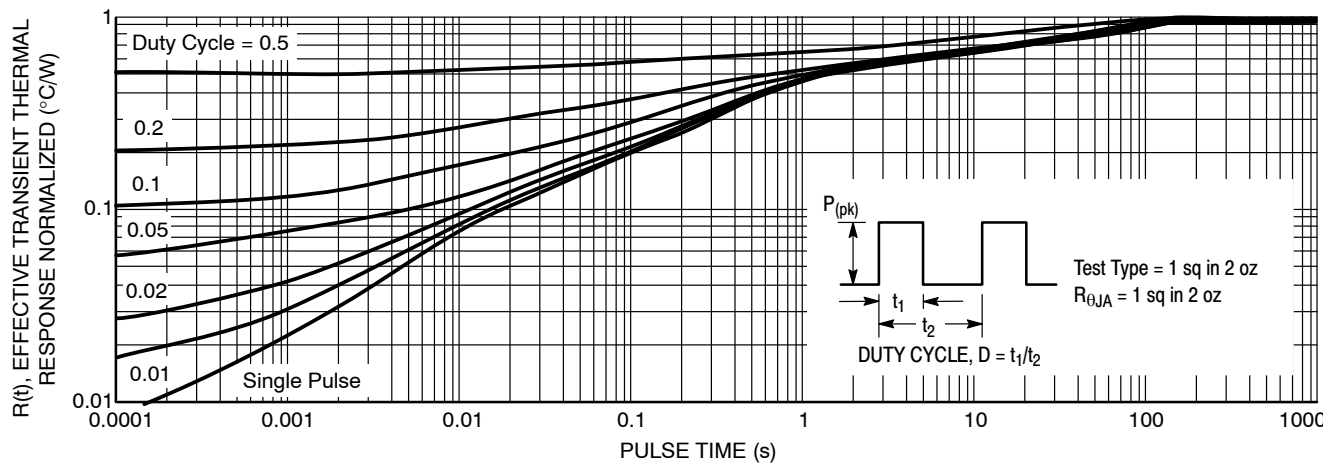


Figure 12. FET Thermal Response

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

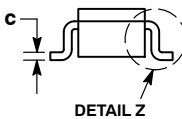
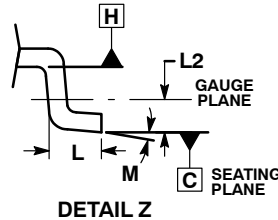
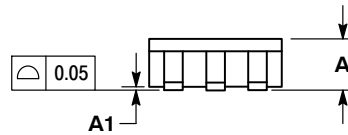
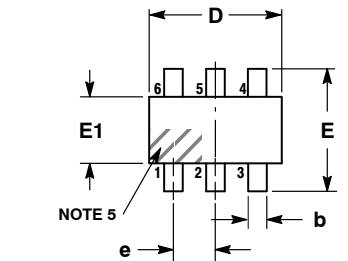
ON Semiconductor®



SCALE 2:1

## TSOP-6 CASE 318G-02 ISSUE V

DATE 12 JUN 2012



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN         | NOM  | MAX  |
| A   | 0.90        | 1.00 | 1.10 |
| A1  | 0.01        | 0.06 | 0.10 |
| b   | 0.25        | 0.38 | 0.50 |
| c   | 0.10        | 0.18 | 0.26 |
| D   | 2.90        | 3.00 | 3.10 |
| E   | 2.50        | 2.75 | 3.00 |
| E1  | 1.30        | 1.50 | 1.70 |
| e   | 0.85        | 0.95 | 1.05 |
| L   | 0.20        | 0.40 | 0.60 |
| L2  | 0.25 BSC    |      |      |
| M   | 0°          | —    | 10°  |

#### STYLE 1:

- PIN 1. DRAIN
- PIN 2. DRAIN
- PIN 3. GATE
- PIN 4. SOURCE
- PIN 5. DRAIN
- PIN 6. DRAIN

#### STYLE 2:

- PIN 1. EMITTER 2
- PIN 2. BASE 1
- PIN 3. COLLECTOR 1
- PIN 4. EMITTER 1
- PIN 5. BASE 2
- PIN 6. COLLECTOR 2

#### STYLE 3:

- PIN 1. ENABLE
- PIN 2. N/C
- PIN 3. R BOOST
- PIN 4. Vz
- PIN 5. V in
- PIN 6. V out

#### STYLE 4:

- PIN 1. N/C
- PIN 2. V in
- PIN 3. NOT USED
- PIN 4. GROUND
- PIN 5. ENABLE
- PIN 6. LOAD

#### STYLE 5:

- PIN 1. EMITTER 2
- PIN 2. BASE 2
- PIN 3. COLLECTOR 1
- PIN 4. EMITTER 1
- PIN 5. BASE 1
- PIN 6. COLLECTOR 2

#### STYLE 6:

- PIN 1. COLLECTOR
- PIN 2. COLLECTOR
- PIN 3. BASE
- PIN 4. EMITTER
- PIN 5. COLLECTOR
- PIN 6. COLLECTOR

#### STYLE 7:

- PIN 1. COLLECTOR
- PIN 2. COLLECTOR
- PIN 3. BASE
- PIN 4. N/C
- PIN 5. COLLECTOR
- PIN 6. EMITTER

#### STYLE 8:

- PIN 1. Vbus
- PIN 2. D(in)
- PIN 3. D(in)+
- PIN 4. D(out)+
- PIN 5. D(out)
- PIN 6. GND

#### STYLE 9:

- PIN 1. LOW VOLTAGE GATE
- PIN 2. DRAIN
- PIN 3. SOURCE
- PIN 4. DRAIN
- PIN 5. DRAIN
- PIN 6. HIGH VOLTAGE GATE

#### STYLE 10:

- PIN 1. D(OUT)+
- PIN 2. GND
- PIN 3. D(OUT)-
- PIN 4. D(IN)-
- PIN 5. VBUS
- PIN 6. D(IN)+

#### STYLE 11:

- PIN 1. SOURCE 1
- PIN 2. DRAIN 2
- PIN 3. DRAIN 2
- PIN 4. SOURCE 2
- PIN 5. GATE 1
- PIN 6. DRAIN 1/GATE 2

#### STYLE 12:

- PIN 1. I/O
- PIN 2. GROUND
- PIN 3. I/O
- PIN 4. I/O
- PIN 5. VCC
- PIN 6. I/O

#### STYLE 13:

- PIN 1. GATE 1
- PIN 2. SOURCE 2
- PIN 3. GATE 2
- PIN 4. DRAIN 2
- PIN 5. SOURCE 1
- PIN 6. DRAIN 1

#### STYLE 14:

- PIN 1. ANODE
- PIN 2. SOURCE
- PIN 3. GATE
- PIN 4. CATHODE/DRAIN
- PIN 5. CATHODE/DRAIN
- PIN 6. CATHODE/DRAIN

#### STYLE 15:

- PIN 1. ANODE
- PIN 2. SOURCE
- PIN 3. GATE
- PIN 4. DRAIN
- PIN 5. N/C
- PIN 6. CATHODE

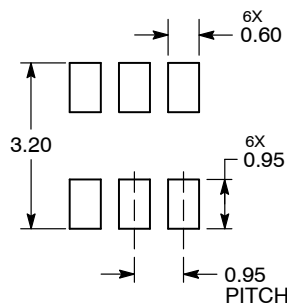
#### STYLE 16:

- PIN 1. ANODE/CATHODE
- PIN 2. BASE
- PIN 3. EMITTER
- PIN 4. COLLECTOR
- PIN 5. ANODE
- PIN 6. CATHODE

#### STYLE 17:

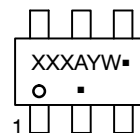
- PIN 1. EMITTER
- PIN 2. BASE
- PIN 3. ANODE/CATHODE
- PIN 4. ANODE
- PIN 5. CATHODE
- PIN 6. COLLECTOR

### RECOMMENDED SOLDERING FOOTPRINT\*

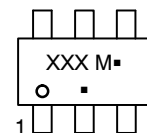


DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM\*



IC



STANDARD

XXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

|                  |             |                                                                                                                                                                                     |
|------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ASB14888C | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | TSOP-6      | PAGE 1 OF 1                                                                                                                                                                         |

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative