

NTD85N02R

Power MOSFET, 85 A, 24 V, N-Channel DPAK/IPAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Low Gate Charge to Minimize Switching Losses
- Pb-Free Packages are Available

Applications

- CPU Power Delivery
- DC-DC Converters
- Low Side Switching

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	24	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	17	A
		$T_A = 85^{\circ}\text{C}$		12	
Power Dissipation $R_{\theta JA}$ (Note 1)		$T_A = 25^{\circ}\text{C}$	P_D	2.4	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)		$T_A = 25^{\circ}\text{C}$	I_D	12	A
		$T_A = 85^{\circ}\text{C}$		8.8	
Power Dissipation $R_{\theta JA}$ (Note 2)		$T_A = 25^{\circ}\text{C}$	P_D	1.25	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)		$T_C = 25^{\circ}\text{C}$	I_D	85	A
		$T_C = 85^{\circ}\text{C}$		58	
Power Dissipation $R_{\theta JC}$ (Note 1)		$T_C = 25^{\circ}\text{C}$	P_D	78.1	W
Pulsed Drain Current		$T_A = 25^{\circ}\text{C}, t_p = 10\mu\text{s}$		I_{DM}	192
Current Limited by Package		$T_A = 25^{\circ}\text{C}$	$I_{DmaxPkg}$	45	A
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to +150	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	78	A
Drain to Source dV/dt			dV/dt	6	V/ns
Single Pulse Drain-to-Source Avalanche Energy $T_J = 25^{\circ}\text{C}, V_{DD} = 30\text{ V}, V_{GS} = 10\text{ V}, I_L = 13\text{ A}_{pk}, L = 1.0\text{ mH}, R_G = 25\text{ }\Omega$			EAS	85	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

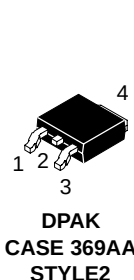
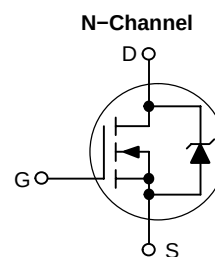
1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.



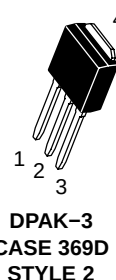
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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
24 V	5.2 m Ω @ 10 V	85 A

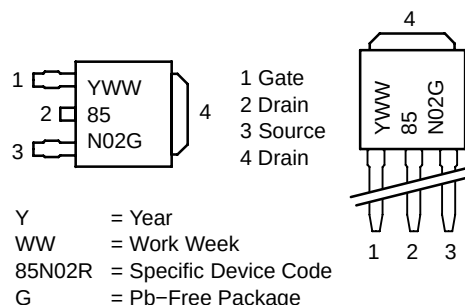


DPAK
CASE 369AA
STYLE2



DPAK-3
CASE 369D
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

NTD85N02R

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	1.6	°C/W
Junction-to-TAB (Drain)	$R_{\theta JC-TAB}$	3.5	
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	52	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	100	

1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	24	28		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			20.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1.5	μA
					10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.0	1.5	2.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4		mV/°C
Drain-to-Source on Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		4.8	5.2	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		6.5		
Forward Transconductance	g_{FS}	$V_{DS} = 10\text{ V}, I_D = 15\text{ A}$		38		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 20\text{ V}$		2050		pF
Output Capacitance	C_{OSS}			871		
Reverse Transfer Capacitance	C_{RSS}			359		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 5.0\text{ V}, V_{DS} = 10\text{ V}; I_D = 10\text{ A}$		17.7		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.6		
Gate-to-Source Charge	Q_{GS}			2.6		
Gate-to-Drain Charge	Q_{GD}			7.1		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}; I_D = 10\text{ A}$		35.1		nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}, I_D = 30\text{ A}, R_G = 3.0\text{ }\Omega$		6.3		ns
Rise Time	t_r			77		
Turn-Off Delay Time	$t_{d(OFF)}$			25		
Fall Time	t_f			12		

3. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
4. Switching characteristics are independent of operating junction temperatures.

NTD85N02R

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 30 A	T _J = 25°C	0.81	1.0	V
			T _J = 125°C	0.65		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 20 A		37.5		ns
Charge Time	t _a			16.8		
Discharge Time	t _b			20.7		
Reverse Recovery Charge	Q _{RR}			27		nC

PACKAGE PARASITIC VALUES

Source Inductance	L _S	T _A = 25°C		2.49		nH
Drain Inductance, DPAK	L _D			0.0164		
Drain Inductance, IPAK*	L _D			1.88		
Gate Inductance	L _G			3.46		
Gate Resistance	R _G			1.2		Ω

*Assume standoff of 110 mils.

ORDERING INFORMATION

Device	Package	Shipping [†]
NTD85N02R	DPAK	75 Units / Rail
NTD85N02RG	DPAK (Pb-Free)	
NTD85N02R-001	IPAK	800 / Tape & Reel
NTD85N02R-1G	IPAK (Pb-Free)	
NTD85N02RT4	DPAK	2500 / Tape & Reel
NTD85N02RT4G	DPAK (Pb-Free)	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTD85N02R

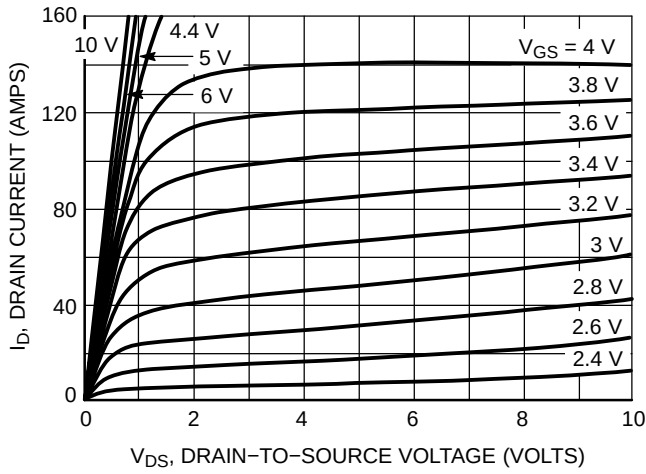


Figure 1. On-Region Characteristics

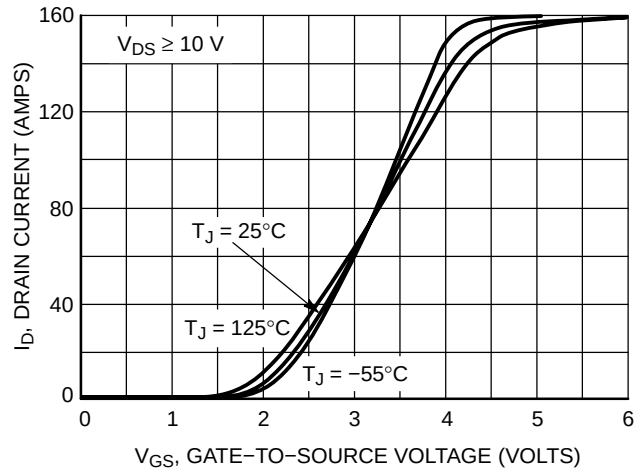


Figure 2. Transfer Characteristics

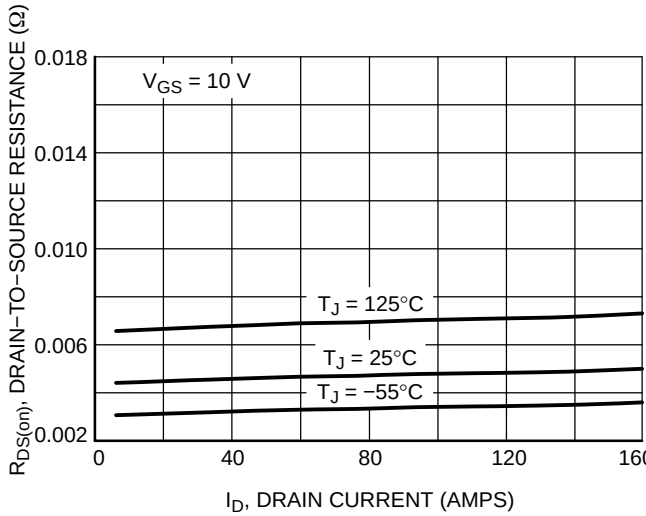


Figure 3. On-Resistance versus Drain Current and Temperature

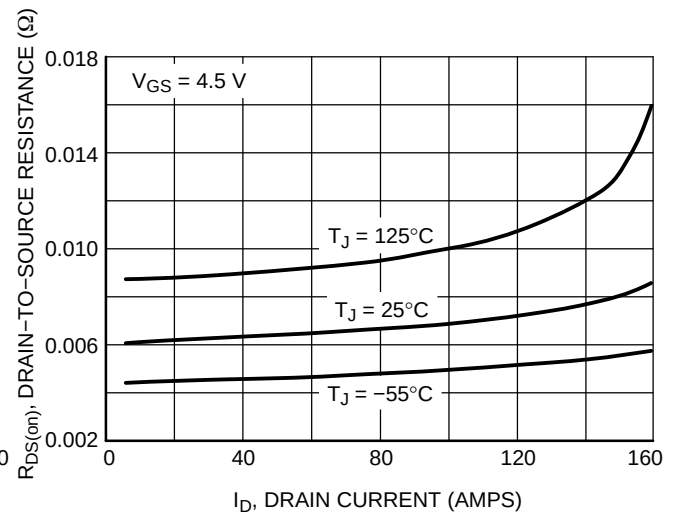


Figure 4. On-Resistance versus Drain Current and Temperature

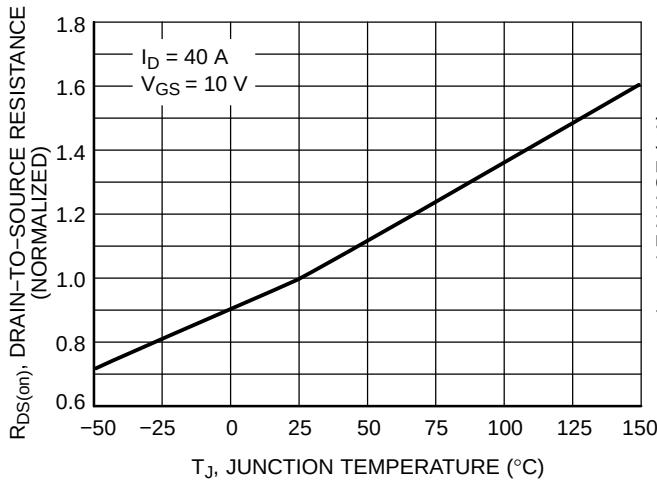


Figure 5. On-Resistance Variation with Temperature

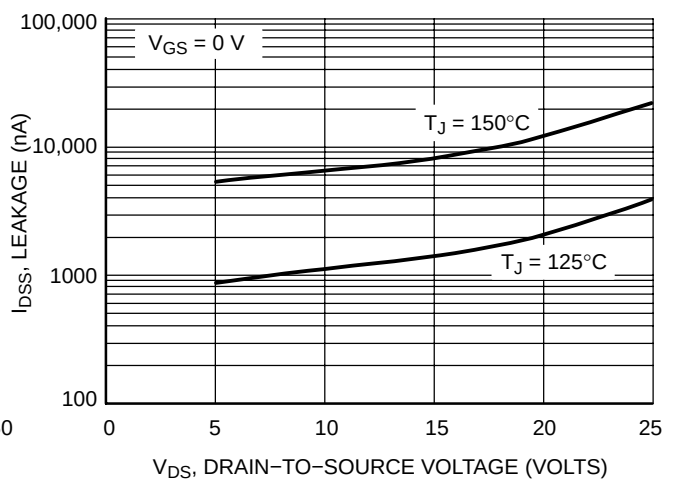
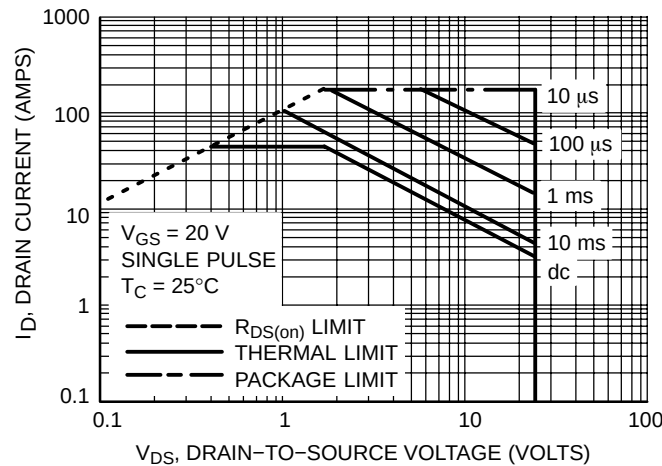
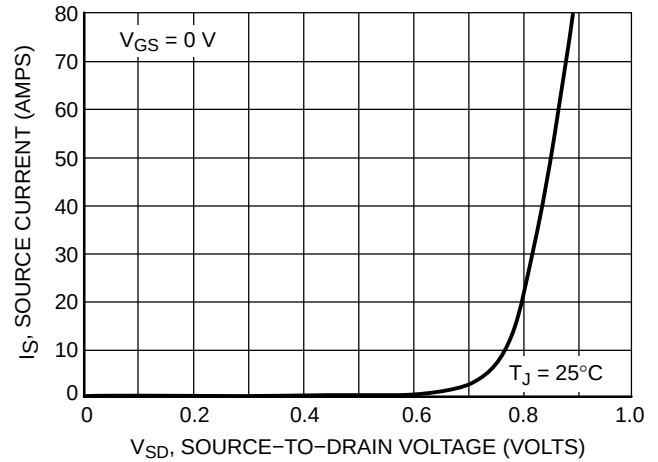
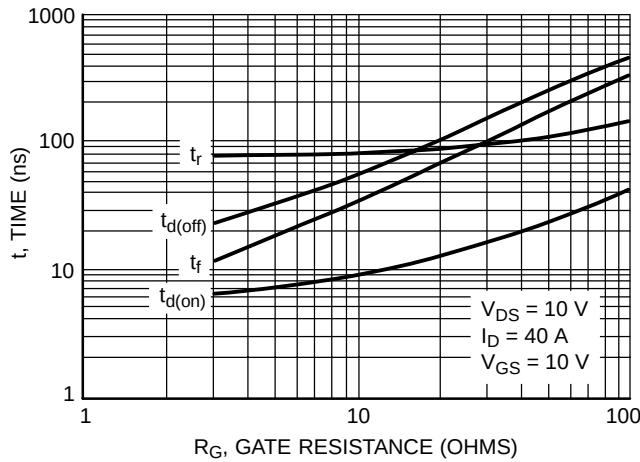
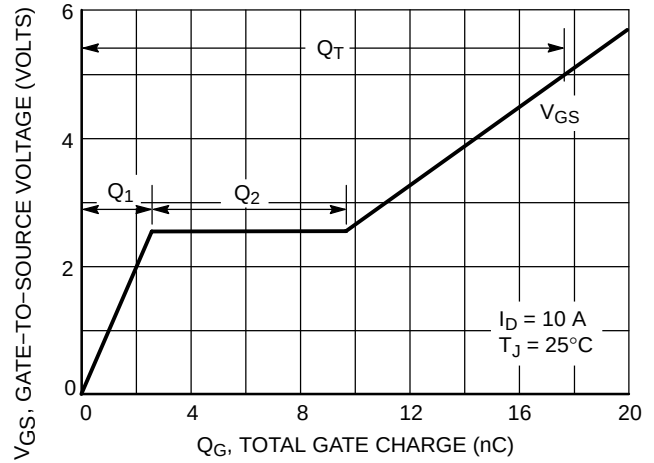
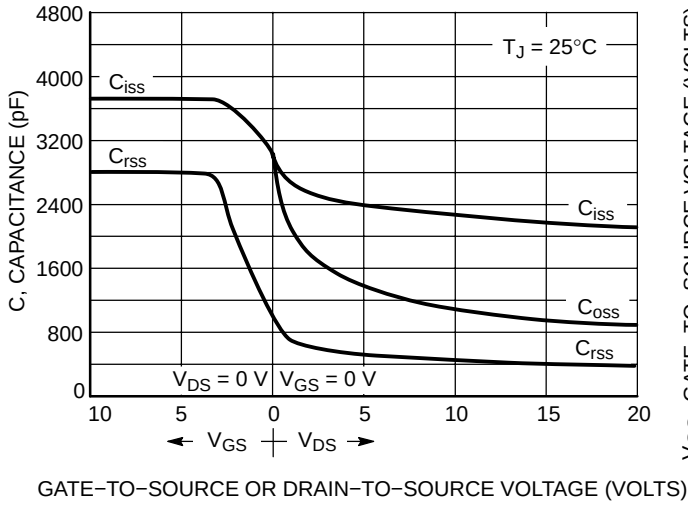


Figure 6. Drain-to-Source Leakage Current versus Voltage

POWER MOSFET SWITCHING



NTD85N02R

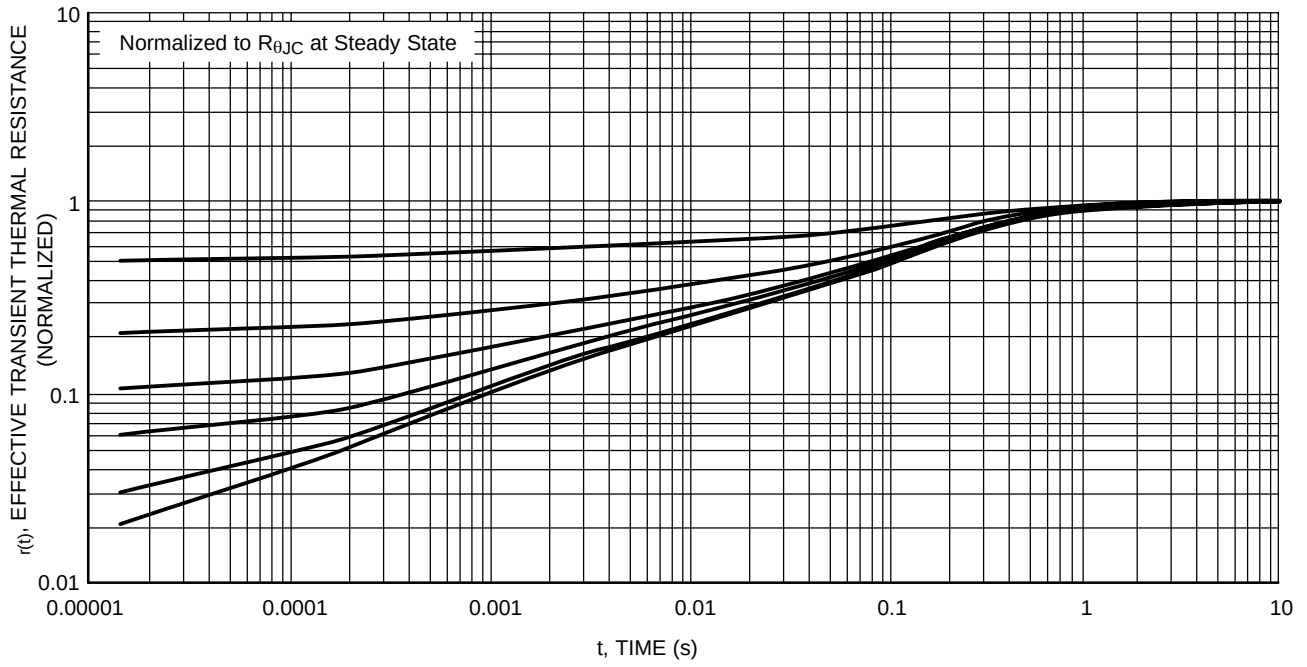


Figure 12. Thermal Response

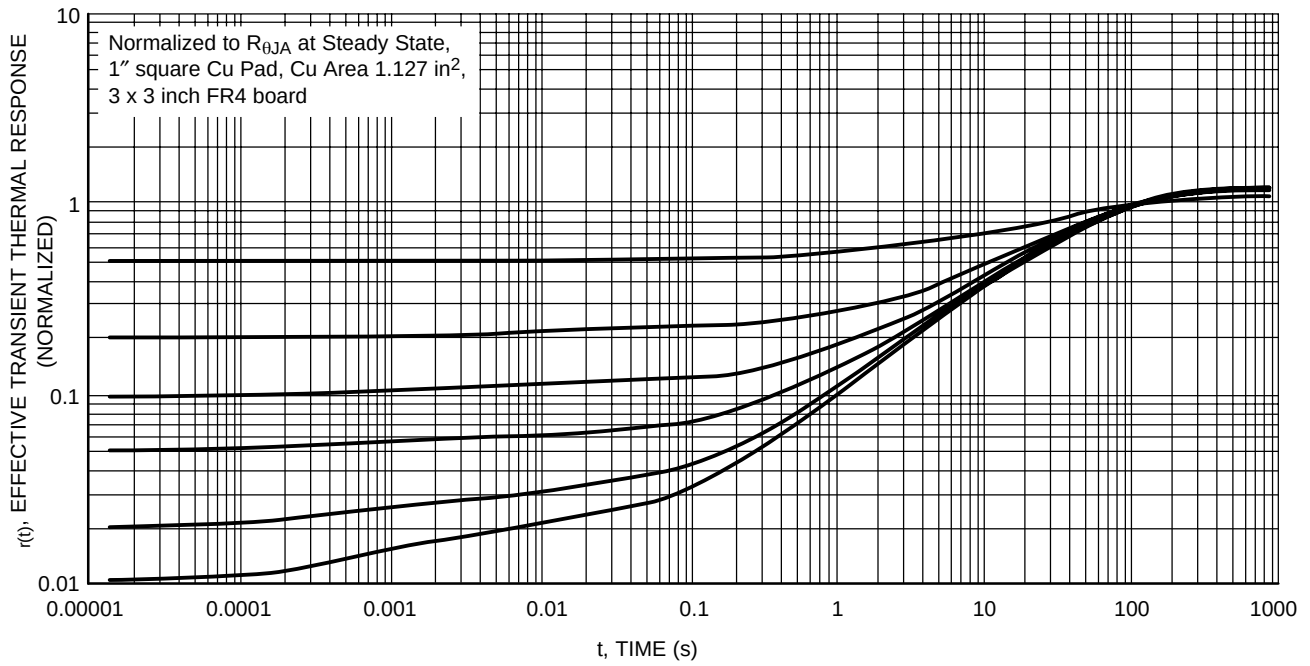


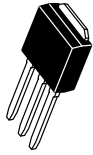
Figure 13. Thermal Response

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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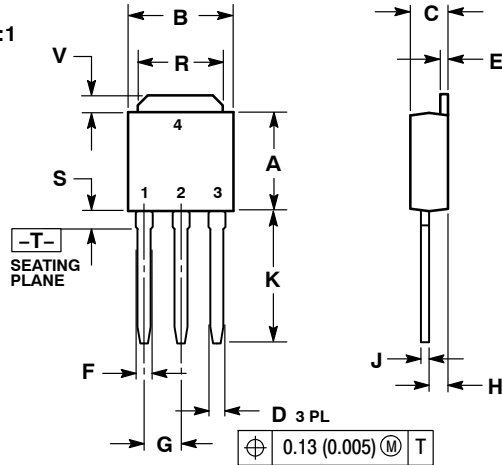
ON



IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

SCALE 1:1



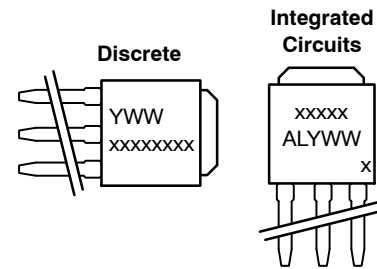
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

MARKING DIAGRAMS

- STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN
- STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE
- STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE
- STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE
- STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2
- STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



xxxxxxxx = Device Code
A = Assembly Location
IL = Wafer Lot
Y = Year
WW = Work Week

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DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)	PAGE 1 OF 1

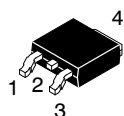
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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ON



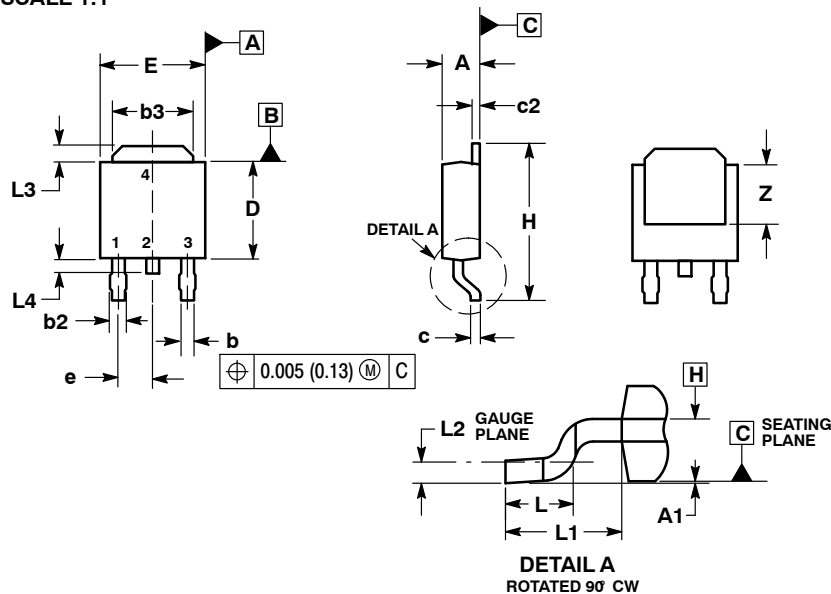
SCALE 1:1

DPAK (SINGLE GAUGE)

CASE 369AA-01

ISSUE B

DATE 03 JUN 2010



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

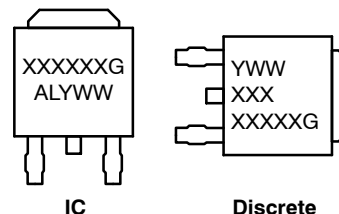
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

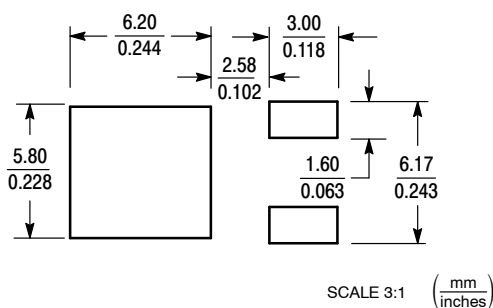
GENERIC MARKING DIAGRAM*



XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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