

MOSFET - Power, Single N-Channel, TOLL

40 V, 0.95 mΩ, 300 A

FDBL9403-F085T6

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- Small Footprint (TOLL) for Compact Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	40	V
Gate-to-Source Voltage			V _{GS}	+20/-16	V
Continuous Drain Current R _{θJC} (Notes 1, 3)	Steady State	T _C = 25°C	I _D	300	A
		T _C = 100°C		217	
Power Dissipation R _{θJC} (Note 1)		T _C = 25°C	P _D	159.6	W
		T _C = 100°C		79.8	
Continuous Drain Current R _{θJA} (Notes 1, 2, 3)	Steady State	T _A = 25°C	I _D	50	A
		T _A = 100°C		36	
Power Dissipation R _{θJA} (Notes 1, 2)		T _A = 25°C	P _D	4.3	W
		T _A = 100°C		2.1	
Pulsed Drain Current	T _A = 25°C, t _p = 10 μs		I _{DM}	3565	A
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +175	°C
Source Current (Body Diode)			I _S	330	A
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 35 A, L = 1 mH)			E _{AS}	612.5	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	0.94	$^\circ\text{C/W}$
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	35	

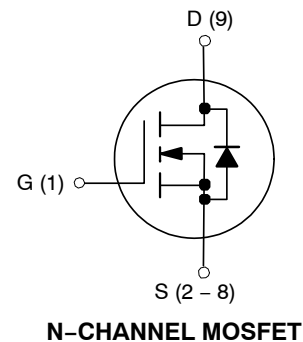
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Current is limited by bondwire configuration.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



ON Semiconductor®

www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	0.95 mΩ @ 10 V	300 A



**H-PSOF8L
CASE 100CU**

ORDERING INFORMATION

Device	Package	Shipping†
FDBL9403-F085T6	H-PSOF8L (Pb-Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FDBL9403–F085T6

Table 1. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$		40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				22		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\ \text{V}$, $V_{GS} = 0\ \text{V}$	$T_J = 25^\circ\text{C}$			1	μA
			$T_J = 175^\circ\text{C}$		310		μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = +20/-16\ \text{V}$				±100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$		2	2.8	4	V
Threshold Temperature Coefficient	$V_{GS(th)}/T_J$				-7.1		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 50\ \text{A}$			0.84	0.95	mΩ
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{iss}	$V_{GS} = 0\ \text{V}$, $V_{DS} = 25\ \text{V}$, $f = 100\ \text{KHz}$			6985		pF
Output Capacitance	C_{oss}				3720		pF
Reverse Transfer Capacitance	C_{rss}				68		pF
Gate Resistance	R_g	$V_{GS} = 0.5\ \text{V}$, $f = 1\ \text{MHz}$			1.1		Ω
Total Gate Charge	$Q_{G(tot)}$	$V_{GS} = 10\ \text{V}$, $V_{DS} = 20\ \text{V}$, $I_D = 50\ \text{A}$			108		nC
Threshold Gate Charge	$Q_{G(th)}$	$V_{GS} = 0\ \text{to}\ 2\ \text{V}$			13		nC
Gate-to-Source Gate Charge	Q_{gs}	$V_{DD} = 22\ \text{V}$, $I_D = 50\ \text{A}$			28		nC
Gate-to-Drain “Miller” Charge	Q_{gd}				23		nC
Plateau Voltage	V_{GP}				4.4		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\ \text{V}$, $V_{DD} = 20\ \text{V}$, $I_D = 50\ \text{A}$, $R_{GEN} = 6\ \Omega$			33		ns
Turn-On Rise Time	t_r				56		ns
Turn-Off Delay Time	$t_{d(off)}$				84		ns
Turn-Off Fall Time	t_f				39		ns
DRAIN-SOURCE DIODE CHARACTERISTICS							
Source-to-Drain Diode Voltage	V_{SD}	$I_{SD} = 50\ \text{A}$, $V_{GS} = 0\ \text{V}$			0.79	1.2	V
Reverse Recovery Time	t_{rr}	$V_{GS} = 0\ \text{V}$, $dI_S/dt = 100\ \text{A}/\mu\text{s}$, $I_S = 50\ \text{A}$			84		ns
Charge Time	t_a				54		ns
Discharge Time	t_b				30		ns
Reverse Recovery Charge	Q_{rr}				172		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

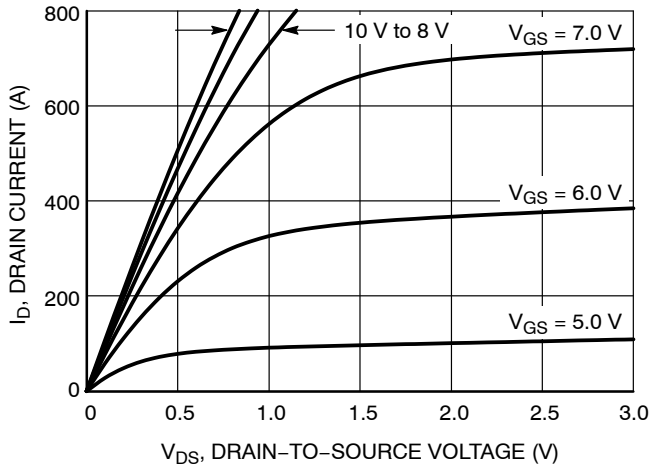


Figure 1. On-Region Characteristics

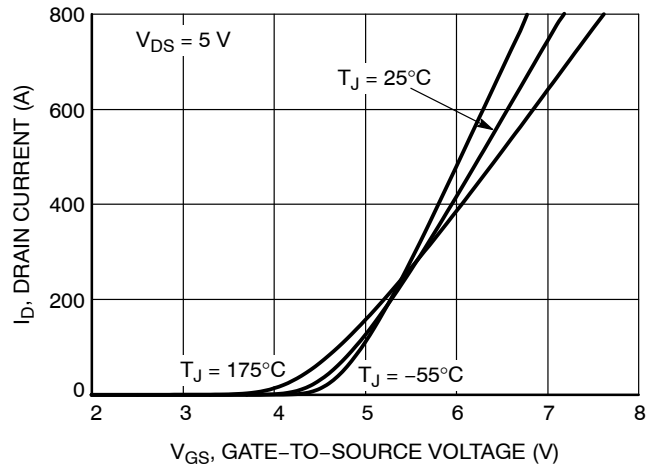


Figure 2. Transfer Characteristics

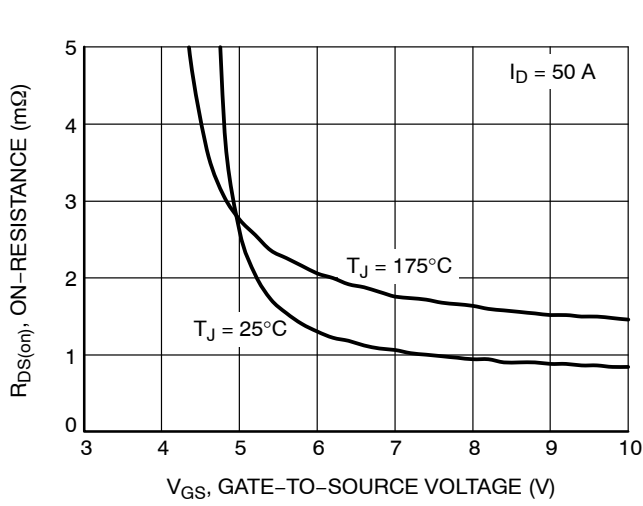


Figure 3. On-Resistance vs. Gate-to-Source Voltage

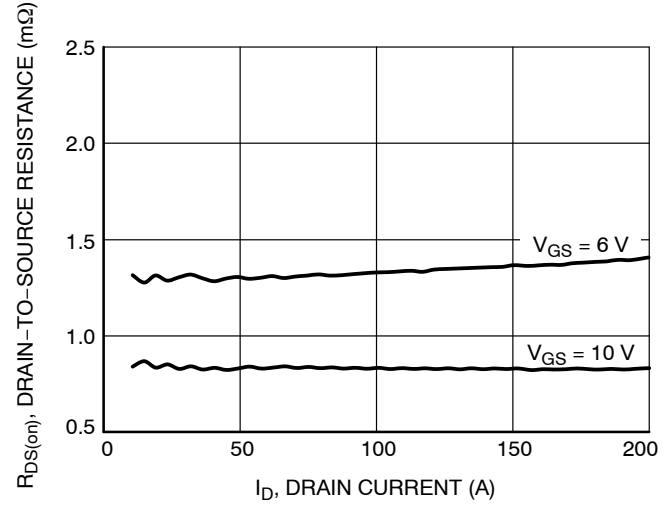


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

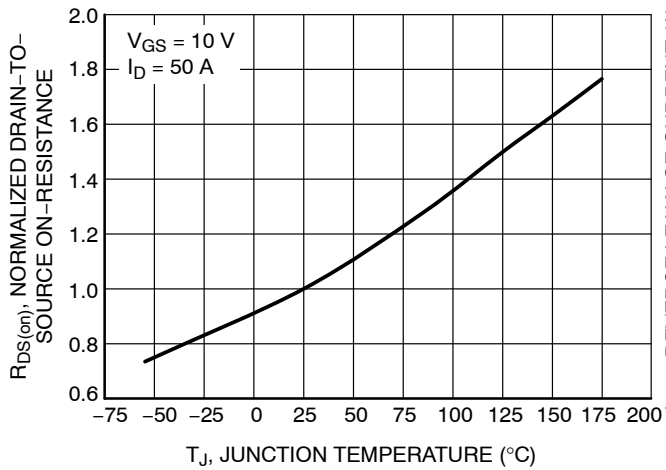


Figure 5. On-Resistance Variation with Temperature

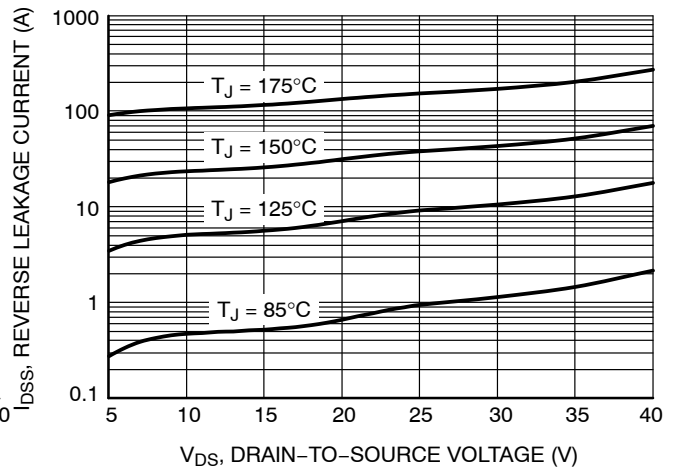


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

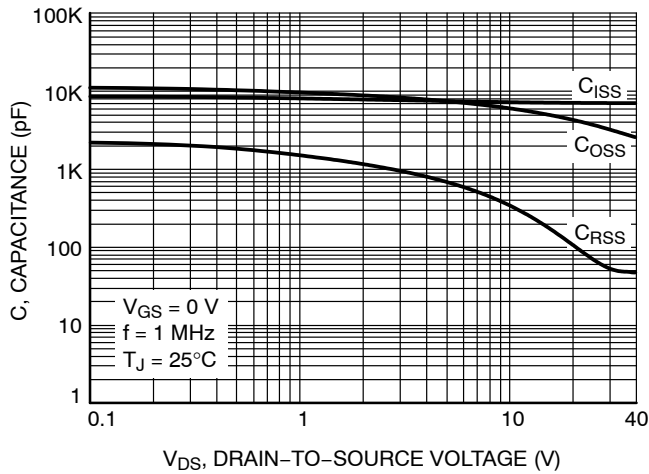


Figure 7. Capacitance Variation

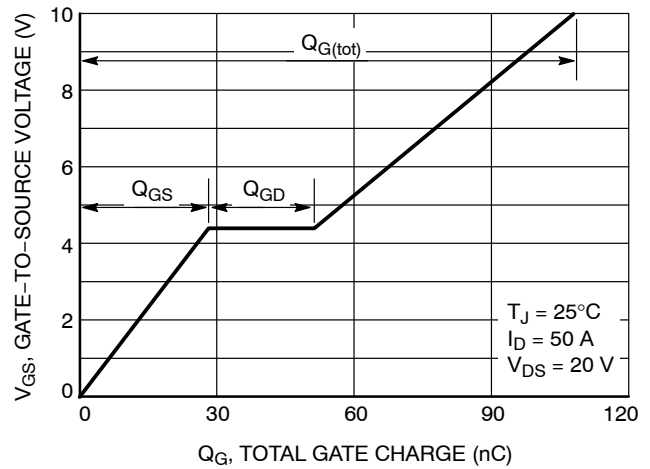


Figure 8. Gate-to-Source Voltage vs. Total Charge

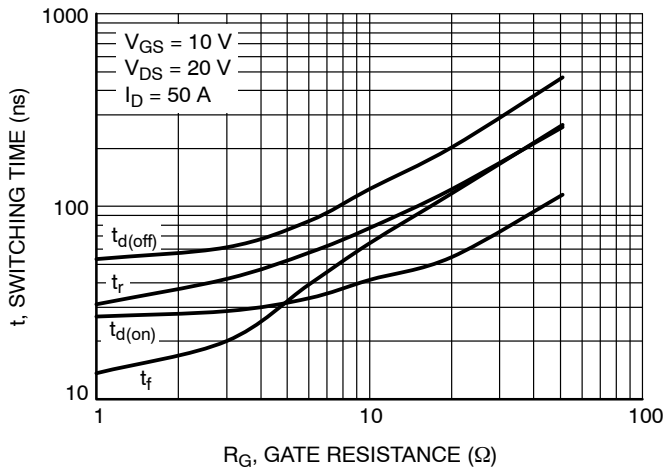


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

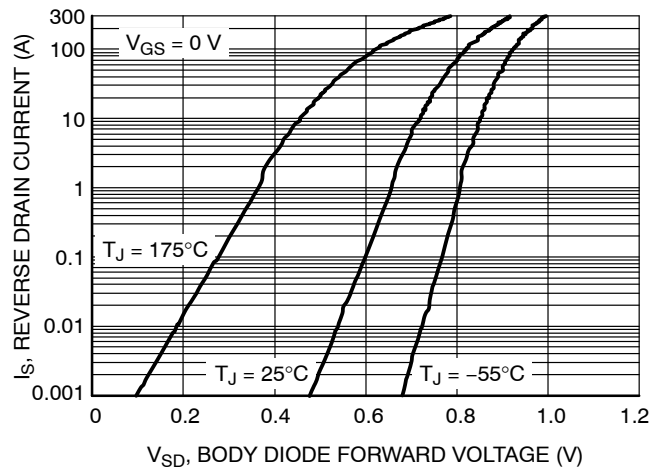


Figure 10. Diode Forward Voltage vs. Current

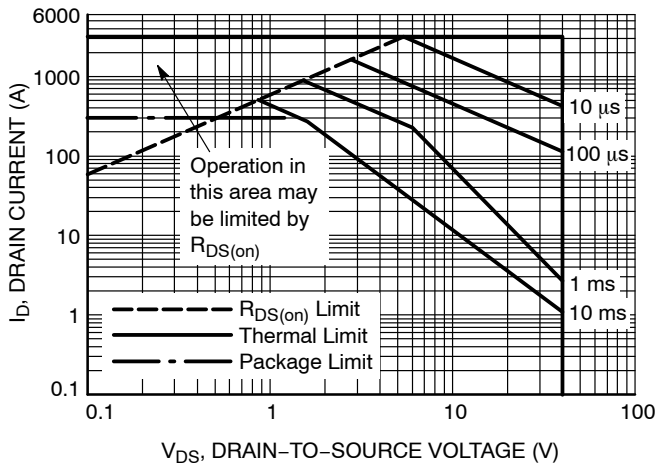


Figure 11. Maximum Rated Forward Biased Safe Operating Area

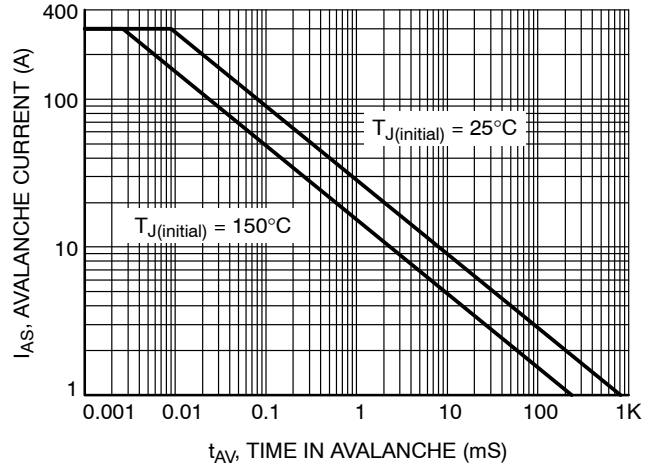


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

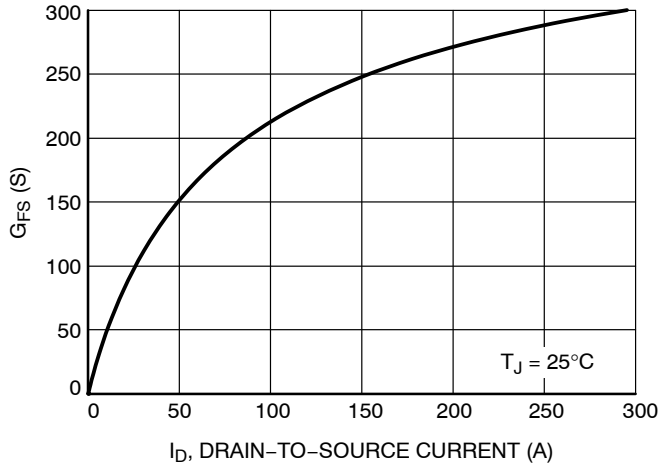


Figure 13. G_{FS} vs. I_D

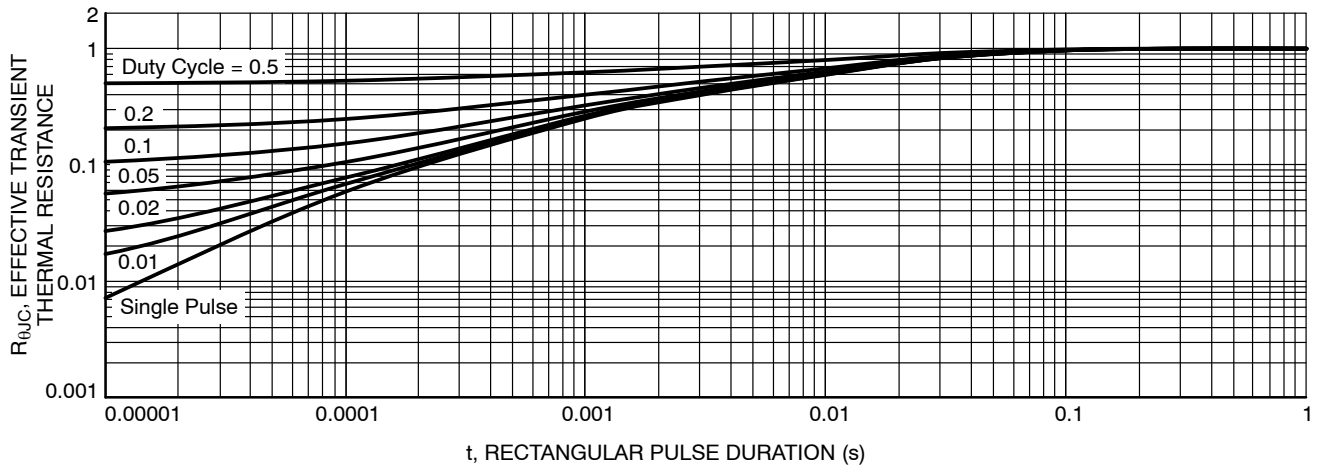


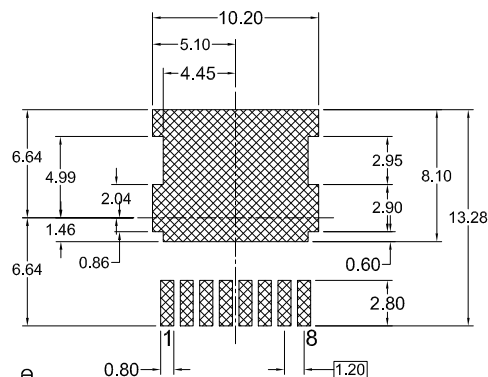
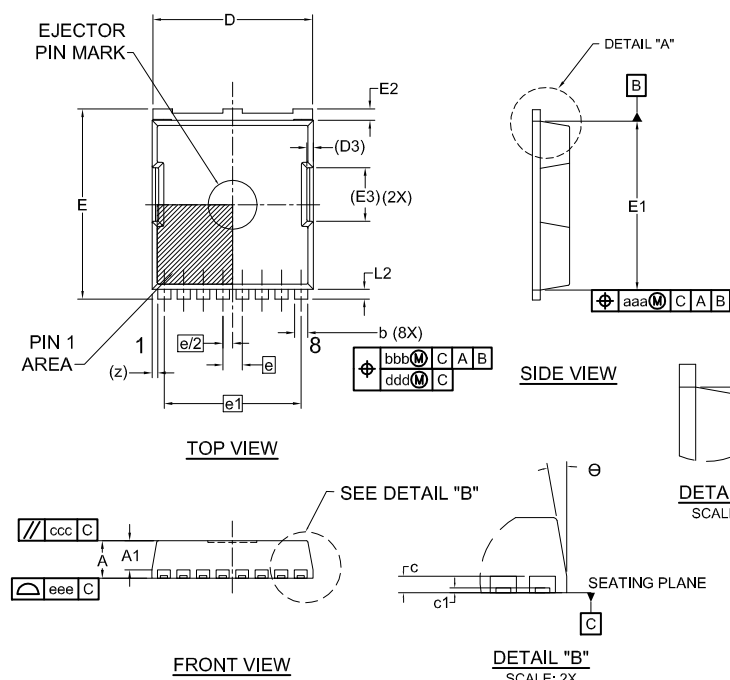
Figure 14. Transient Thermal Impedance

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



H-PSOF8L 11.68x9.80 CASE 100CU ISSUE B

DATE 20 MAY 2022



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

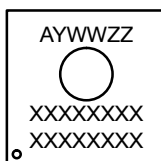
NOTES:

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	8.00 REF		
c	0.40	0.50	0.60
c1	0.10	---	---
D	9.70	9.80	9.90
D1	9.80	9.90	10.00
D2	4.73 BSC		
D3	0.40 REF		
D4	3.75 BSC		
D5	---	1.20	---
D6	7.40	7.50	7.60
D7	8.30 REF		
E	11.58	11.68	11.78
E1	10.28	10.38	10.48
E2	0.60	0.70	0.80
E3	3.30 REF		
E4	---	2.60	---
E5	---	3.30	---

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E6	---	0.65	---
E7	7.15 REF		
E8	6.55	6.65	6.75
E9	5.89 BSC		
E10	5.19 BSC		
E11	0.10 REF		
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
K	2.43	2.53	2.63
L	1.90	2.00	2.10
L2	0.50	0.60	0.70
z	0.35 REF		
θ	0°	---	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON13813G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	H-PSOF8L 11.68x9.80	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative