

FDMC8010

MOSFET – N-Channel, POWERTRENCH® 30 V, 75 A, 1.3 mΩ

General Description

This N-Channel MOSFET is produced using ON Semiconductor's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance. This device is well suited for applications where ultra low $r_{DS(on)}$ is required in small spaces such as High performance VRM, POL and Oring functions.

Features

- Max $r_{DS(on)}$ = 1.3 mΩ at V_{GS} = 10 V, I_D = 30 A
- Max $r_{DS(on)}$ = 1.8 mΩ at V_{GS} = 4.5 V, I_D = 25 A
- High Performance Technology for Extremely Low $r_{DS(on)}$
- These Devices are Pb-Free and are RoHS Compliant

Applications

- DC – DC Buck Converters
- Point of Load
- High Efficiency Load Switch and Low Side Switching
- Oring FET

MOSFET MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 4)	±20	V
I_D	Drain Current –Continuous (Package limited) T_C = 25°C –Continuous (Silicon limited) T_C = 25°C –Continuous T_A = 25°C (Note 1a) –Pulsed	75 166 30 120	A
EAS	Single Pulse Avalanche Energy (Note 3)	153	mJ
P_D	Power Dissipation T_C = 25°C Power Dissipation T_A = 25°C (Note 1a)	54 2.4	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

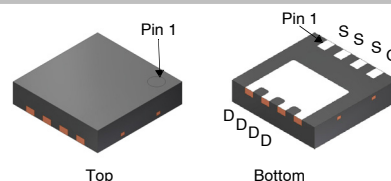
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	°C/W



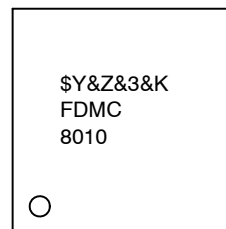
ON Semiconductor®

www.onsemi.com

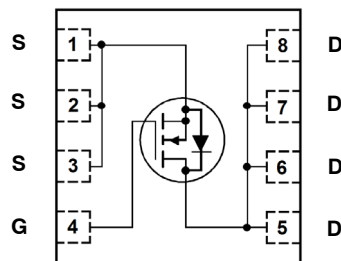


PQFN8 3.3x3.3, 0.65P
CASE 483AW
Power 33

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
FDMC8010 = Specific Device Code



ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 2 of this data sheet.

FDMC8010

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8010	FDMC8010	Power 33	13"	12 mm	3000 Units

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
--------	-----------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0 V	30			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, referenced to 25°C		15		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = 20 V, V _{DS} = 0 V			100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 1 mA	1.2	1.5	2.5	V
ΔV _{GS(th)} /ΔT _J	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 1 mA, referenced to 25°C		-5		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 30 A		0.9	1.3	mΩ
		V _{GS} = 4.5 V, I _D = 25 A		1.3	1.8	
		V _{GS} = 10 V, I _D = 30 A, T _J = 125°C		1.3	2	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 30 A		188		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		4405	5860	pF
C _{oss}	Output Capacitance			1570	2090	pF
C _{rss}	Reverse Transfer Capacitance			167	250	pF
R _g	Gate Resistance		0.1	0.5	1.25	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 15 V, I _D = 30 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		15	27	ns
t _r	Rise Time			7.5	15	ns
t _{d(off)}	Turn-Off Delay Time			40	64	ns
t _f	Fall Time			5.3	11	ns
Q _g	Total Gate Charge	V _{GS} = 0 V to 10 V	V _{DD} = 15 V I _D = 30 A	67	94	nC
Q _g	Total Gate Charge	V _{GS} = 0 V to 4.5 V		32	45	nC
Q _{gs}	Gate to Source Charge			10		nC
Q _{gd}	Gate to Drain "Miller" Charge			9.5		nC

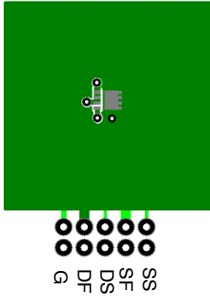
DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2 A (Note 2)		0.6	1.2	V
		V _{GS} = 0 V, I _S = 30 A (Note 2)		0.7	1.2	
t _{rr}	Reverse Recovery Time	I _F = 30 A, di/dt = 100 A/μs		49	78	ns
Q _{rr}	Reverse Recovery Charge			29	46	nC

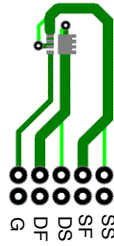
FDMC8010

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0 %.
3. E_{AS} of 153 mJ is based on starting $T_J = 25$ °C, $L = 0.3$ mH, $I_{AS} = 32$ A, $V_{DD} = 27$ V, $V_{GS} = 10$ V. 100% test at $L = 0.1$ mH, $I_{AS} = 47$ A.
4. As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS

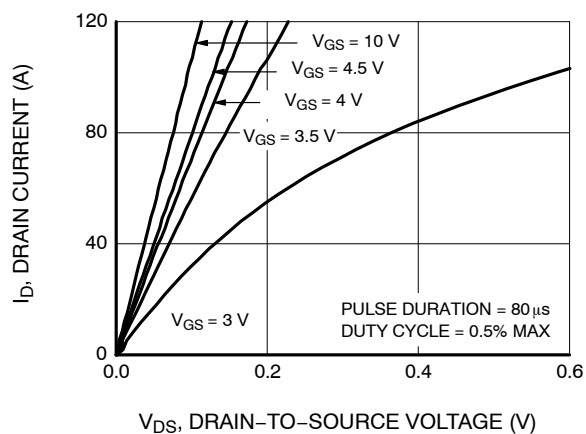
 $T_J = 25^\circ\text{C}$ Unless Otherwise Noted

Figure 1. On-Region Characteristics

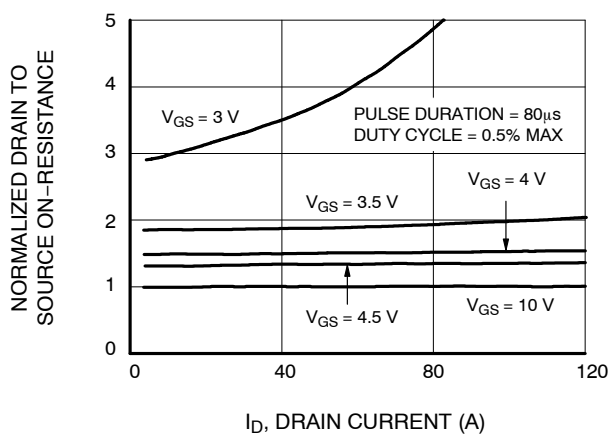


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

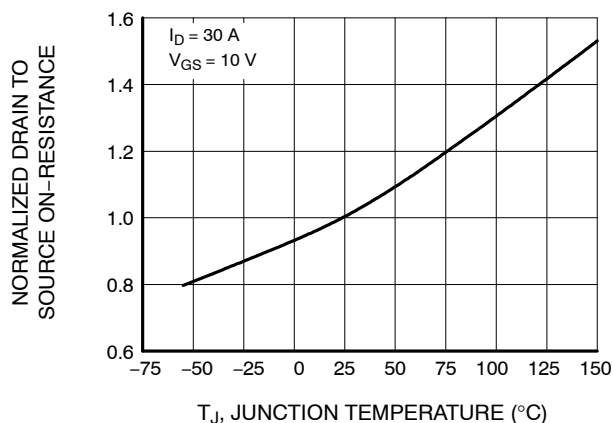


Figure 3. Normalized On Resistance vs Junction Temperature

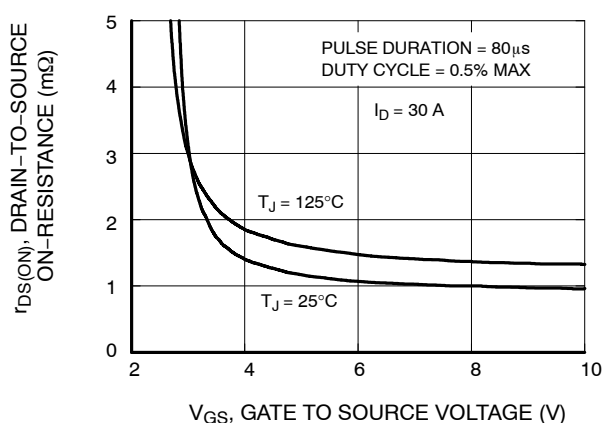


Figure 4. On-Resistance vs Gate to Source Voltage

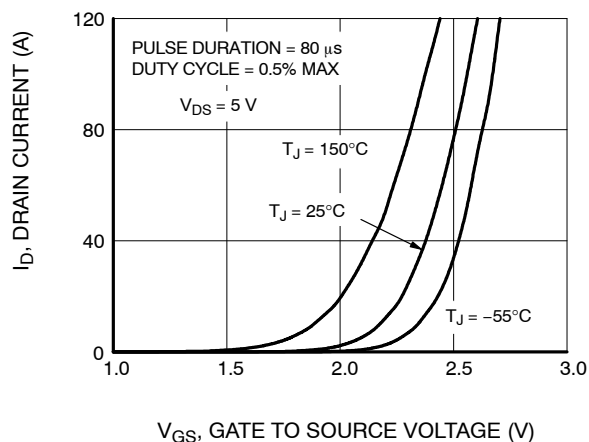


Figure 5. Transfer Characteristics

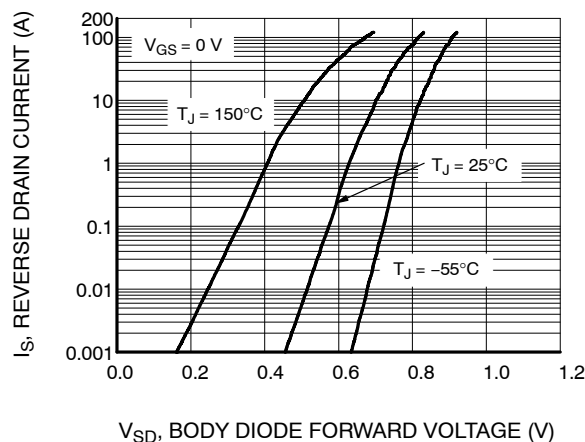


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (continued)

$T_J = 25^\circ\text{C}$ Unless Otherwise Noted

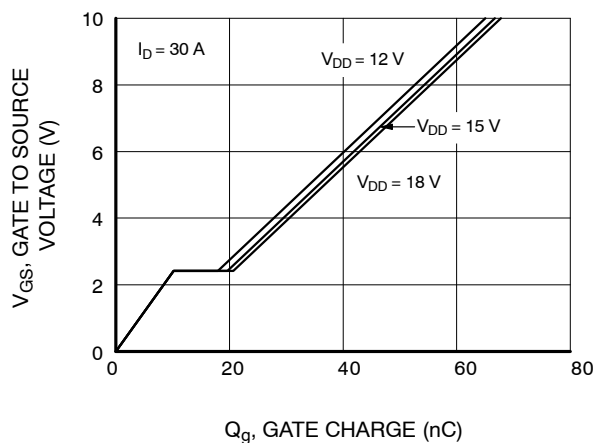


Figure 7. Gate Charge Characteristics

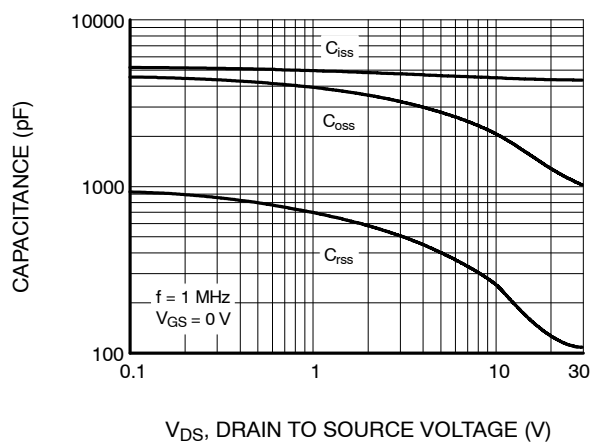


Figure 8. Capacitance vs Drain to Source Voltage

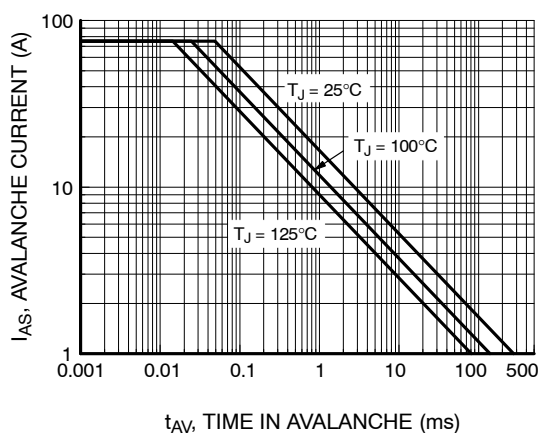


Figure 9. Unclamped Inductive Switching Capability

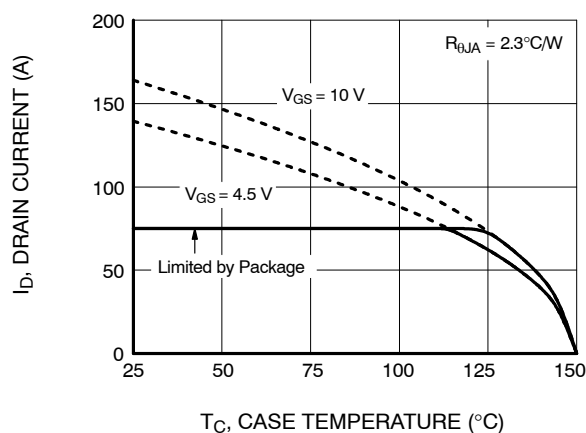


Figure 10. Maximum Continuous Drain Current vs Case Temperature

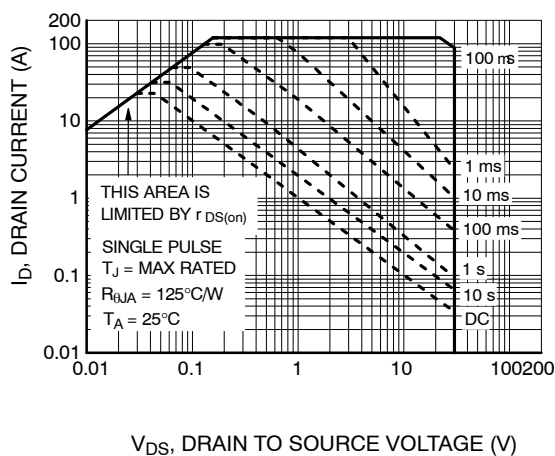


Figure 11. Forward Bias Safe Operating Area

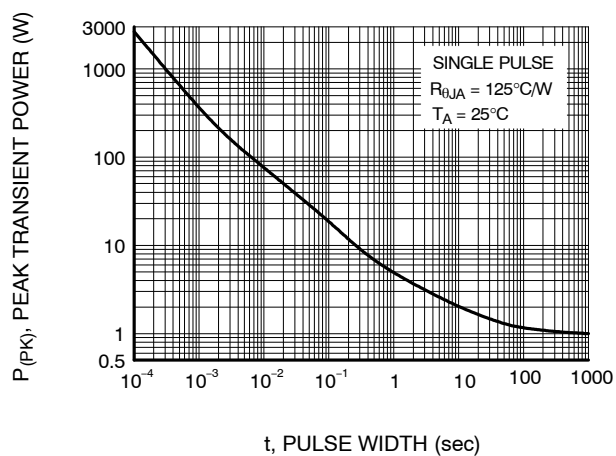


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

$T_J = 25^\circ\text{C}$ Unless Otherwise Noted

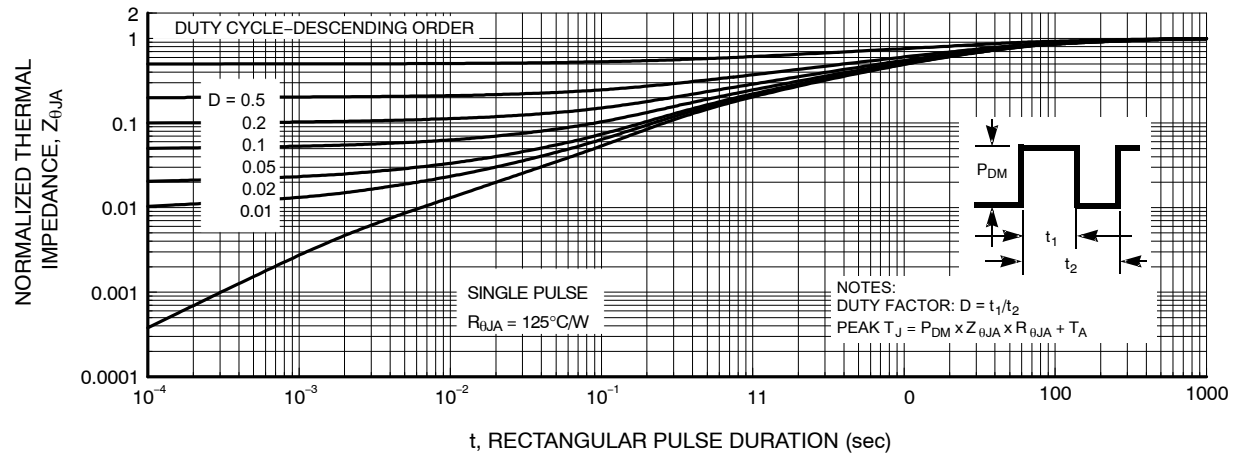
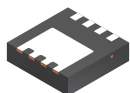


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

MECHANICAL CASE OUTLINE

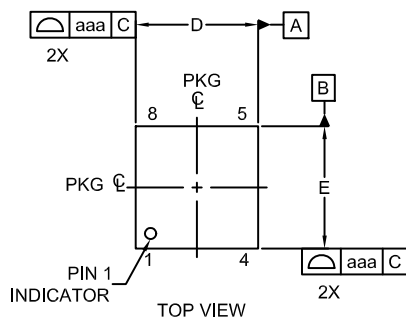
PACKAGE DIMENSIONS

ON Semiconductor®

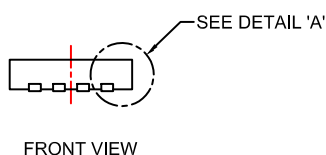


WDFN8 3.3X3.3, 0.65P
CASE 483AW
ISSUE A

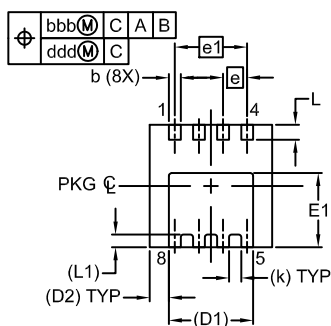
DATE 10 SEP 2019



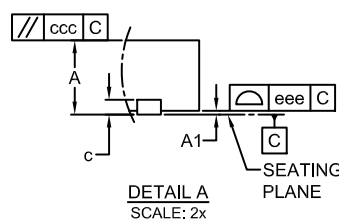
TOP VIEW



FRONT VIEW

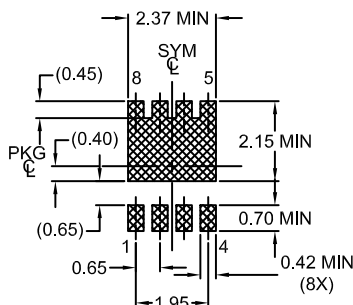


BOTTOM VIEW



DETAIL A
SCALE: 2x

LAND PATTERN RECOMMENDATION*



*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR
SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	-	0.05
b	0.27	0.32	0.37
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.27 REF		
D2	0.52 REF		
E	3.20	3.30	3.40
E1	1.85	1.95	2.05
e	0.65 BSC		
e1	1.95 BSC		
k	0.33 REF		
L	0.30	0.40	0.50
L1	0.34 REF		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON13672G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	WDFN8 3.3X3.3, 0.65P	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative