MOSFET – N-Channel, SUPREMOS

600 V, 22 A, 165 mΩ

FCH22N60N

Description

The SUPREMOS® MOSFET is ON Semiconductor's next generation of high voltage super−junction (SJ) technology employing a deep trench filling process that differentiates it from the conventional SJ MOSFETs. This advanced technology and precise process control provides lowest Rsp on−resistance, superior switching performance and ruggedness. SUPREMOS MOSFET is suitable for high frequency switching power converter applications such as PFC, server/telecom power, FPD TV power, ATX power, and industrial power applications.

Features

- 650 V @ $T_J = 150°C$
- $R_{DS(on)} = 140$ mΩ (Typ.) @ $V_{GS} = 10$ V, $I_D = 11$ A
- Ultra Low Gate Charge (Typ. $Q_g = 45$ nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 196.4$ pF)
- 100% Avalanche Tested
- This Device is Pb−Free and is RoHS Compliant

Applications

- PDP TV
- Solar Inverter
- AC−DC Power Supply

ON Semiconductor®

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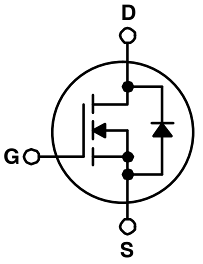
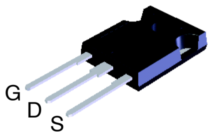
V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
600 V	165 mΩ @ 10 V	22 A

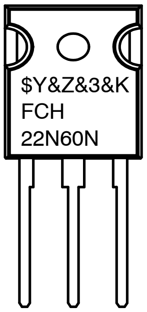


N-CHANNEL MOSFET



TO−247−3LD
CASE 340CK

MARKING DIAGRAM



$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
FCH22N60N = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

October, 2020 − Rev. 3

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FCH22N60N	Unit
V_{DSS}	Drain to Source Voltage		600	V
V_{GSS}	Gate to Source Voltage		±30	V
I_D	Drain Current	– Continuous (T_C = 25°C)	22	A
		– Continuous (T_C = 100°C)	13.8	
I_{DM}	Drain Current	– Pulsed (Note 1)	66	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		672	mJ
I_{AR}	Avalanche Current (Note 1)		7.3	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		2.75	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	(T_C = 25°C)	205	W
		– Derate above 25°C	1.64	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to + 150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 Second		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. I_{AS} = 7.3 A, R_G = 25 Ω, starting T_J = 25 °C
3. $I_{SD} \leq$ 22 A, di/dt ≤ 200 A/s, $V_{DD} \leq$ 380 V, starting T_J = 25 °C

THERMAL CHARACTERISTICS

Symbol	Parameter	FCH22N60N	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.61	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Package Method	Reel Size	Tape Width	Quantity
FCH22N60N	FCH22N60N	TO−247−3LD	Tube	N/A	N/A	30 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V, T_J = 25°C	600	–	–	V
		I_D = 1 mA, V_{GS} = 0 V, T_J = 150°C	650	–	–	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	–	0.68	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 480 V, V_{GS} = 0 V	–	–	10	μA
		V_{DS} = 480 V, T_J = 125°C	–	–	100	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±50 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	3	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 11 A	–	0.140	0.165	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 11 A	–	22	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	–	1950	–	pF
C_{oss}	Output Capacitance		–	75.9	–	pF
C_{rss}	Reverse Transfer Capacitance		–	3	–	pF
C_{oss}	Output Capacitance	V_{DS} = 380 V, V_{GS} = 0 V, f = 1 MHz	–	43.2	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	–	196.4	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 380 V, I_D = 11 A, V_{GS} = 10 V (Note 4)	–	45	–	nC
Q_{gs}	Gate to Source Gate Charge		–	8.7	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	14.5	–	nC
ESR	Equivalent Series Resistance(G–S)	f = 1 MHz	–	1	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 380 V, I_D = 11 A, R_G = 4.7 Ω (Note 4)	–	16.9	–	ns
t_r	Turn–On Rise Time		–	16.7	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	49	–	ns
t_f	Turn–Off Fall Time		–	4	–	ns
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	22	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	66	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 11 A	–	–	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 11 A, dI_F/dt = 100 A/μs	–	350	–	ns
Q_{rr}	Reverse Recovery Charge		–	6	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially Independent of Operating Temperature Typical Characteristics.

TYPICAL CHARACTERISTICS

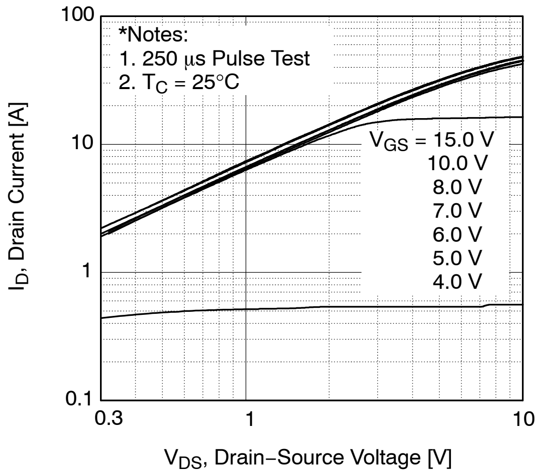


Figure 1. On−Region Characteristics

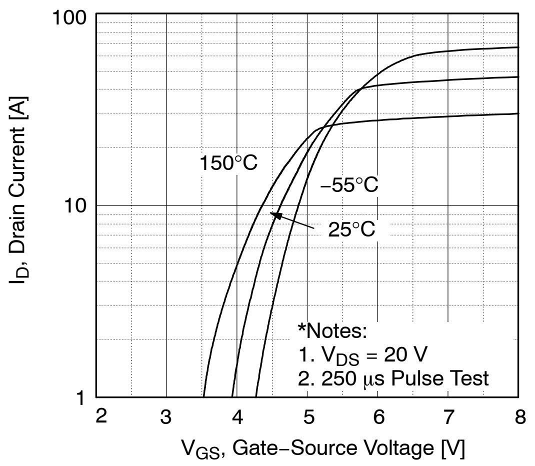


Figure 2. Transfer Characteristics

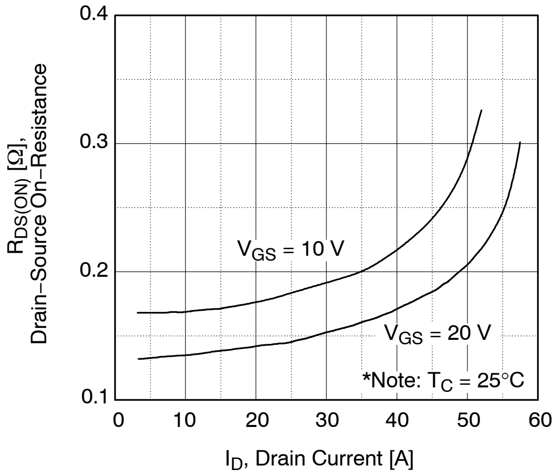


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

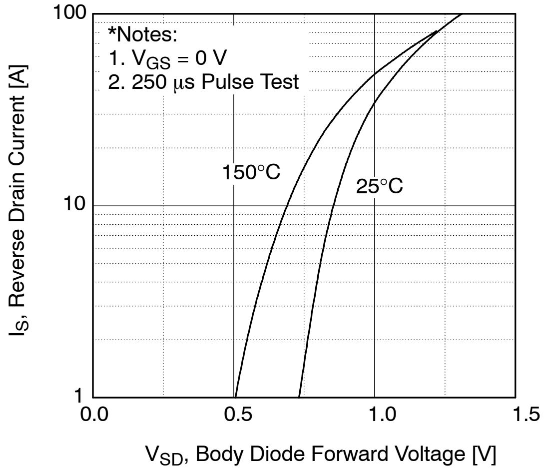


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

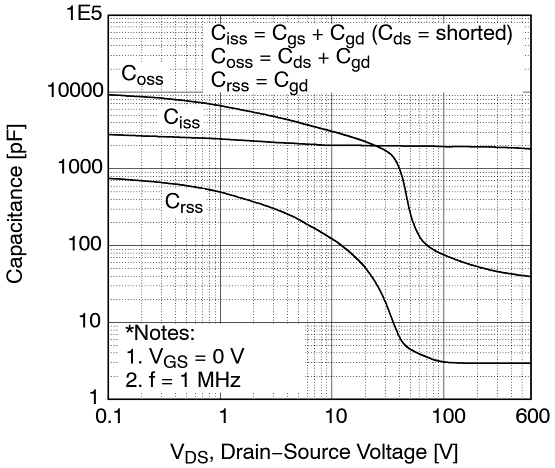


Figure 5. Capacitance Characteristics

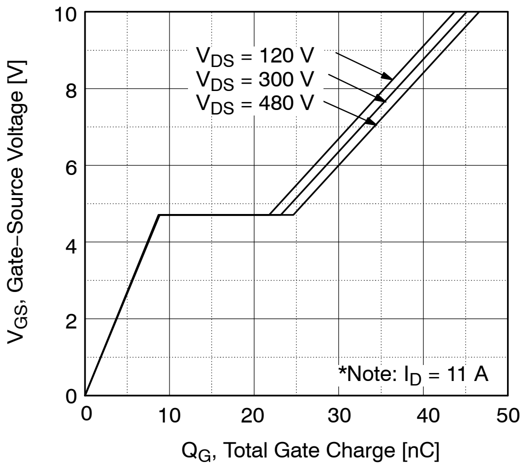
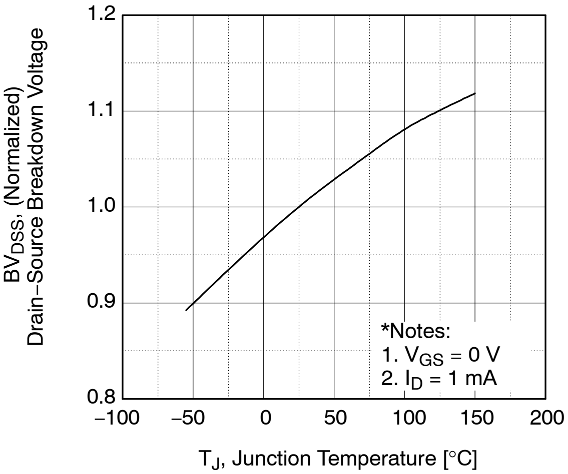


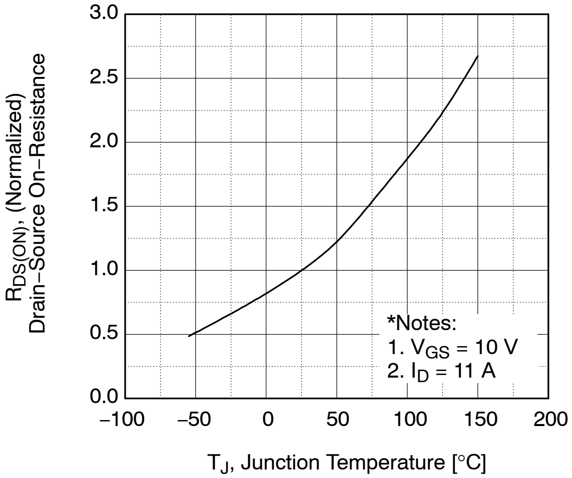
Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)



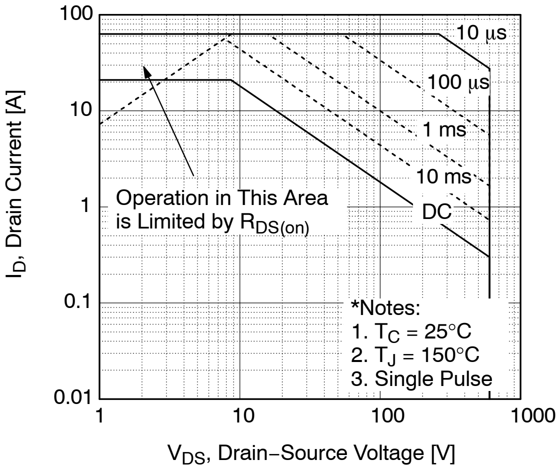
*Notes:
1. V_{GS} = 0 V
2. I_D = 1 mA

Figure 7. Breakdown Voltage Variation vs. Temperature



*Notes:
1. V_{GS} = 10 V
2. I_D = 11 A

Figure 8. On−Resistance Variation vs. Temperature



*Notes:
1. T_C = 25°C
2. T_J = 150°C
3. Single Pulse

Figure 9. Maximum Safe Operating Area

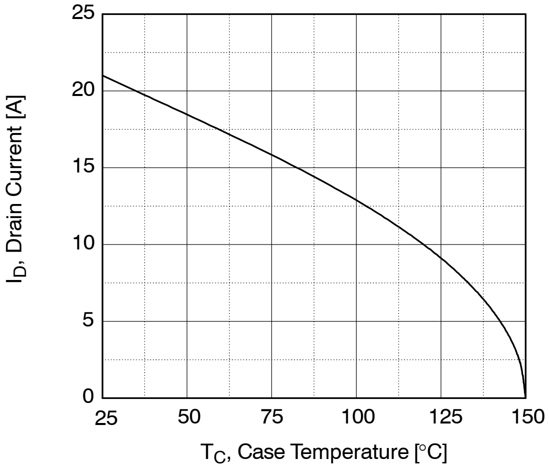
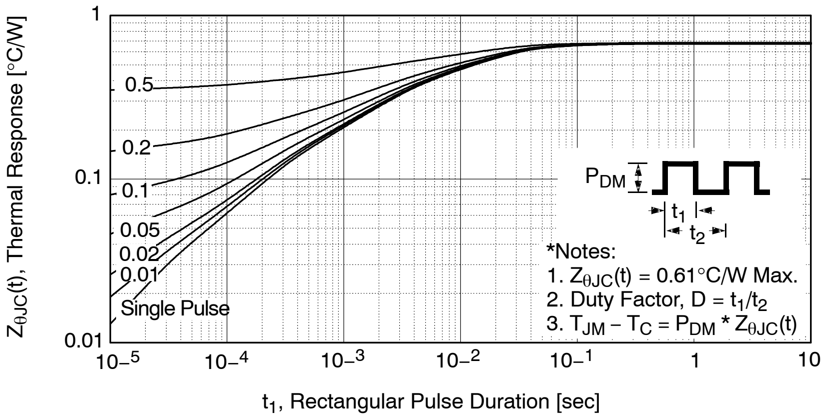


Figure 10. Maximum Drain Current vs. Case Temperature



*Notes:
1. $Z_{\theta JC}(t)$ = 0.61°C/W Max.
2. Duty Factor, $D = t_1/t_2$
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$

Figure 11. Transient Thermal Response Curve

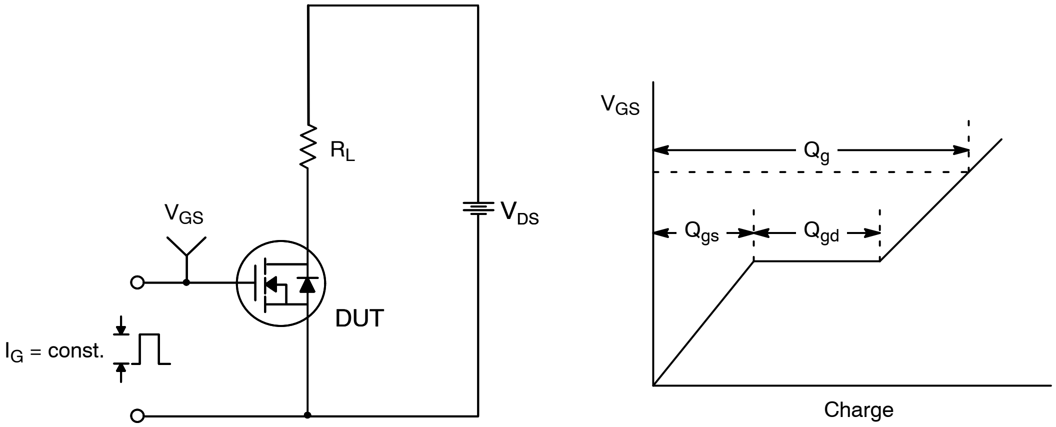


Figure 12. Gate Charge Test Circuit & Waveform

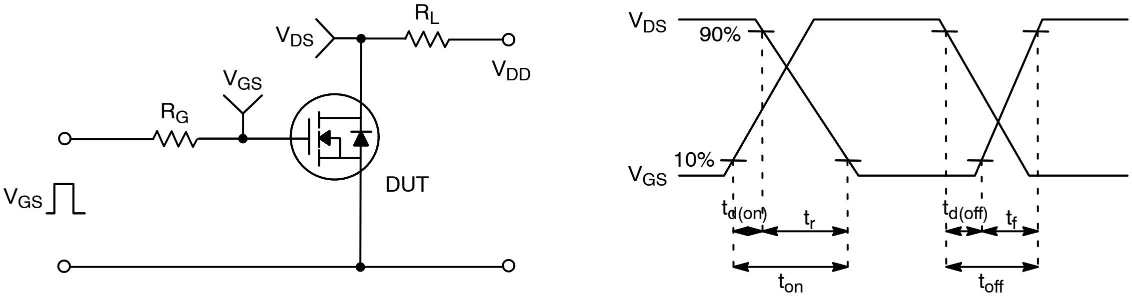


Figure 13. Resistive Switching Test Circuit & Waveforms

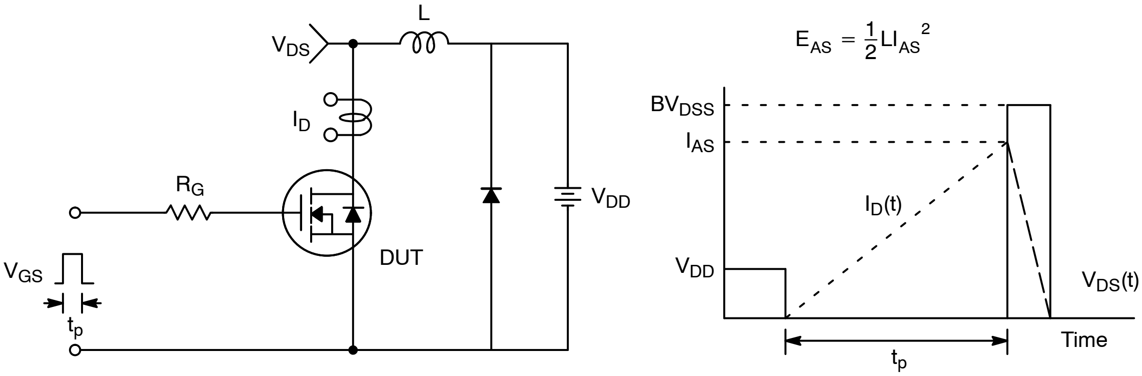
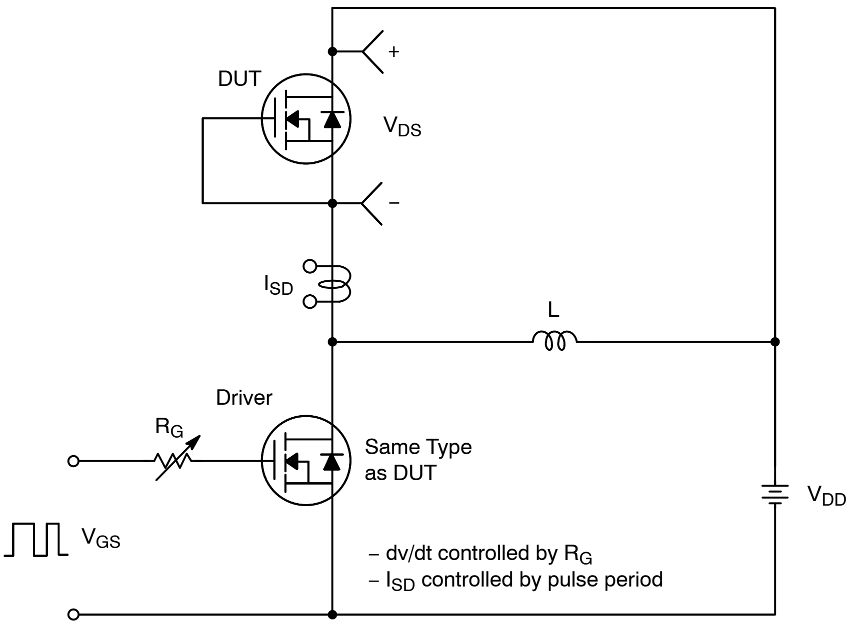


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



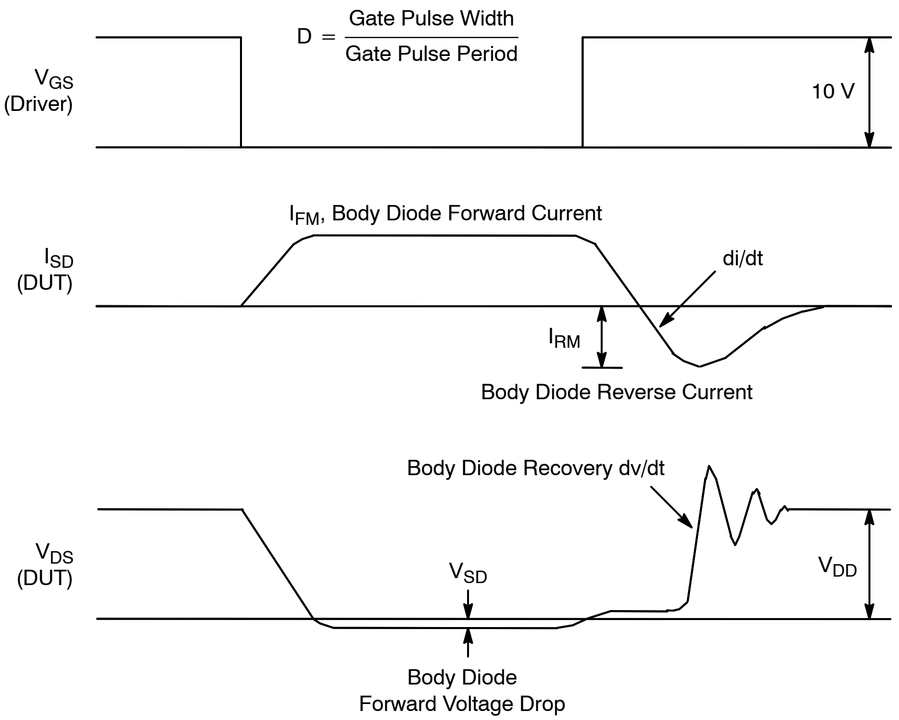


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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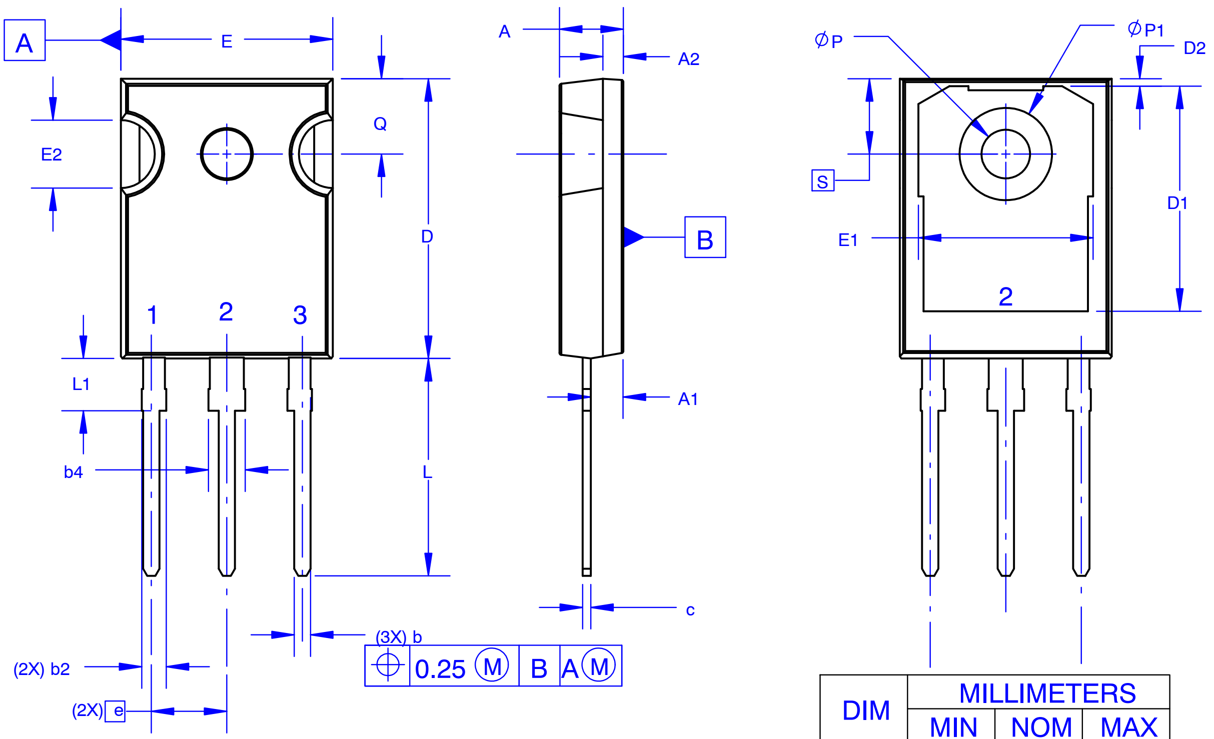
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−247−3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*

AYWWZZ
XXXXXXX
XXXXXXX
∘

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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