

# MOSFET - Power, N-Channel, SUPERFET® III, FRFET®

650 V, 24 A, 150 mΩ

## NTMT150N65S3HF

### Description

SUPERFET III MOSFET is onsemi's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power systems for miniaturization and higher efficiency.

SUPERFET III FRFET MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

The TDFN4 package is an ultra-slim surface-mount package (1 mm high) with a low profile and small footprint (8x8 mm<sup>2</sup>). SUPERFET III MOSFET in a TDFN4 package offers excellent switching performance due to lower parasitic source inductance and separated power and drive sources. TDFN4 offers Moisture Sensitivity Level 1 (MSL 1).

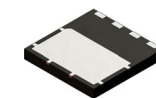
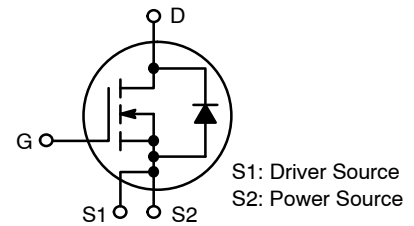
### Features

- 700 V @ T<sub>J</sub> = 150°C
- Typ. R<sub>DS(on)</sub> = 121 mΩ
- Ultra Low Gate Charge (Typ. Q<sub>g</sub> = 43 nC)
- Low Effective Output Capacitance (Typ. C<sub>oss(eff.)</sub> = 400 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

### Applications

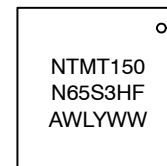
- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar
- Lighting

V <sub>DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
650 V	150 mΩ @ 10 V	24 A



TDFN4 8X8  
CASE 520AB

### MARKING DIAGRAM



NTMT150N65S3HF = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# NTMT150N65S3HF

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , Unless otherwise noted)

Symbol	Parameter		Value	Unit
$V_{DSS}$	Drain to Source Voltage		650	V
$V_{GSS}$	Gate to Source Voltage	– DC	$\pm 30$	V
		– AC ( $f > 1\text{ Hz}$ )	$\pm 30$	
$I_D$	Drain Current	– Continuous ( $T_C = 25^\circ\text{C}$ )	24	A
		– Continuous ( $T_C = 100^\circ\text{C}$ )	15.2	
$I_{DM}$	Drain Current	– Pulsed (Note 1)	60	A
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)		275	mJ
$I_{AS}$	Avalanche Current (Note 2)		3.8	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)		1.92	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	192	W
		– Derate Above $25^\circ\text{C}$	1.54	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range		–55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $I_{AS} = 3.8\text{ A}$ ,  $R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 12\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 400\text{ V}$ , starting  $T_J = 25^\circ\text{C}$ .

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.65	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max., (Note 4)	45	

4. Device on 1 in<sup>2</sup> 2-oz copper pad on 1.5 x 1.5 in. board of FR-4 material.

## PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Reel Size	Tape Width	Shipping <sup>†</sup>
NTMT150N65S3HF	NTMT150N65S3HF	TDFN4	13"	13.3 mm	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTMT150N65S3HF

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA, T <sub>J</sub> = 25°C	650			V
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA, T <sub>J</sub> = 150°C	700			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 10 mA, Referenced to 25°C		0.62		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V			10	μA
		V <sub>DS</sub> = 520 V, T <sub>C</sub> = 125°C		10		
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V			±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 0.54 mA	3.0		5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A		121	150	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 12 A		14		S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, f = 1 MHz		1985		pF
C <sub>oss</sub>	Output Capacitance			40		pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V		400		pF
C <sub>oss(er.)</sub>	Energy Related Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V		71		pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10 V	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 12 A, V <sub>GS</sub> = 10 V (Note 5)		43		nC
Q <sub>gs</sub>	Gate to Source Gate Charge			13		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge			17		nC
ESR	Equivalent Series Resistance	f = 1 MHz		3.1		Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 12 A, V <sub>GS</sub> = 10 V R <sub>g</sub> = 4.7 Ω (Note 5)		24		ns
t <sub>r</sub>	Turn-On Rise Time			12		ns
t <sub>d(off)</sub>	Turn-Off Delay Time			60		ns
t <sub>f</sub>	Turn-Off Fall Time			3.1		ns

### SOURCE-DRAIN DIODE CHARACTERISTICS

I <sub>S</sub>	Maximum Continuous Source to Drain Diode Forward Current			24		A
I <sub>SM</sub>	Maximum Pulsed Source to Drain Diode Forward Current			60		A
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 12 A			1.3	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>DD</sub> = 400 V, I <sub>SD</sub> = 12 A, dI <sub>F</sub> /dt = 100 A/μs		80		ns
Q <sub>rr</sub>	Reverse Recovery Charge			285		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

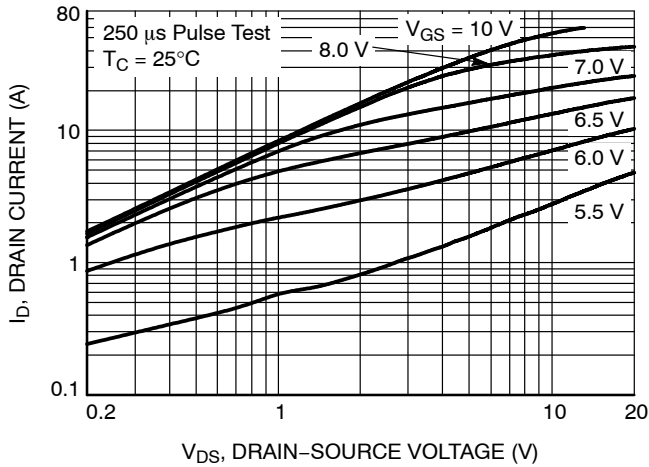


Figure 1. On-Region Characteristics

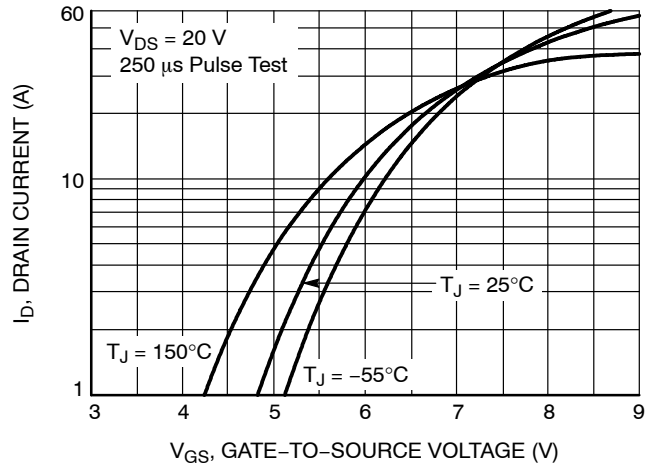


Figure 2. Transfer Characteristics

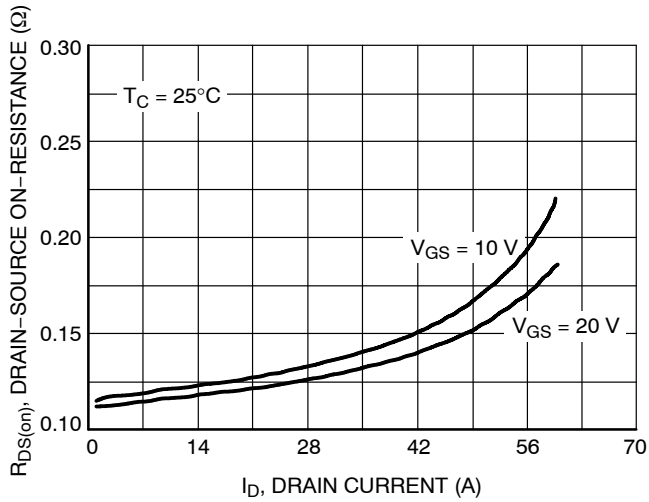


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

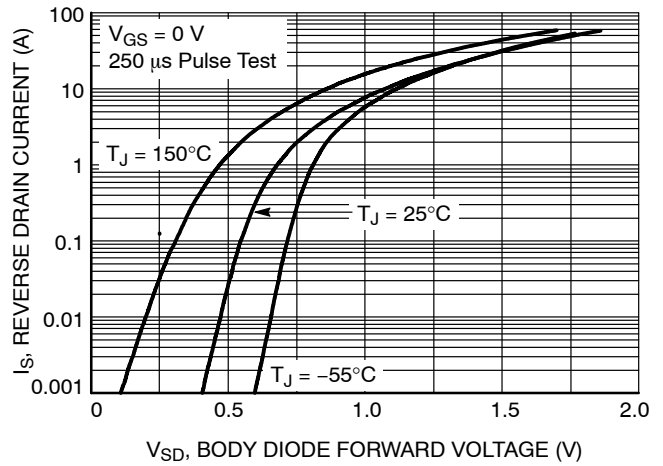


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

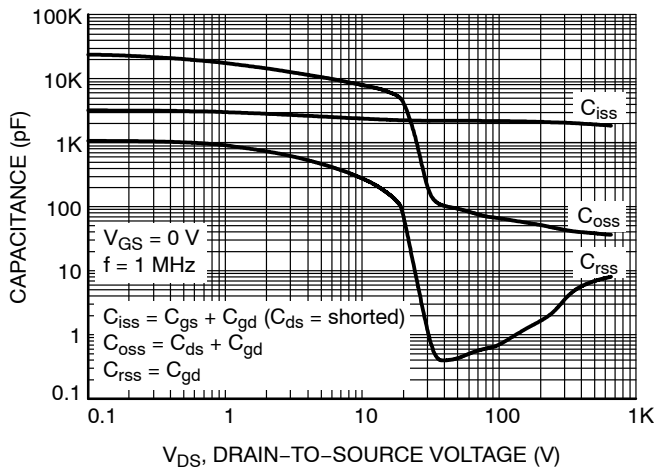


Figure 5. Capacitance Characteristics

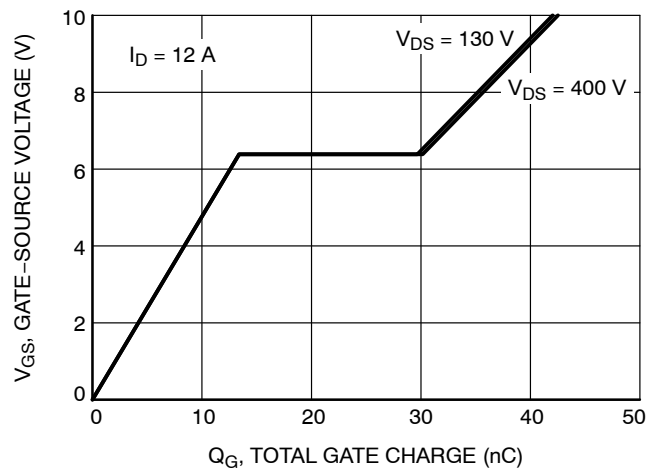


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

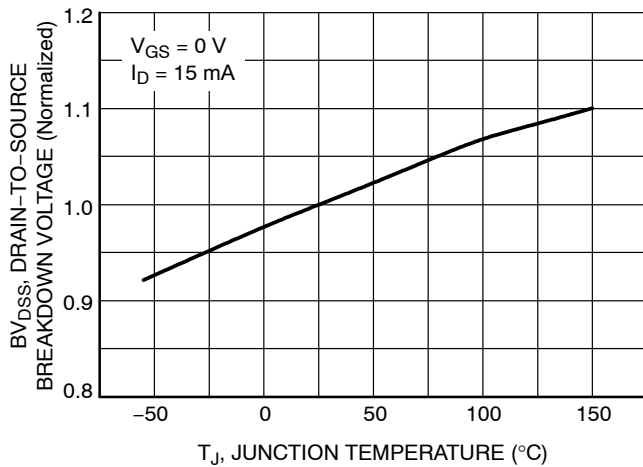


Figure 7. Breakdown Voltage Variation vs. Temperature

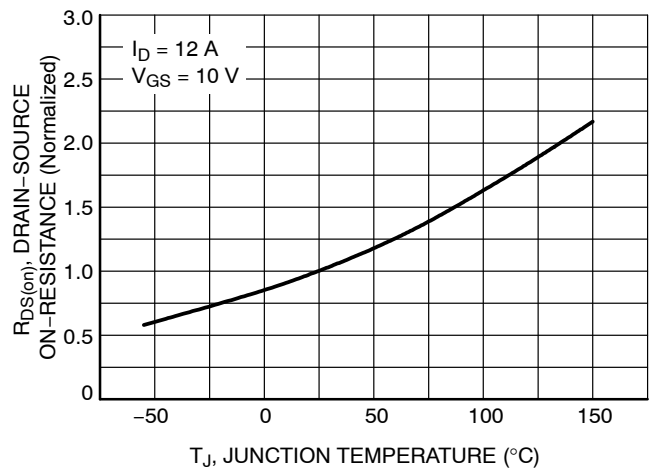


Figure 8. On-Resistance Variation vs. Temperature

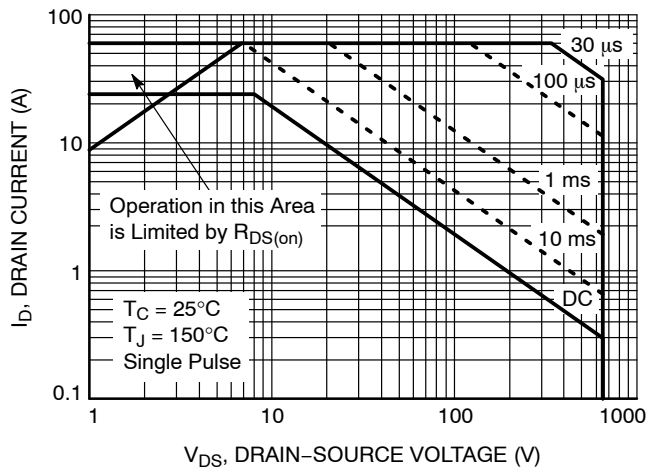


Figure 9. Maximum Safe Operating Area

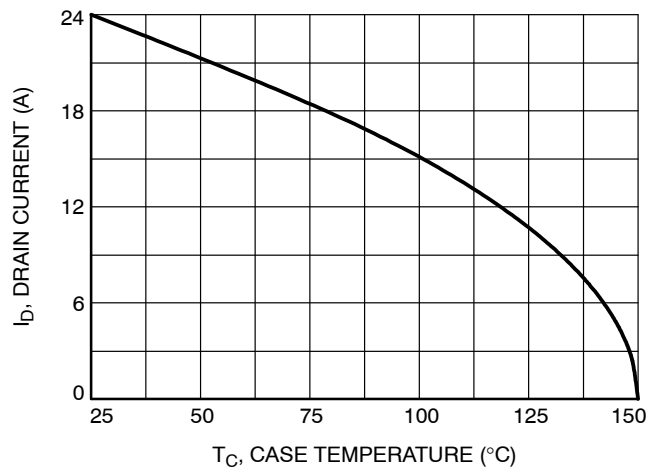


Figure 10. Maximum Drain Current vs. Case Temperature

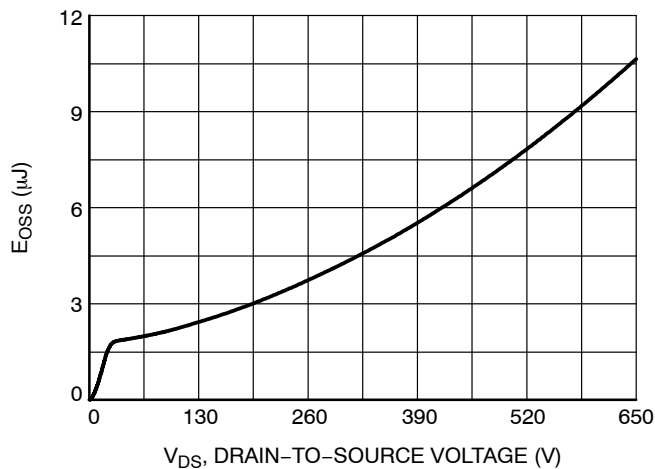


Figure 11.  $E_{OSS}$  vs. Drain-to-Source Voltage

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## TYPICAL CHARACTERISTICS

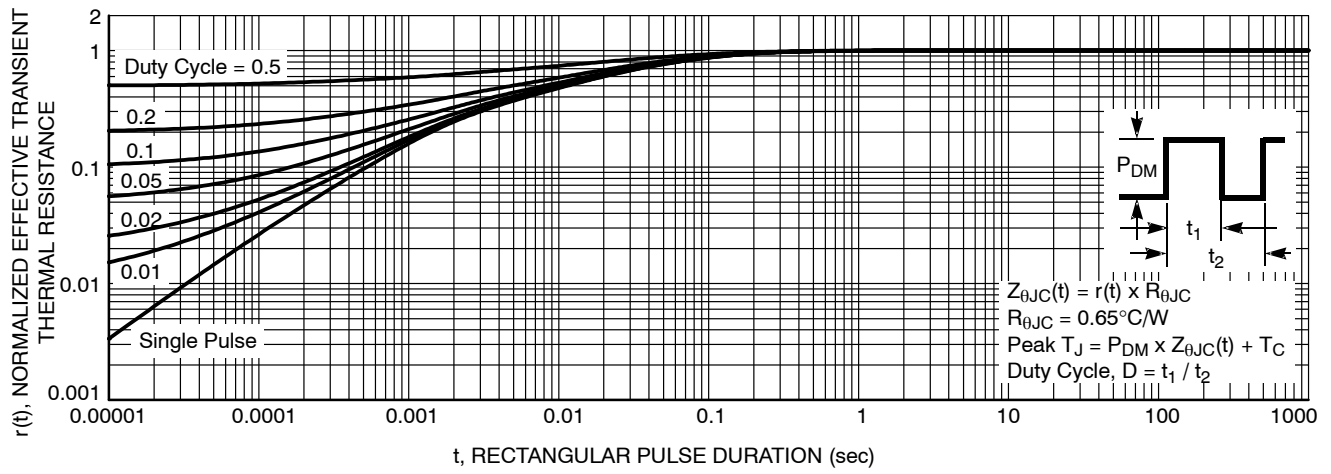


Figure 12. Transient Thermal Response Curve

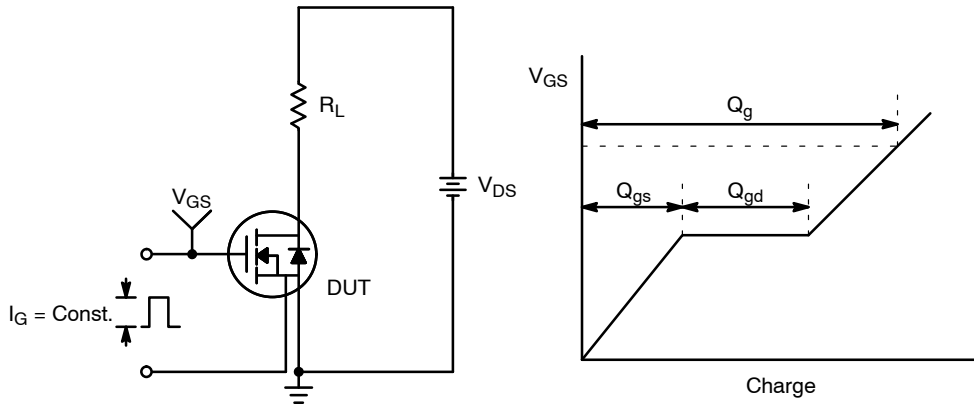


Figure 13. Gate Charge Test Circuit & Waveform

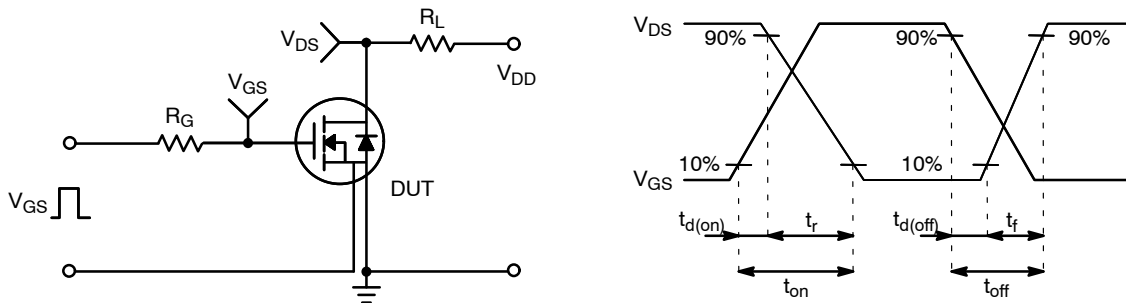


Figure 14. Resistive Switching Test Circuit & Waveforms

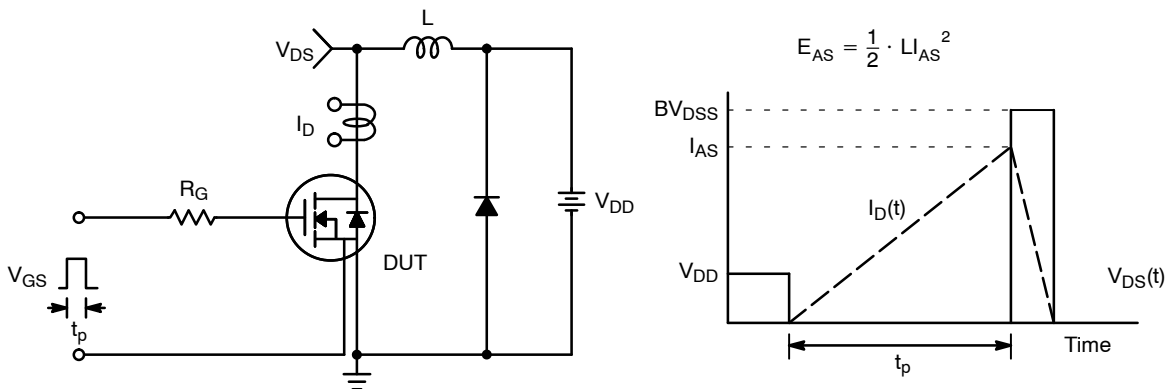
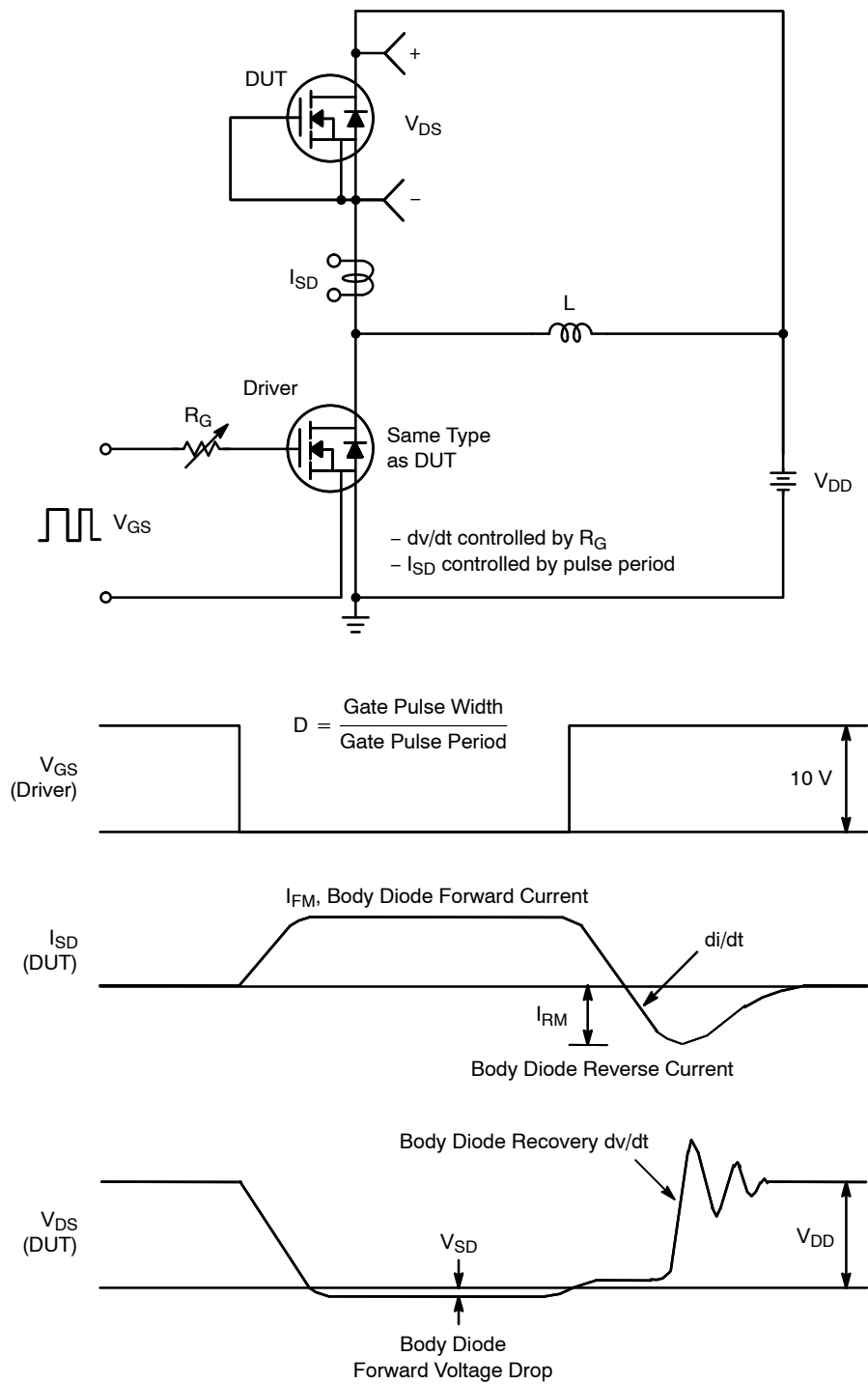


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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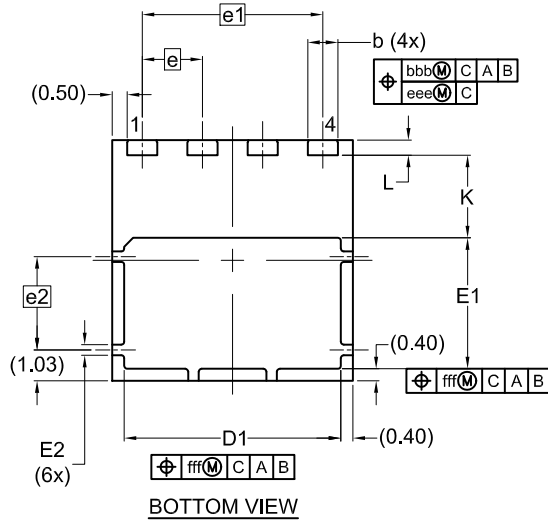
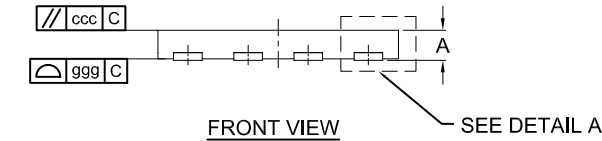
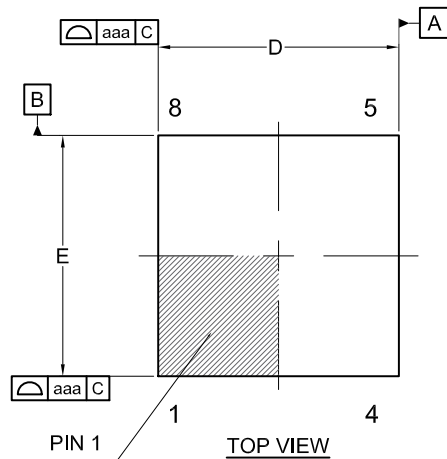


**Figure 16. Peak Diode Recovery  $dV/dt$  Test Circuit & Waveforms**

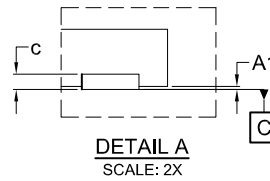
# NTMT150N65S3HF

## PACKAGE DIMENSIONS

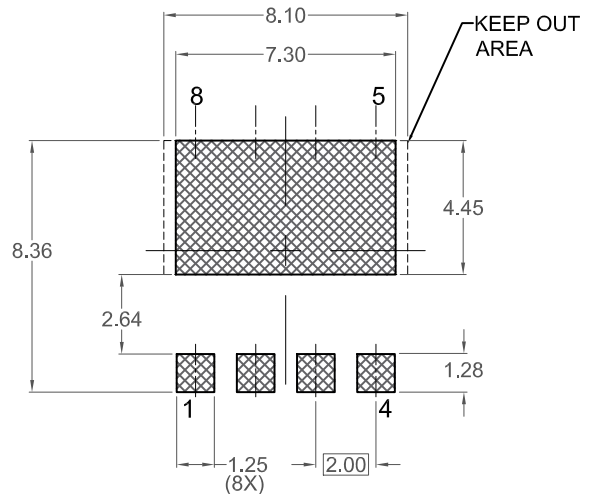
**TDFN4 8x8, 2P**  
CASE 520AB  
ISSUE O



NOTES: UNLESS OTHERWISE SPECIFIED  
A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220.  
B) ALL DIMENSIONS ARE IN MILLIMETERS.  
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.  
D) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.90	1.00	1.10
c	0.10	0.20	0.30
D	7.90	8.00	8.10
D1	7.10	7.20	7.30
E	7.90	8.00	8.10
E1	4.25	4.35	4.45
E2	0.15	0.25	0.35
e	2.00 BSC		
e1	6.00 BSC		
e2	3.10 BSC		
K	(2.75)		
L	0.40	0.50	0.60
aaa	0.10		
bbb	0.10		
ccc	0.05		
eee	0.05		
fff	0.10		
ggg	0.15		



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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