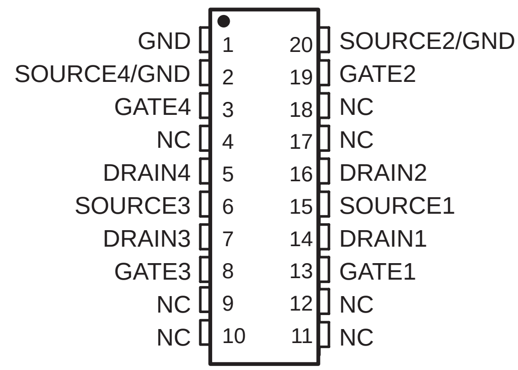
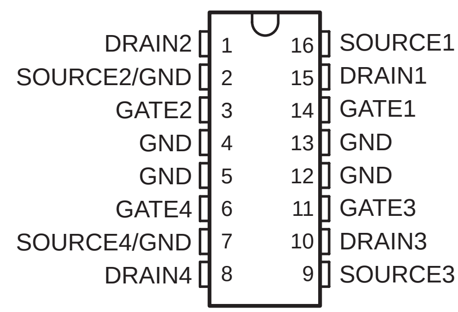
- **Low $r_{DS(on)}$ . . . 0.4 Ω Typ**
- **High-Voltage Output . . . 60 V**
- **Pulsed Current . . . 3 A Per Channel**
- **Fast Commutation Speed**
- **Direct Logic-Level Interface**

DW PACKAGE
(TOP VIEW)



NC − No internal connection

NE PACKAGE
(TOP VIEW)

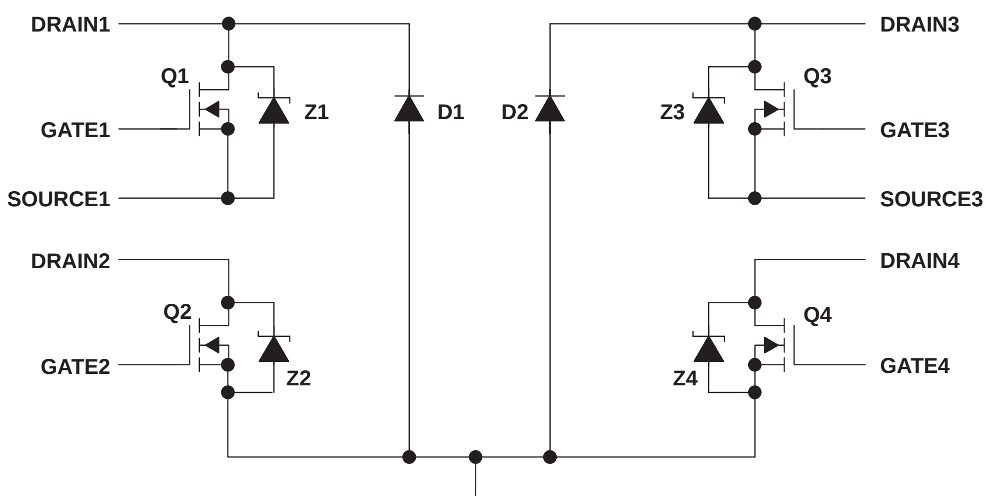


description

The TPIC5424L is a monolithic logic-level power DMOS array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors, two of which are configured with a common source.

The TPIC5424L is offered in a 16-pin thermally enhanced dual-in-line (NE) package and a 20-pin wide-body surface-mount (DW) package. The TPIC5424L is characterized for operation over the case temperature range of −40°C to 125°C.

schematic



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q2, Q4)	60 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, T_C = 25°C	1 A
Continuous source-to-drain diode current, T_C = 25°C	1 A
Pulsed drain current, each output, I_{max}, T_C = 25°C (see Note 1 and Figure 15)	3 A
Single-pulse avalanche energy, E_{AS}, T_C = 25°C (see Figure 4)	180 mJ
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.

DISSIPATION RATING TABLE

PACKAGE	$T_C \leq$ 25°C POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	279 mW
NE	2075 mW	16.6 mW/°C	415 mW

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA,	V_{GS} = 0	60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, See Figure 5	$V_{DS} = V_{GS}$,	1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = 250 µA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 1 A, See Notes 2 and 3	V_{GS} = 5 V,		0.4	0.48	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1 A, V_{GS} = 0 (Z1, Z2, Z3, Z4), See Notes 2 and 3 and Figure 12			1	1.2	V
V_F	Forward on-state voltage, GND-to-drain	I_D = 1 A (D1, D2), See Notes 2 and 3			4.6		V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 5 V,	V_{DS} = 0		10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{SG} = 5 V,	V_{DS} = 0		10	100	nA
I_{lkg}	Leakage current, drain-to-GND	V_{DGND} = 48 V (D1, D2)	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 5 V, I_D = 1 A, See Notes 2 and 3 and Figures 6 and 7	T_C = 25°C		0.4	0.48	Ω
			T_C = 125°C		0.65	0.68	
g_{fs}	Forward transconductance	V_{DS} = 15 V, See Notes 2 and 3 and Figure 9	I_D = 0.5 A,	1.25	1.39		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 1 MHz,	V_{GS} = 0, See Figure 11		220	275	pF
C_{oss}	Short-circuit output capacitance, common source				120	150	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				100	125	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S =0.5 A, V_{GS} = 0, See Figures 1 and 14	V_{DS} = 48 V, di/dt = 100 A/µs,	Z1 and Z3		55		ns
				Z2 and Z4		150		
				D1 and D2		200		
Q_{RR}	Total diode charge			Z1 and Z3		0.06		µC
				Z2 and Z4		0.3		
				D1 and D2		0.7		

resistive-load switching characteristics, T_C = 25°C

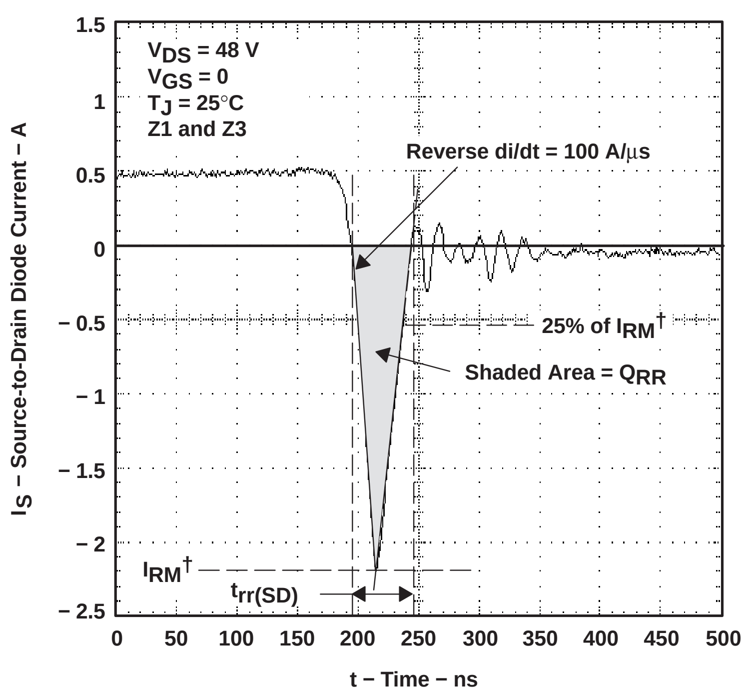
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 25 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		34	68	ns
$t_{d(off)}$	Turn-off delay time			40	82	
t_r	Rise time			21	42	
t_f	Fall time			25	50	
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 1 A, V_{GS} = 10 V, See Figure 3		3.9	5	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.55	0.8	
Q_{gd}	Gate-to-drain charge			2.5	3.6	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance (see Note 4)	DW package	All outputs with equal power		90		°C/W
		NE package			60		
$R_{θJP}$	Junction-to-pin thermal resistance	DW package			30		°C/W
		NE package			25		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

PARAMETER MEASUREMENT INFORMATION

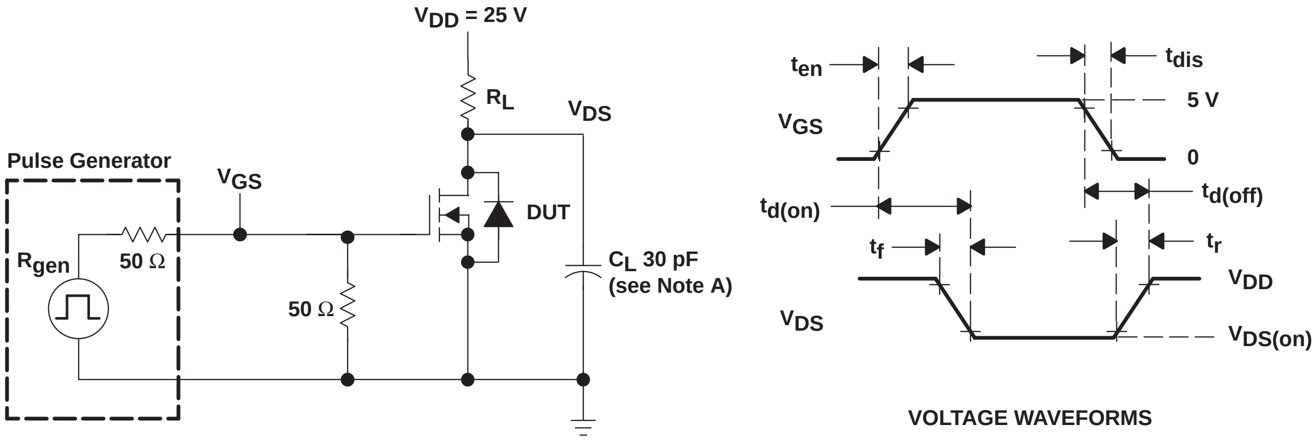


† I_{RM} = maximum recovery current

NOTE A. The above waveform is representative of Z2, Z4, D1, and D2 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

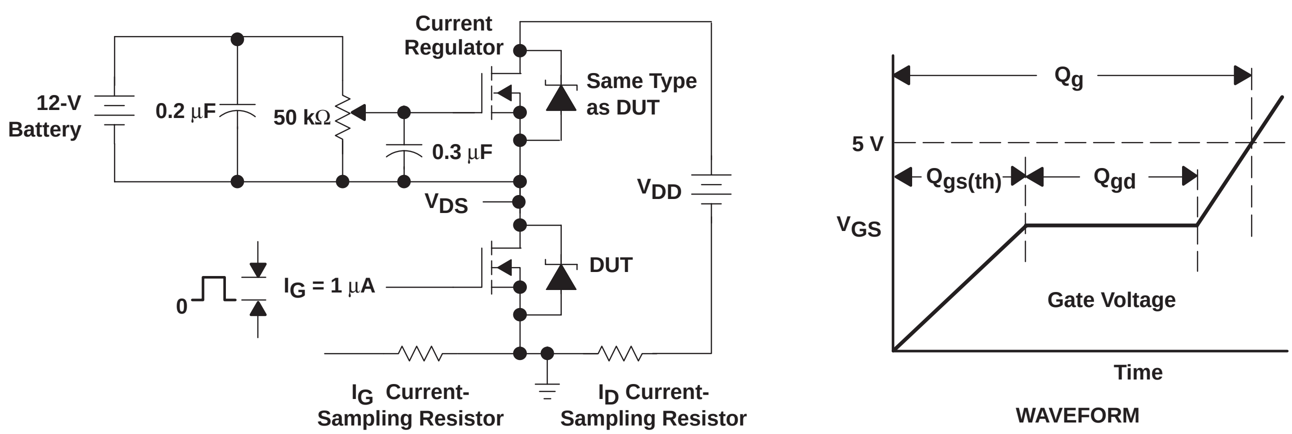
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

NOTE A: C_L includes probe and jig capacitance.

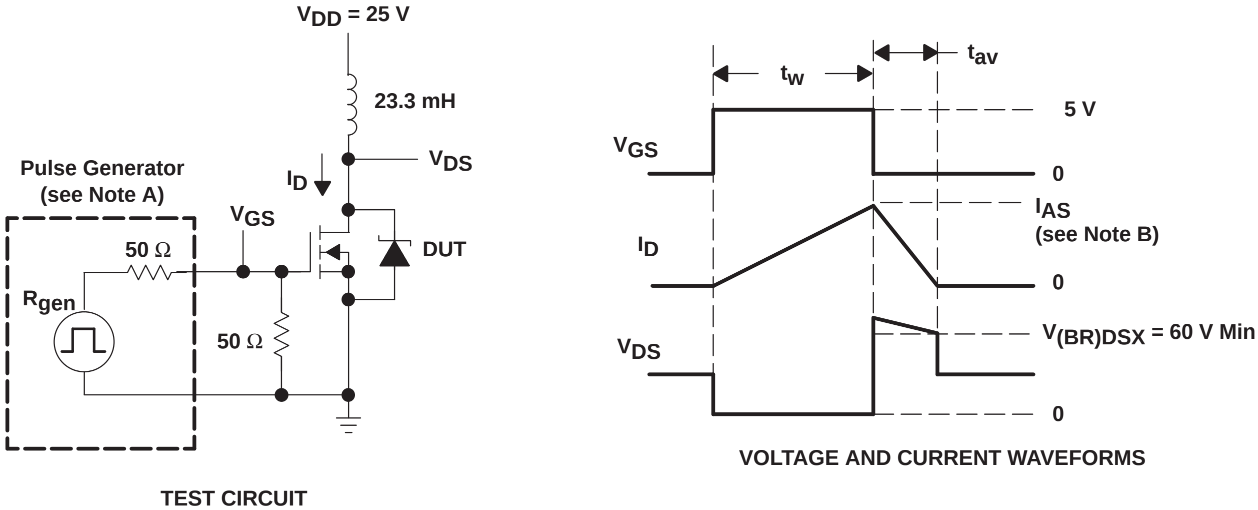
Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms



TEST CIRCUIT

Figure 3. Gate-Charge Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 3$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 180$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

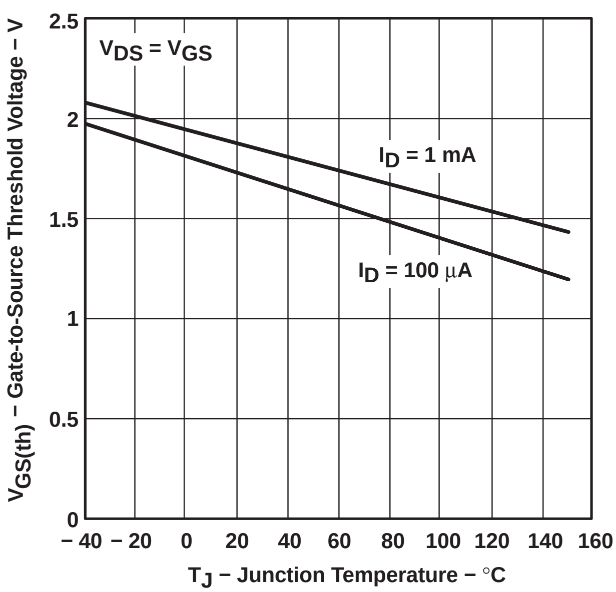


Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

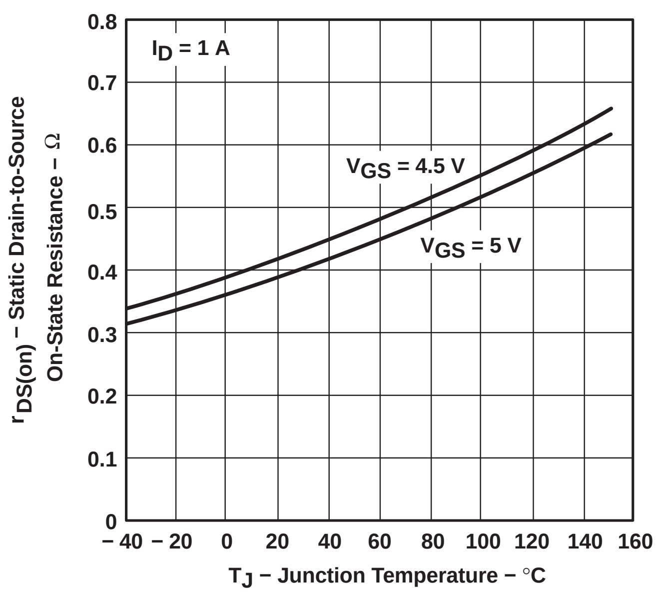


Figure 6

TYPICAL CHARACTERISTICS

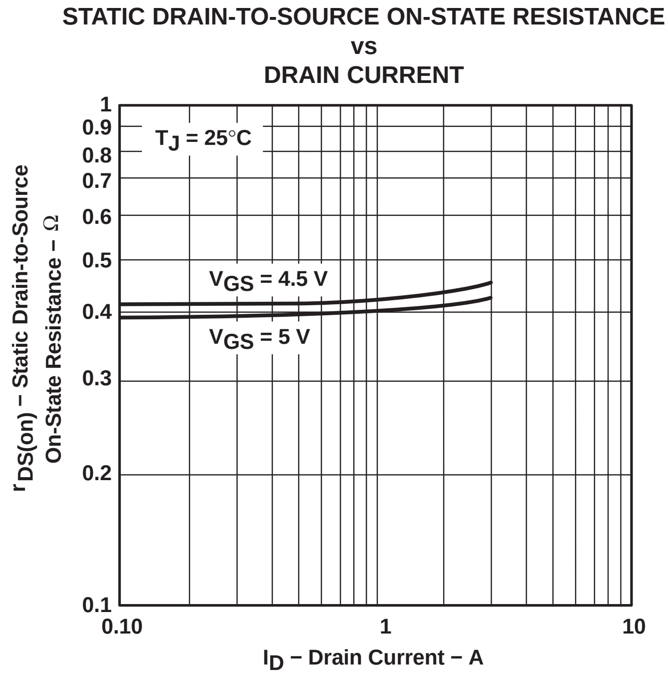


Figure 7

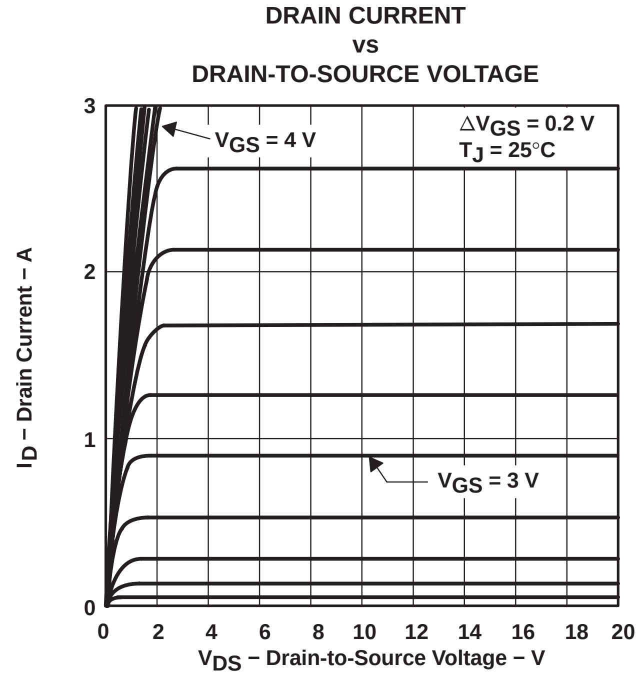


Figure 8

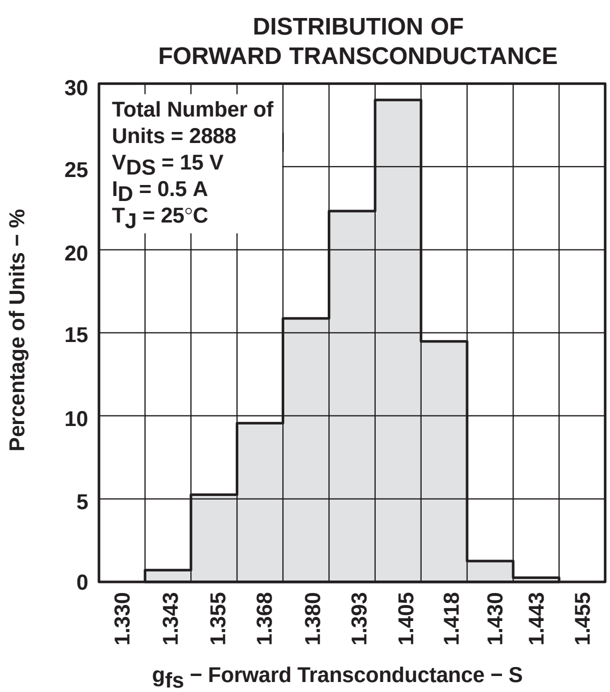


Figure 9

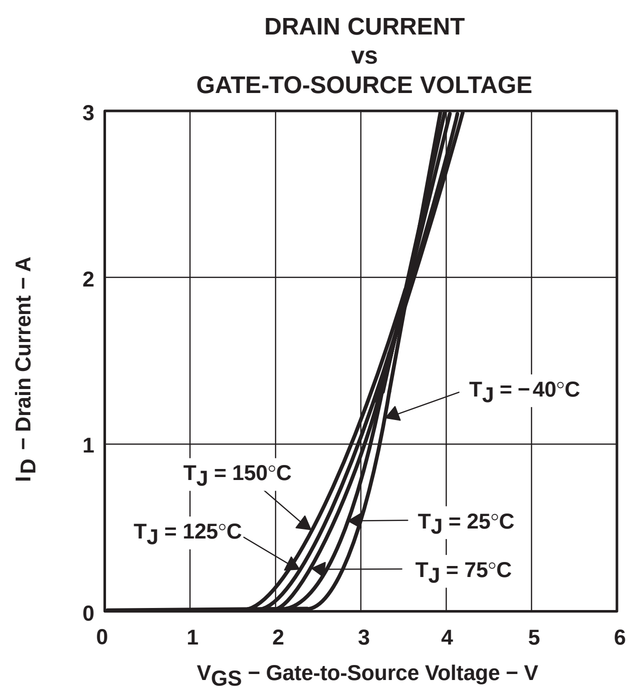


Figure 10

TYPICAL CHARACTERISTICS

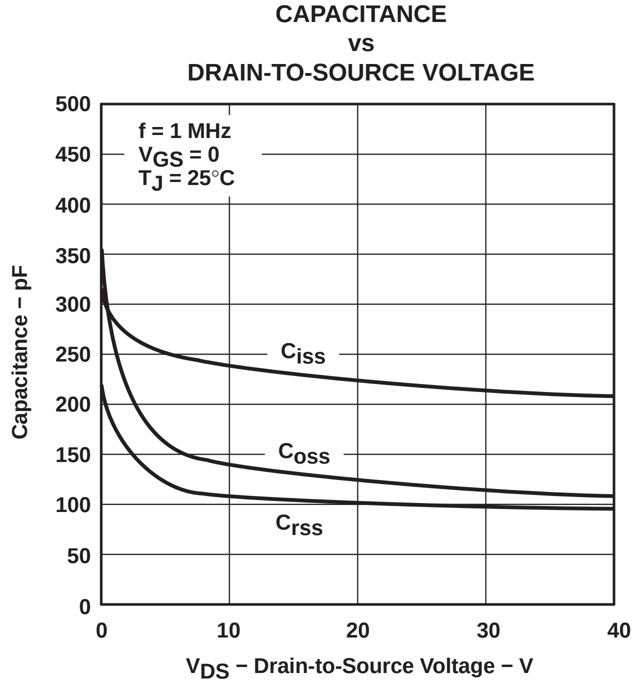


Figure 11

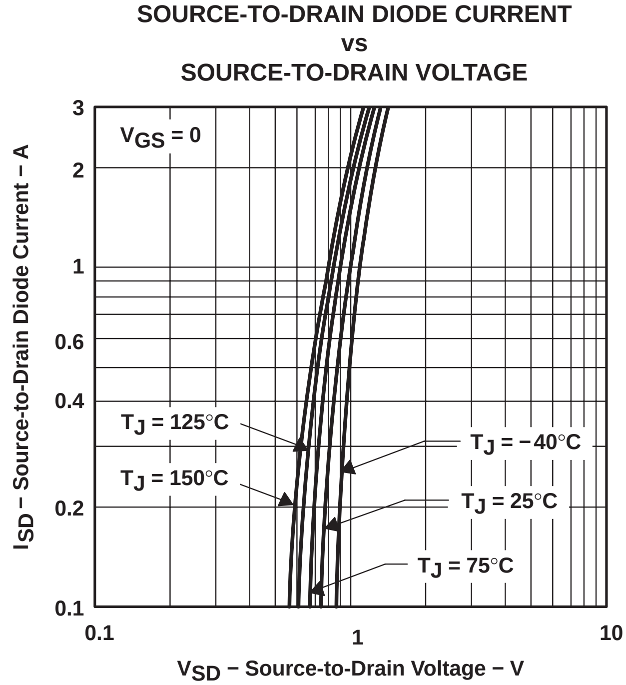


Figure 12

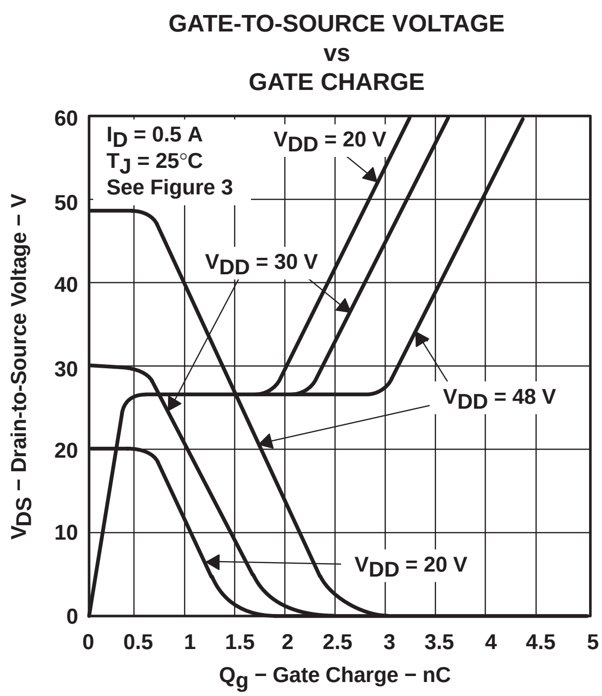


Figure 13

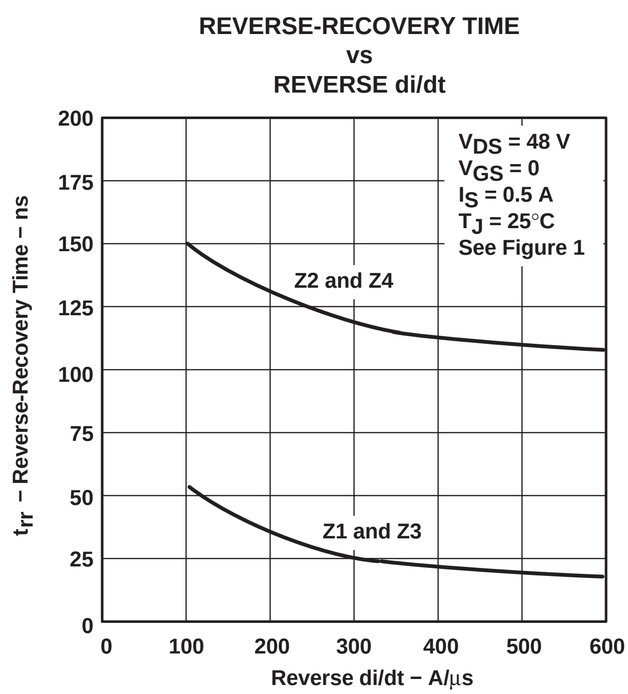
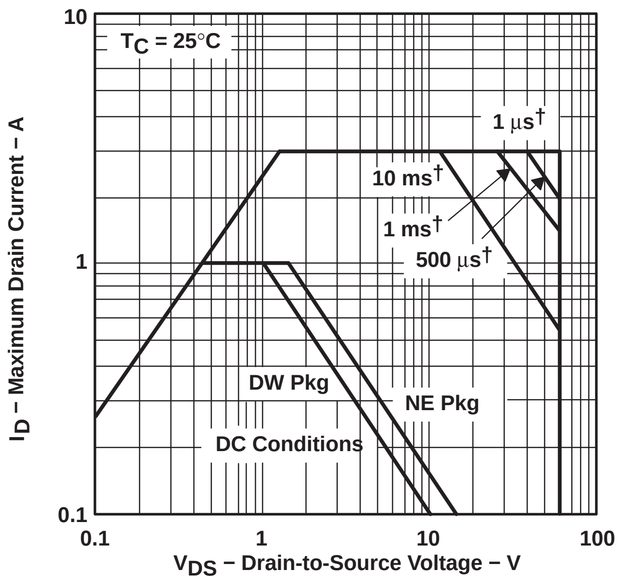


Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



† Less than 2% duty cycle

Figure 15

MAXIMUM PEAK-AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

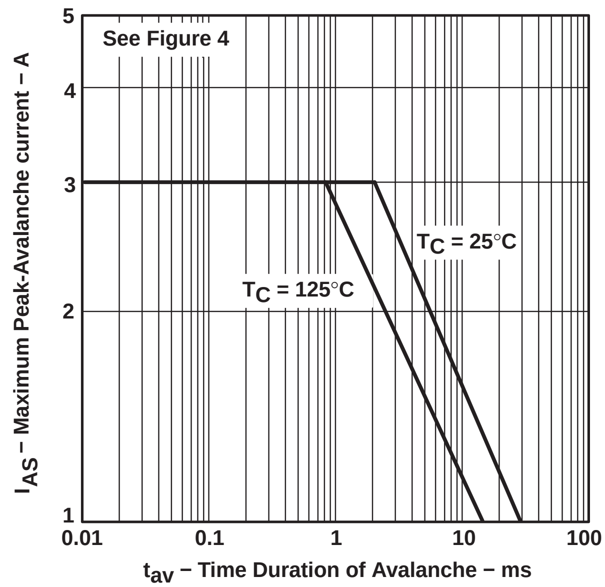
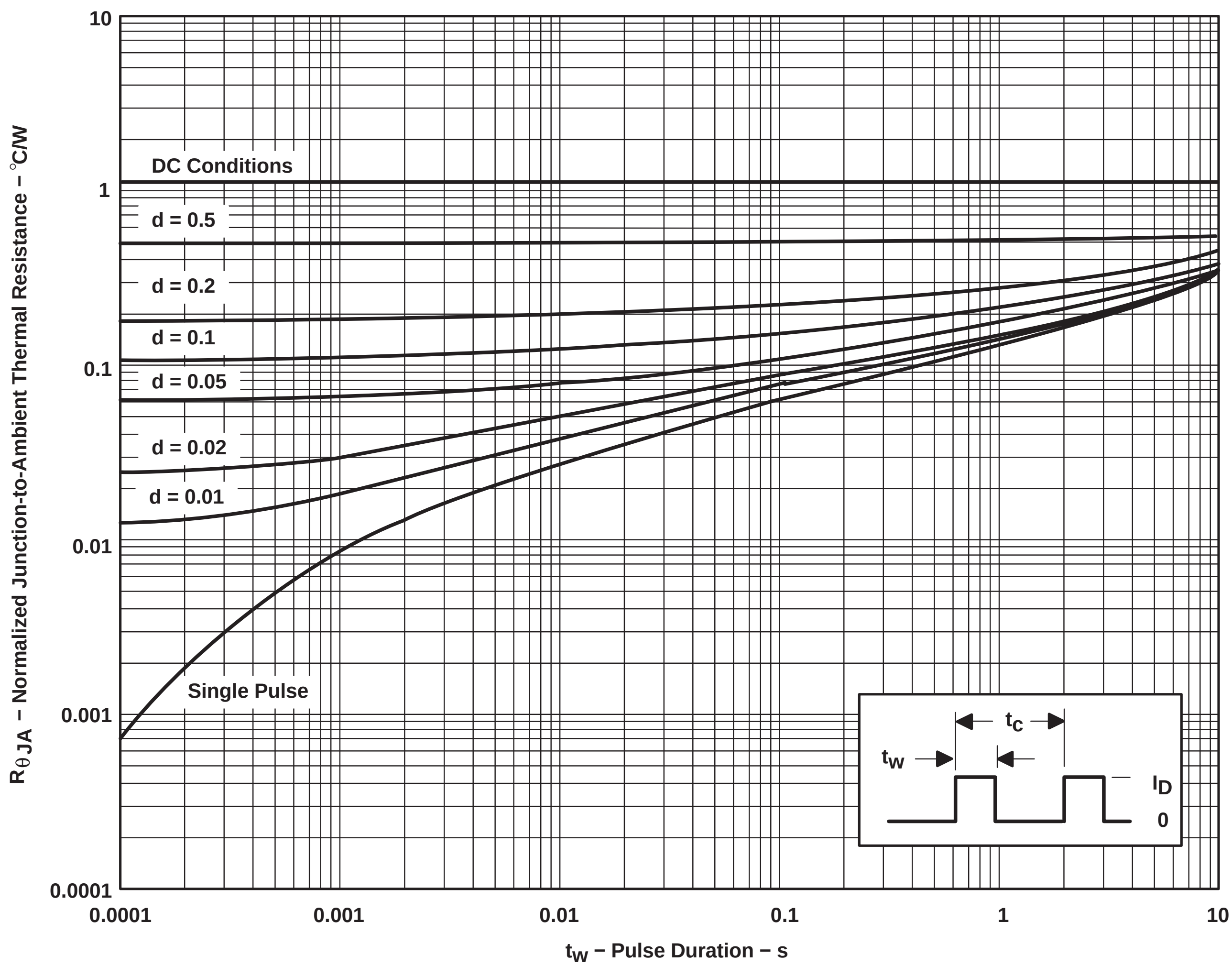


Figure 16

THERMAL INFORMATION

NE PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



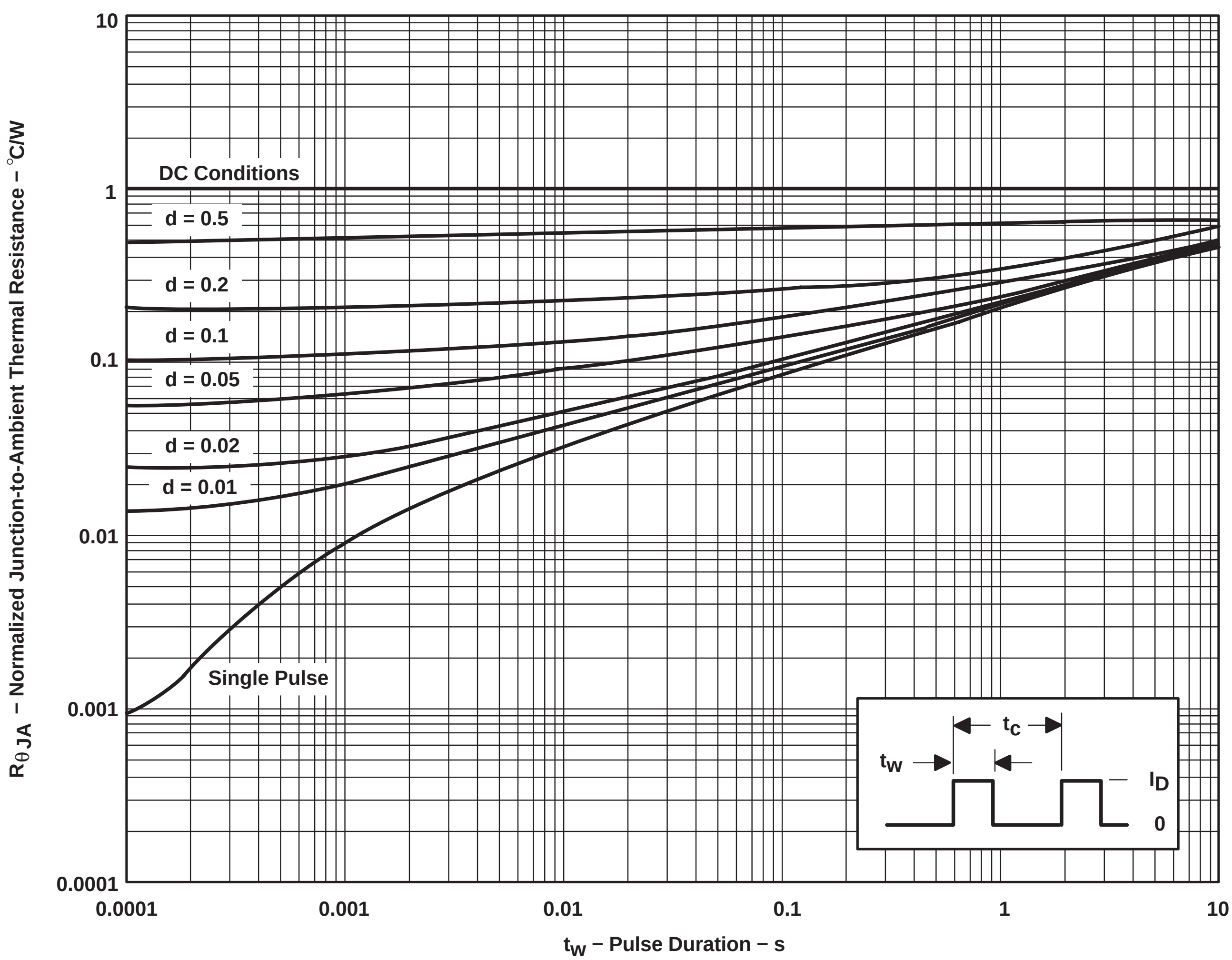
† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

THERMAL INFORMATION

DW PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPIC5424LDW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
TPIC5424LNE	OBSOLETE	PDIP	NE	16		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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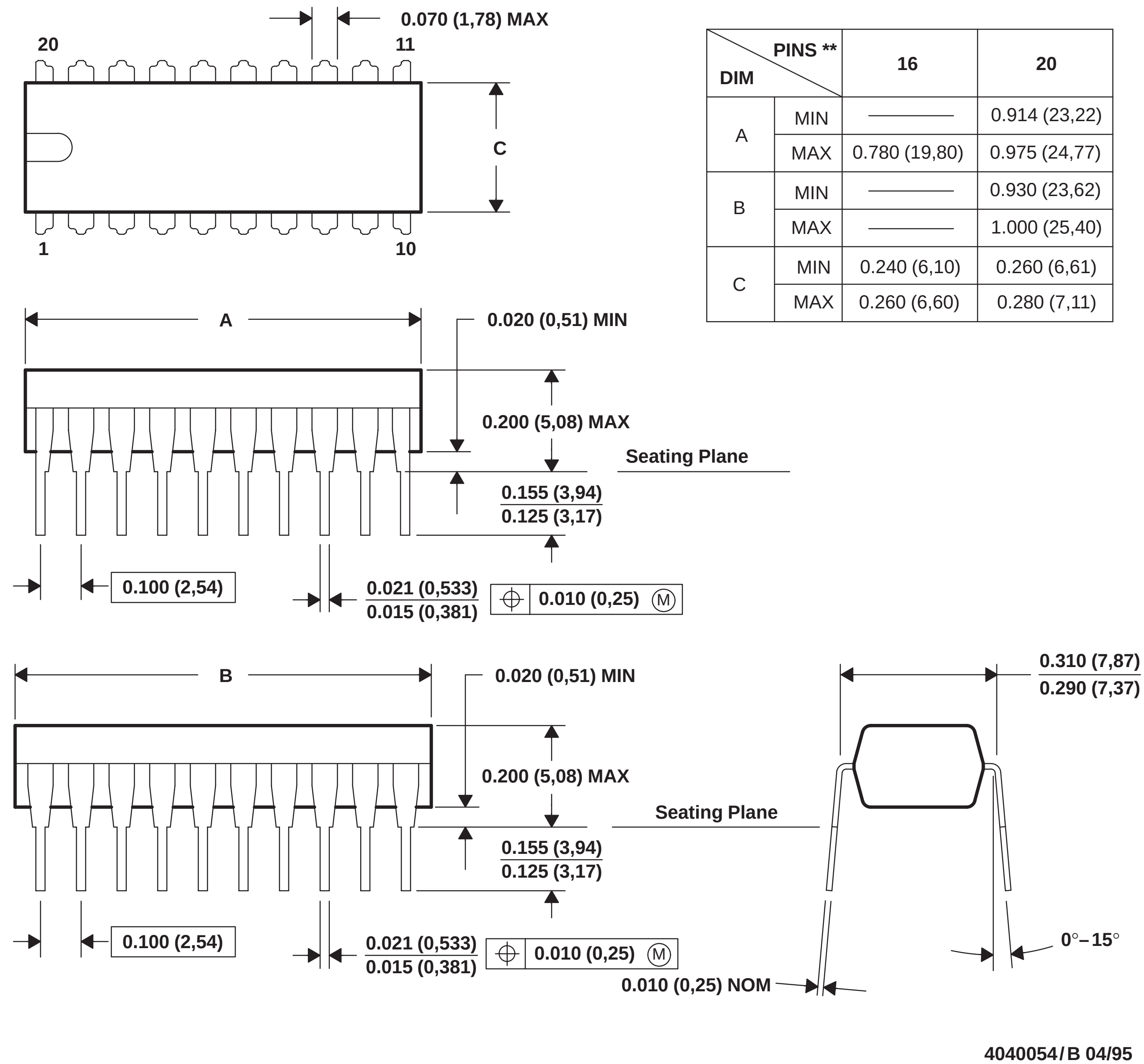
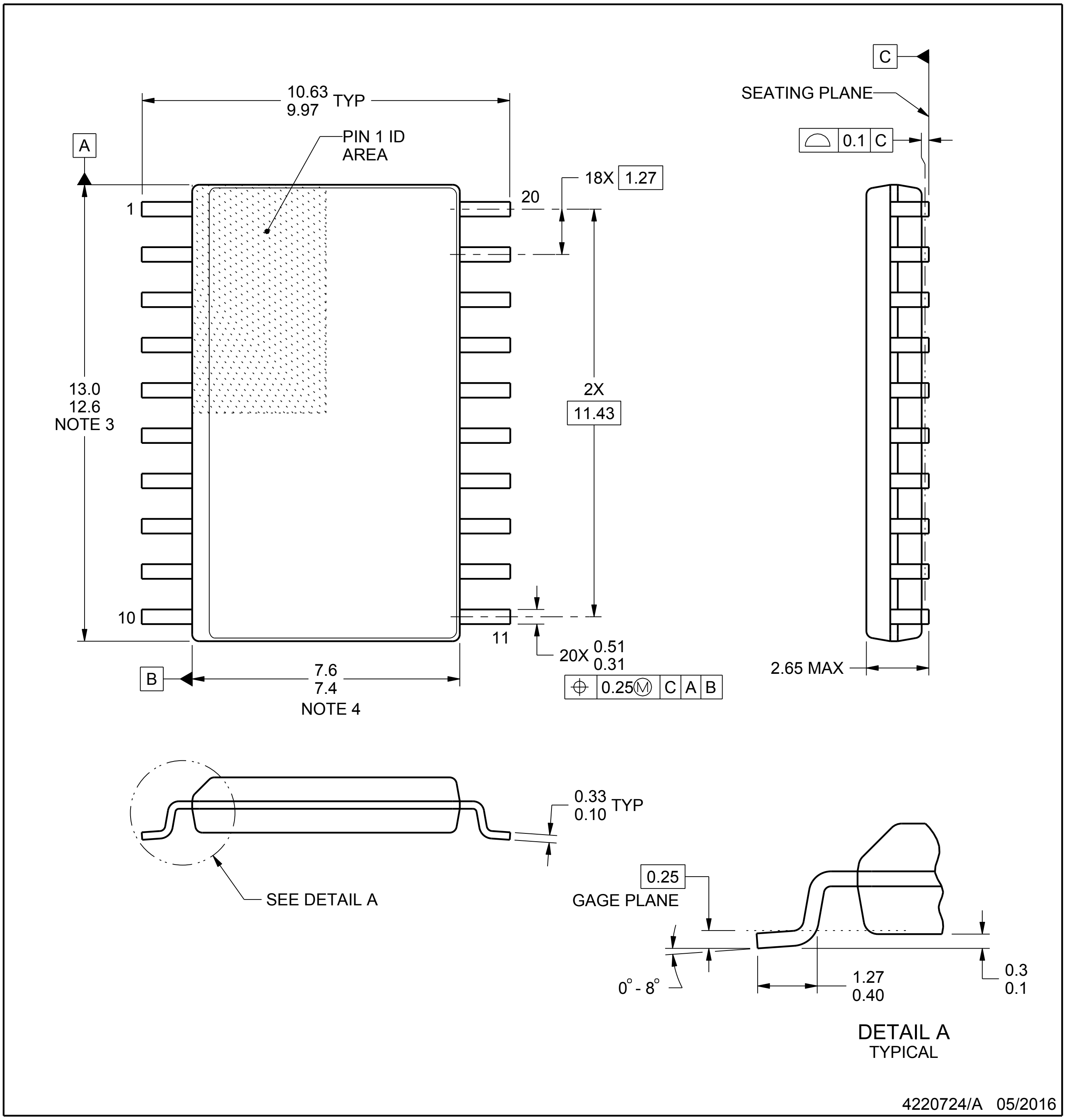
NE (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

20 PIN SHOWN



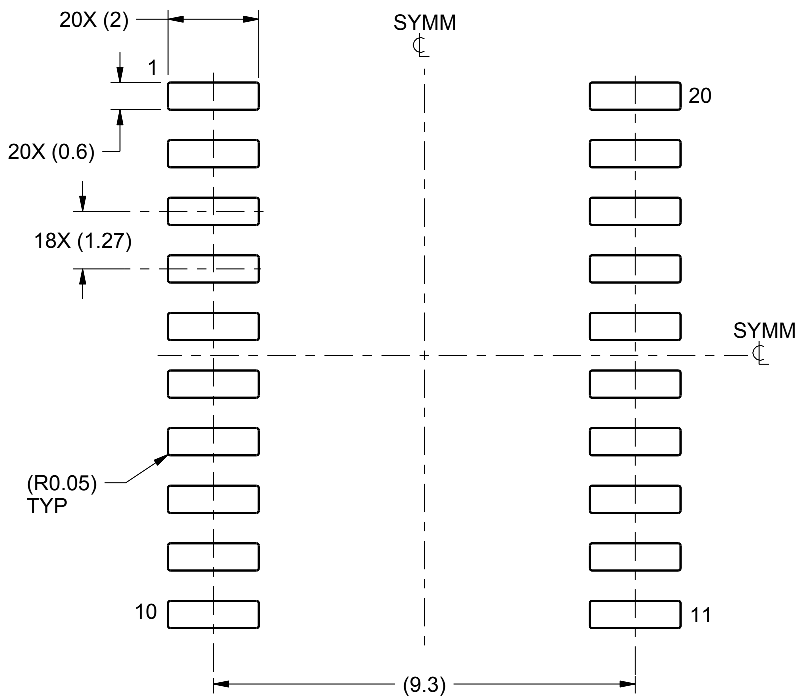
DIM		PINS ** 16	20
A	MIN	————	0.914 (23,22)
	MAX	0.780 (19,80)	0.975 (24,77)
B	MIN	————	0.930 (23,62)
	MAX	————	1.000 (25,40)
C	MIN	0.240 (6,10)	0.260 (6,61)
	MAX	0.260 (6,60)	0.280 (7,11)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (16 pin only)

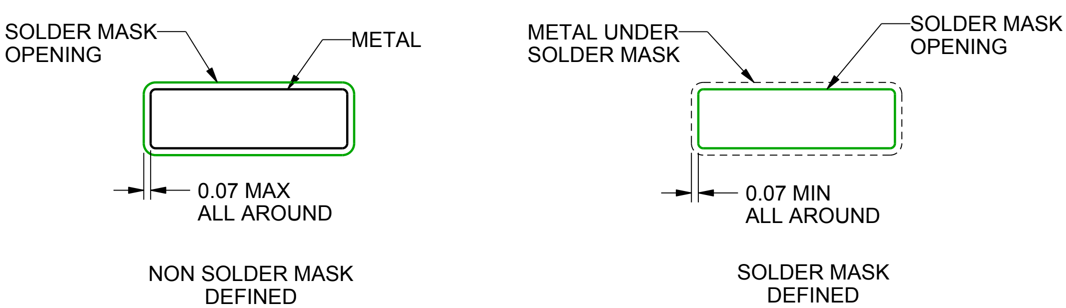


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

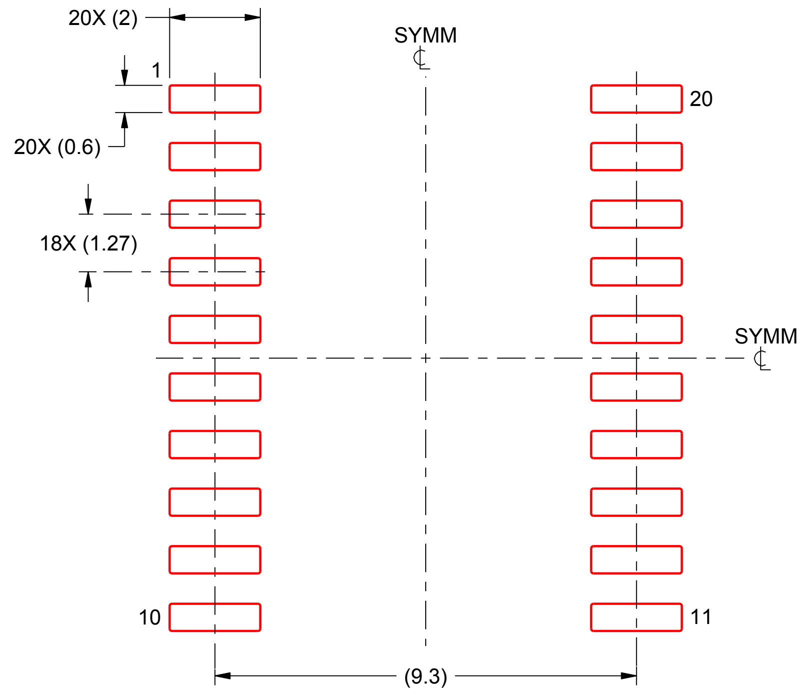


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
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