

FQB9N50CF

500V N-Channel MOSFET

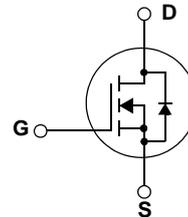
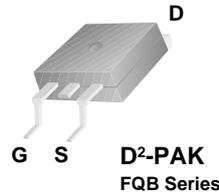
Features

- 9A, 500V, $R_{DS(on)} = 0.85 \Omega @ V_{GS} = 10 V$
- Low gate charge (typical 28nC)
- Low C_{rss} (typical 24pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, electronic lamp ballasts based on half bridge topology.



Absolute Maximum Ratings

Symbol	Parameter	FQB9N50CF	Units
V_{DSS}	Drain-Source Voltage	500	V
I_D	Drain Current - Continuous ($T_C = 25^\circ C$) - Continuous ($T_C = 100^\circ C$)	9	A
		5.7	A
I_{DM}	Drain Current - Pulsed (Note 1)	36	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	300	mJ
I_{AR}	Avalanche Current (Note 1)	5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	9.6	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ C$) - Derate above $25^\circ C$	173	W
		1.38	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ C$

Thermal Characteristics

Symbol	Parameter	FQB9N50CF	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.72	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient*	40	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ C/W$

* When mounted on the minimum pad size recommended (PCB Mount)

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB9N50CF	FQB9N50CFTM	D2-PAK	330mm	24mm	800
FQB9N50CFS	FQB9N50CFTM_WS	D2-PAK	330mm	24mm	800

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	500	--	--	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	--	0.57	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	--	--	10	μA
		V _{DS} = 400 V, T _C = 125°C	--	--	100	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.0	--	4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 4.5A	--	0.7	0.85	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 4.5 A (Note 4)	--	6.5	--	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	790	1030	pF
C _{oss}	Output Capacitance		--	130	170	pF
C _{rss}	Reverse Transfer Capacitance		--	24	30	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 250 V, I _D = 9A, R _G = 25 Ω	--	18	45	ns
t _r	Turn-On Rise Time		--	65	140	ns
t _{d(off)}	Turn-Off Delay Time		--	93	195	ns
t _f	Turn-Off Fall Time		(Note 4, 5)	--	64	125
Q _g	Total Gate Charge	V _{DS} = 400 V, I _D = 9A, V _{GS} = 10 V	--	28	35	nC
Q _{gs}	Gate-Source Charge		--	4	--	nC
Q _{gd}	Gate-Drain Charge		(Note 4, 5)	--	15	--
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	9	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	36	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 9 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 9 A, dI _F / dt = 100 A/μs (Note 4)	--	100	--	ns
Q _{rr}	Reverse Recovery Charge		--	300	--	nC

NOTES:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 8mH, I_{AS} = 9A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 9A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Performance Characteristics

Figure 1. On-Region Characteristics

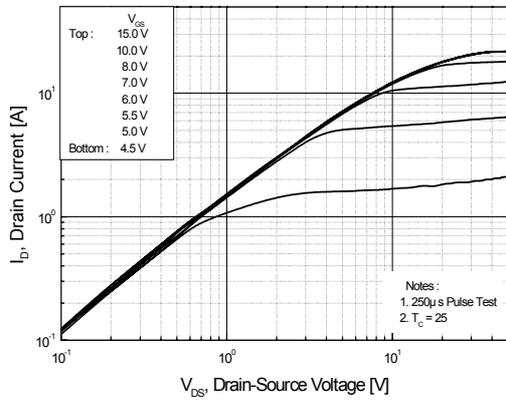


Figure 2. Transfer Characteristics

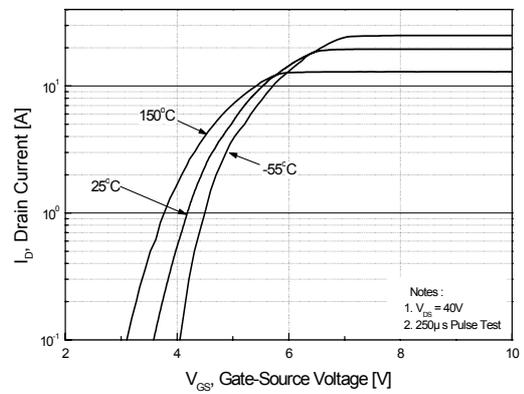


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

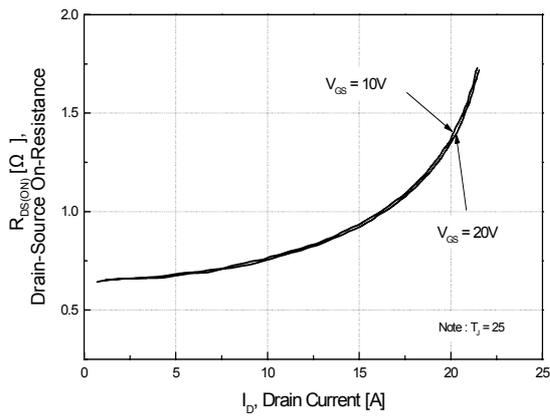


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

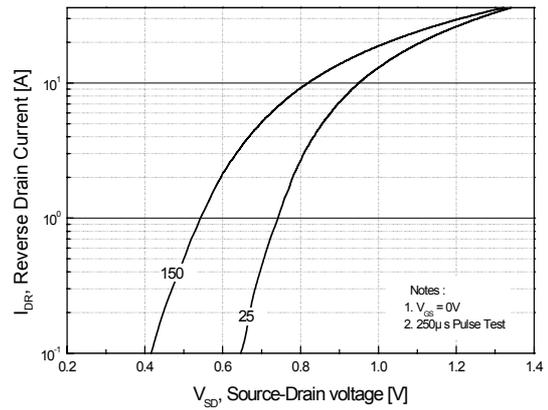


Figure 5. Capacitance Characteristics

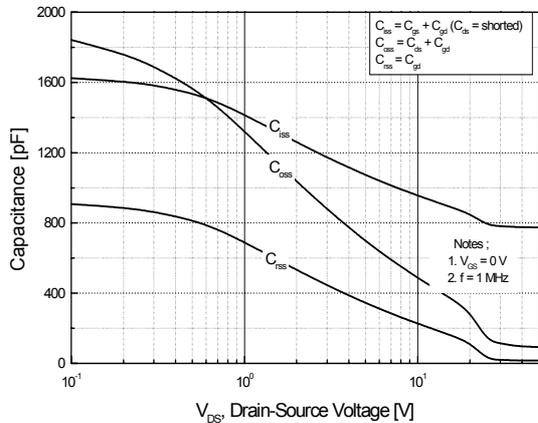
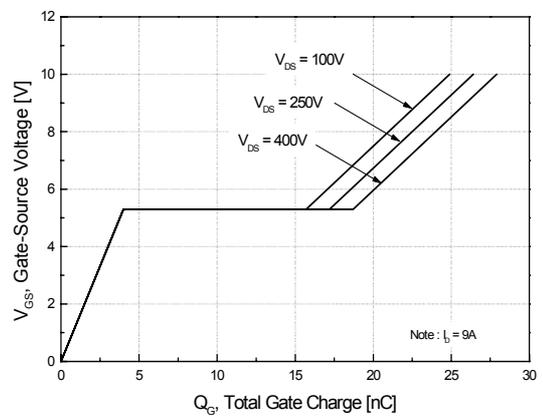


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

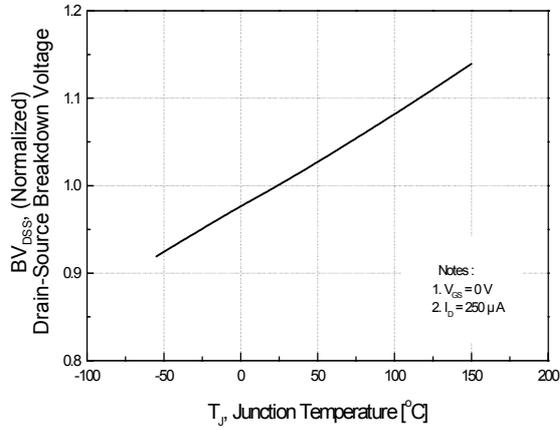


Figure 8. On-Resistance Variation vs. Temperature

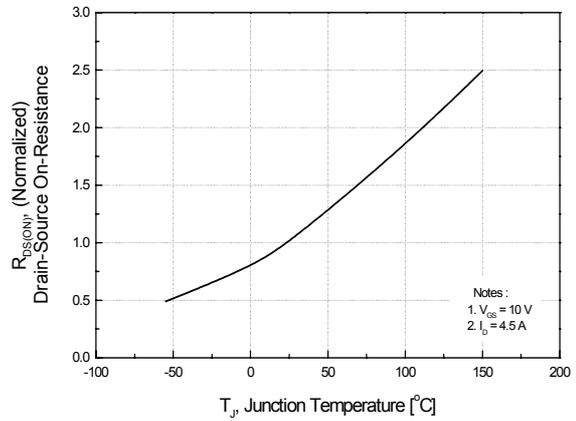


Figure 9. Maximum Safe Operating Area

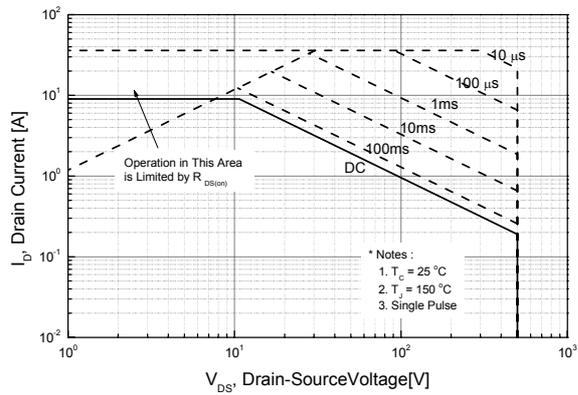


Figure 10. Maximum Drain Current vs. Case Temperature

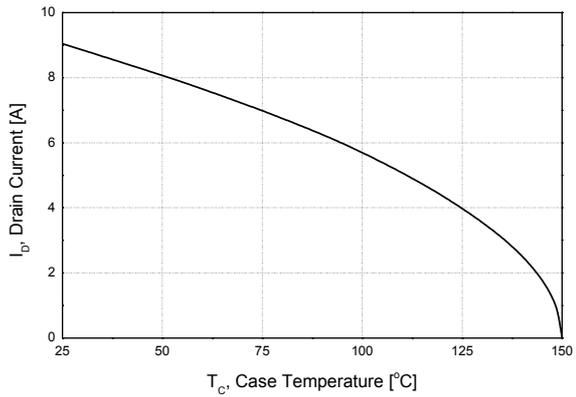
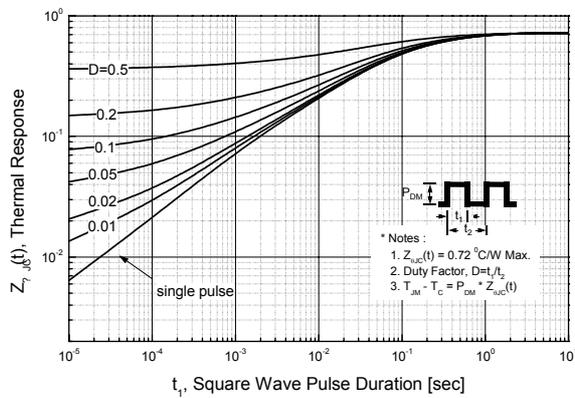
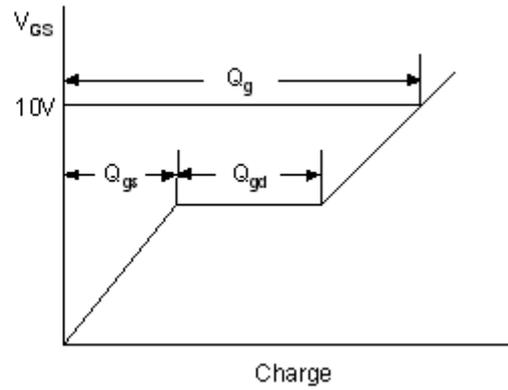
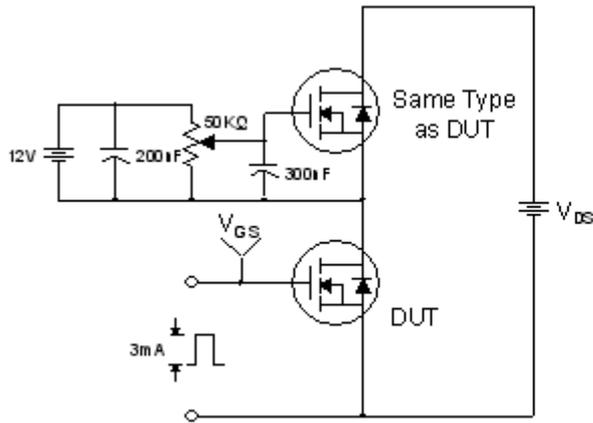


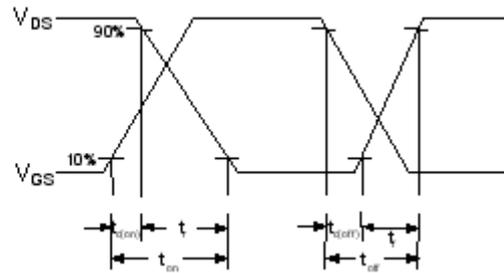
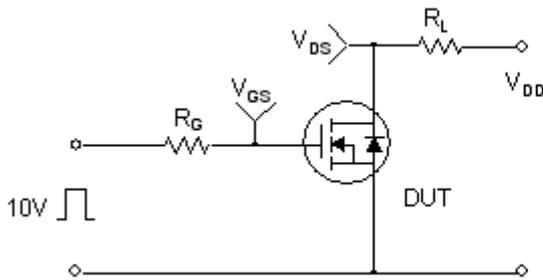
Figure 11. Transient Thermal Response Curve



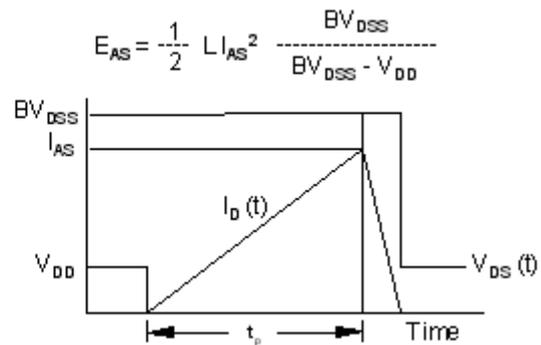
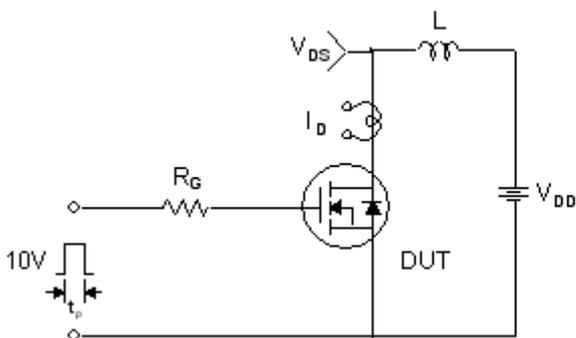
Gate Charge Test Circuit & Waveform



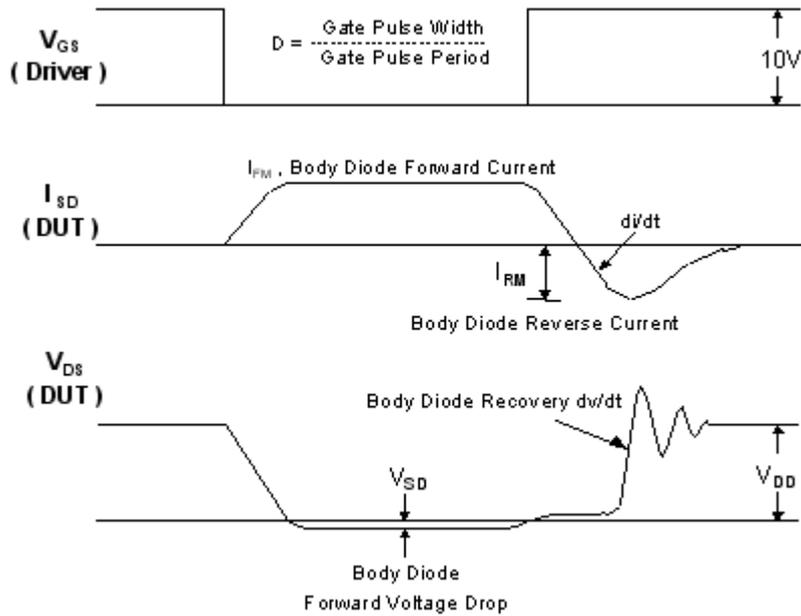
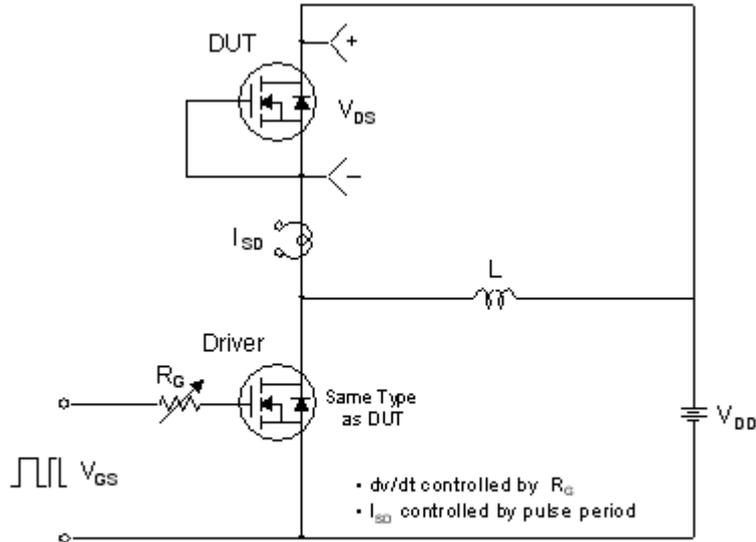
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

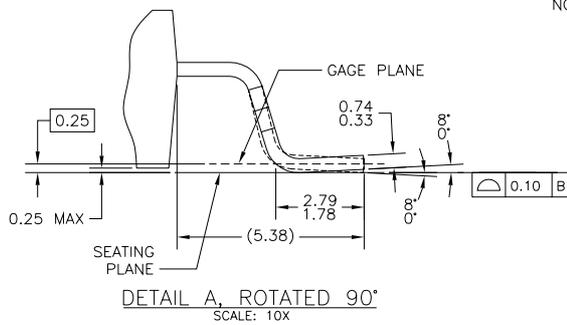
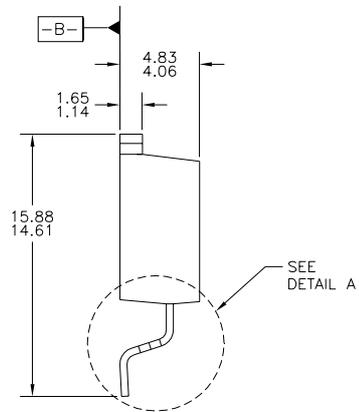
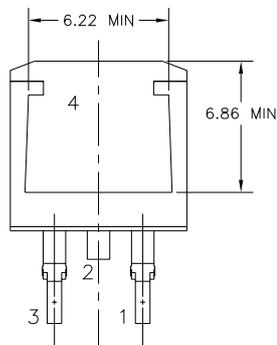
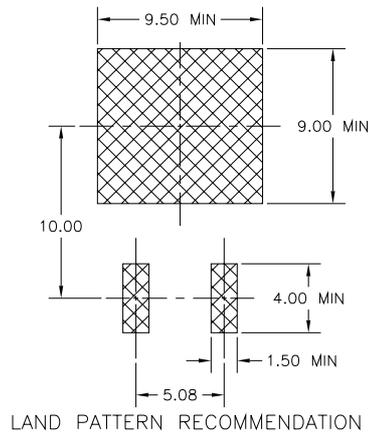
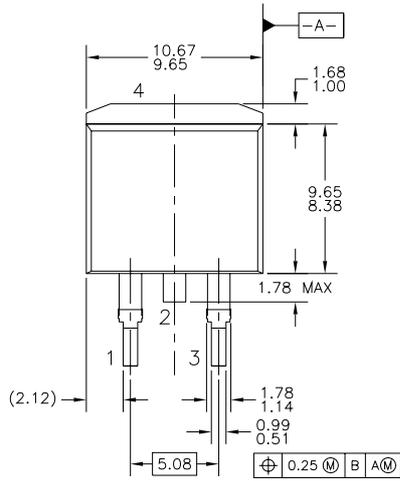


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

D2-PAK



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) REFERENCE JEDEC, TO-263, ISSUE D, VARIATION AB, DATED JULY 2003.
 - C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1982.
 - D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
 - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

TO263A02REVD

Dimensions in Millimeters

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I20

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FQB9N50CF

500V N-Channel MOSFET

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General description

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Product	Product status	Pb-free Status	Pricing*	Package type	Leads	Packing method	Package Marking Convention**
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FQB9N50CFTM	Full Production	 Full Production	\$1.40	TO-263(D2PAK)	2	TAPE REEL	Line 1: \$Y (Fairchild logo) &Z (Asm. Plant Code) &E&3 (3-Digit Date Code) Line 2: FQB Line 3: 9N50CF
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* Fairchild 1,000 piece Budgetary Pricing

** A sample button will appear if the part is available through Fairchild's on-line samples program. If there is no sample button, please contact a [Fairchild distributor](#) to obtain samples



Indicates product with Pb-free second-level interconnect. For more information [click here](#).

Package marking information for product FQB9N50CF is available. [Click here for more information](#).

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Qualification Support

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FQB9N50CFTM

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