

MOSFET - PowerTrench[®], N-Channel, Dual Cool[™], Shielded Gate

150 V, 40 A, 17 mΩ



ON Semiconductor[®]

www.onsemi.com

FDMS86200DC

General Description

This N-Channel MOSFET is produced using ON Semiconductor's advanced PowerTrench[®] process that incorporates Shielded Gate technology. Advancements in both silicon and Dual Cool[™] package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

Features

- Shielded Gate MOSFET Technology
- Dual Cool[™] Top Side Cooling DFN8 Package
- Max $r_{DS(on)}$ = 17 mΩ at $V_{GS} = 10$ V, $I_D = 9.3$ A
- Max $r_{DS(on)}$ = 25 mΩ at $V_{GS} = 6$ V, $I_D = 7.8$ A
- High Performance Technology for Extremely Low $r_{DS(on)}$
- 100% UIL Tested
- RoHS Compliant

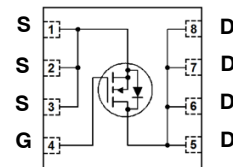
Applications

- Primary MOSFET in DC - DC Converters
- Secondary Synchronous Rectifier
- Load Switch

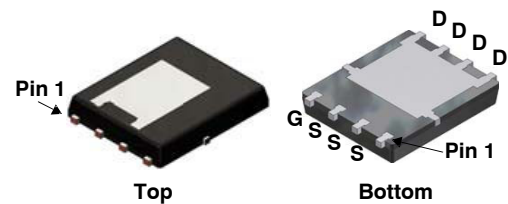
MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Ratings | Unit |
|----------------|---|------------------|------------------|
| V_{DS} | Drain to Source Voltage | 150 | V |
| V_{GS} | Gate to Source Voltage | ±20 | V |
| I_D | Drain Current: Continuous, $T_C = 25^\circ\text{C}$ Continuous, $T_A = 25^\circ\text{C}$ (Note 1a) Pulsed (Note 4) | 40 9.3 100 | A |
| E_{AS} | Single Pulse Avalanche Energy (Note 3) | 294 | mJ |
| P_D | Power Dissipation: $T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a) | 125 3.2 | W |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | $^\circ\text{C}$ |

ELECTRICAL CONNECTION

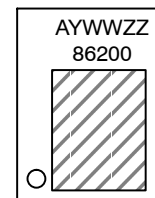


N-Channel MOSFET



DFN8, Dual Cool[™]
CASE 506EG

MARKING DIAGRAM



86200 = Specific Device Code
A = Assembly Location
Y = Year of Production, Last Number
WW = Work Week Number
ZZ = Assembly Lot Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMS86200DC

Table 1. THERMAL CHARACTERISTICS

| Symbol | Characteristic | Value | Unit |
|-----------------|---|-------|------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case (Top Source) | 2.5 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case (Bottom Drain) | 1.0 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 38 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1b) | 81 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1i) | 16 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1j) | 23 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1k) | 11 | |

ORDERING INFORMATION AND PACKAGE MARKING

| Device | Top Marking | Package | Reel Size | Tape Width | Shipping† |
|-------------|-------------|---------|-----------|------------|----------------------------|
| FDMS86200DC | 86200 | DFN8 | 13" | 12 mm | 3000 Units/ Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|--------|-----------|----------------|-----|-----|-----|------|
|--------|-----------|----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|--------------------------------|---|--|-----|-----|-----------|---------------|
| BV_{DSS} | Drain to Source Breakdown Voltage | $I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$ | 150 | | | V |
| $\Delta BV_{DSS} / \Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D = 250 \mu\text{A}$, referenced to 25°C | | 105 | | mV/°C |
| I_{BSS} | Zero Gate Voltage Drain Current | $V_{DS} = 120 \text{ V}, V_{GS} = 0 \text{ V}$ | | | 1 | μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$ | | | ± 100 | nA |

ON CHARACTERISTICS

| | | | | | | |
|----------------------------------|--|---|-----|-----|-----|------------|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$ | 2.0 | 3.3 | 4.0 | V |
| $\Delta V_{GS(th)} / \Delta T_J$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250 \mu\text{A}$, referenced to 25°C | | -11 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS} = 10 \text{ V}, I_D = 9.3 \text{ A}$ | | 14 | 17 | m Ω |
| | | $V_{GS} = 6 \text{ V}, I_D = 7.8 \text{ A}$ | | 17 | 25 | |
| | | $V_{GS} = 10 \text{ V}, I_D = 9.3 \text{ A}, T_J = 125^\circ\text{C}$ | | 29 | 35 | |
| g_{FS} | Forward Transconductance | $V_{DS} = 10 \text{ V}, I_D = 9.3 \text{ A}$ | | 32 | | S |

DYNAMIC CHARACTERISTICS

| | | | | | | |
|-----------|------------------------------|---|-----|------|------|----------|
| C_{iss} | Input Capacitance | $V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$ | | 2110 | 2955 | pF |
| C_{oss} | Output Capacitance | | | 205 | 290 | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 8.1 | 15 | pF |
| R_g | Gate Resistance | | 0.1 | 1.5 | 3.0 | Ω |

SWITCHING CHARACTERISTICS

| | | | | | | |
|--------------|---------------------|--|--|----|----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 75 \text{ V}, I_D = 9.3 \text{ A}, V_{GS} = 10 \text{ V},$ $R_{GEN} = 6 \Omega$ | | 16 | 29 | ns |
| t_r | Rise Time | | | 4 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 23 | 37 | ns |
| t_f | Fall Time | | | 5 | 10 | ns |

FDMS86200DC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|-----------------|-------------------------------|---|-----|-----|-----|------|
| Q _g | Total Gate Charge | V _{GS} = 0 V to 10 V, V _{DD} = 75 V, I _D = 9.3 A | | 30 | 42 | nC |
| | | V _{GS} = 0 V to 5 V, V _{DD} = 75 V, I _D = 9.3 A | | 19 | 27 | nC |
| Q _{gs} | Gate to Source Charge | V _{DD} = 75 V, I _D = 9.3 A | | 9.7 | | nC |
| Q _{gd} | Gate to Drain "Miller" Charge | | | 5.6 | | nC |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | |
|-----------------|---------------------------------------|--|--|-----|-----|----|
| V _{SD} | Source to Drain Diode Forward Voltage | V _{GS} = 0 V, I _S = 9.3 A (Note 2) | | 0.8 | 1.3 | V |
| | | V _{GS} = 0 V, I _S = 2.6 A (Note 2) | | 0.7 | 1.2 | |
| t _{rr} | Reverse Recovery Time | I _F = 9.3 A, di/dt = 100 A/μs | | 79 | 126 | ns |
| Q _{rr} | Reverse Recovery Charge | | | 126 | 176 | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

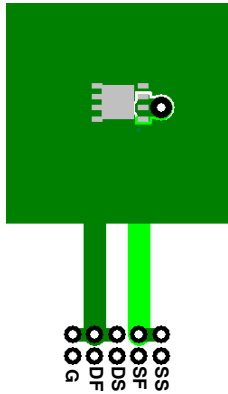
RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Max | Unit |
|------------------|---|-----|------|
| R _{θJC} | Thermal Resistance, Junction to Case (Top Source) | 2.5 | °C/W |
| R _{θJC} | Thermal Resistance, Junction to Case (Bottom Drain) | 1.0 | |
| R _{θJA} | Thermal Resistance, Junction to Ambient (Note 1a) | 38 | |
| R _{θJA} | Thermal Resistance, Junction to Ambient (Note 1b) | 81 | |
| R _{θJA} | Thermal Resistance, Junction to Ambient (Note 1c) | 27 | |
| R _{θJA} | Thermal Resistance, Junction to Ambient (Note 1d) | 34 | |
| R _{θJA} | Thermal Resistance, Junction to Ambient (Note 1e) | 16 | |
| R _{θJA} | Thermal Resistance, Junction to Ambient (Note 1f) | 19 | |
| R _{θJA} | Thermal Resistance, Junction to Ambient (Note 1g) | 26 | |
| R _{θJA} | Thermal Resistance, Junction to Ambient (Note 1h) | 61 | |
| R _{θJA} | Thermal Resistance, Junction to Ambient (Note 1i) | 16 | |
| R _{θJA} | Thermal Resistance, Junction to Ambient (Note 1j) | 23 | |
| R _{θJA} | Thermal Resistance, Junction to Ambient (Note 1k) | 11 | |
| R _{θJA} | Thermal Resistance, Junction to Ambient (Note 1l) | 13 | |

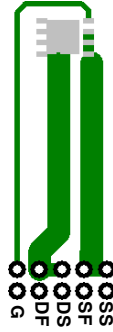
1. R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. R_{θCA} is determined by the user's board design.

FDMS86200DC

NOTES: $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a) 38°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 81°C/W when mounted on a 1 in² pad of 2 oz copper.

- c) Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- d) Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e) Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- f) Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- g) 200FPM Airflow, No Heat Sink, 1 in² pad of 2 oz copper
- h) 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i) 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- j) 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- k) 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- l) 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- 3. E_{AS} of 294 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3\text{ mH}$, $I_{AS} = 14\text{ A}$, $V_{DD} = 150\text{ V}$. $V_{GS} = 10\text{ V}$, 100% tested at $L = 0.3\text{ mH}$, $I_{AS} = 31\text{ A}$.
- 4. Pulsed Id limited by junction temperature, $t_d \leq 10\ \mu\text{s}$, please refer to SOA curve for more details.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

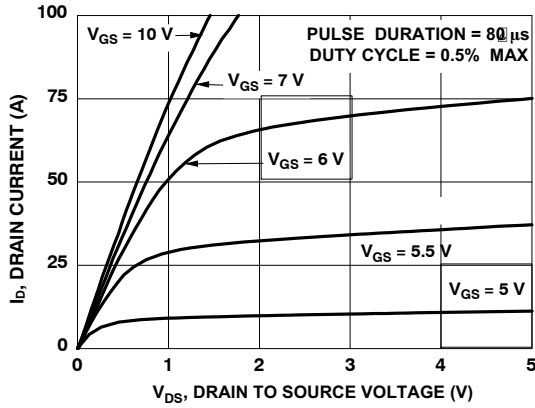


Figure 1. On-Region Characteristics

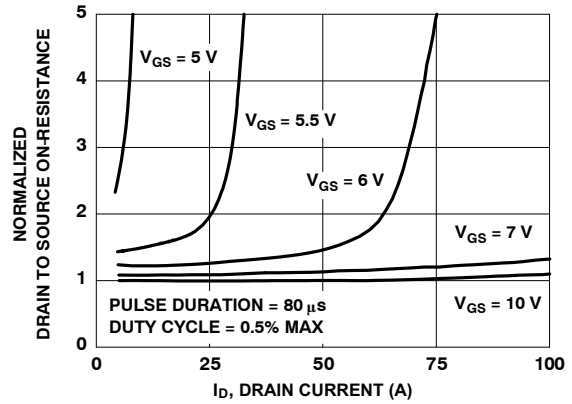


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

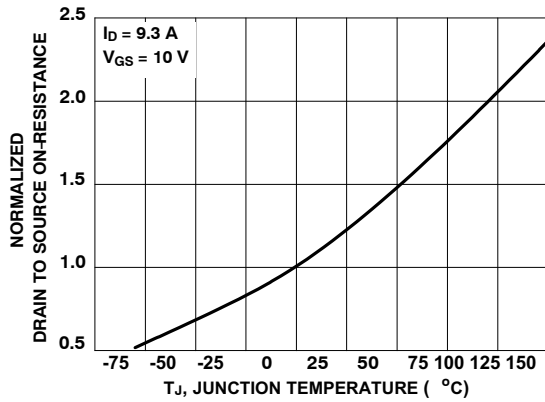


Figure 3. Normalized On-Resistance vs. Junction Temperature

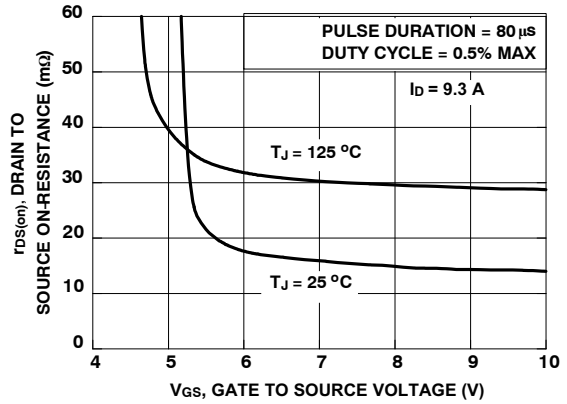


Figure 4. On-Resistance vs. Gate to Source Voltage

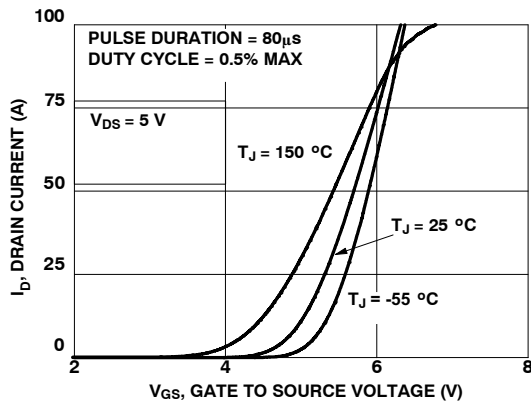


Figure 5. Transfer Characteristics

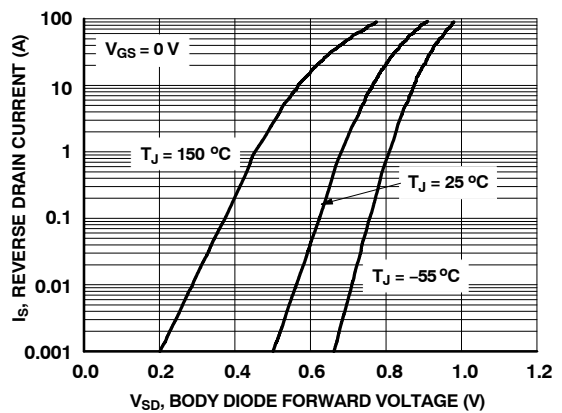


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

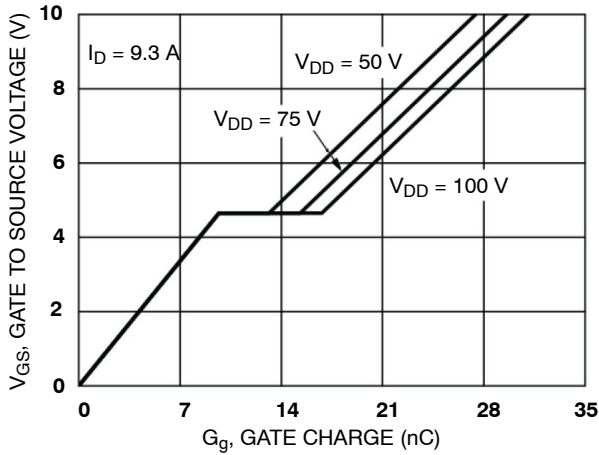


Figure 7. Gate Charge Characteristics

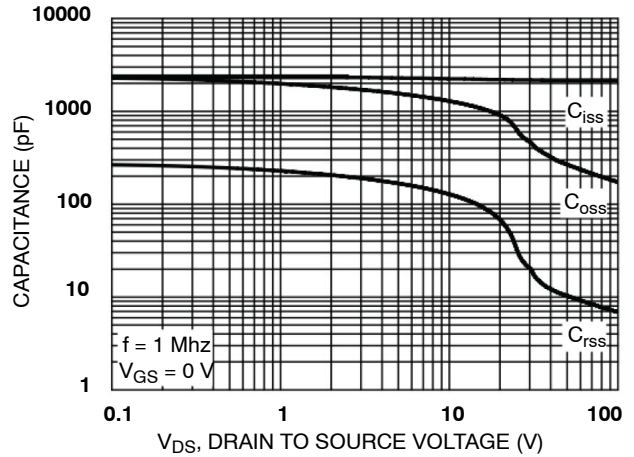


Figure 8. Capacitance vs Drain to Source Voltage

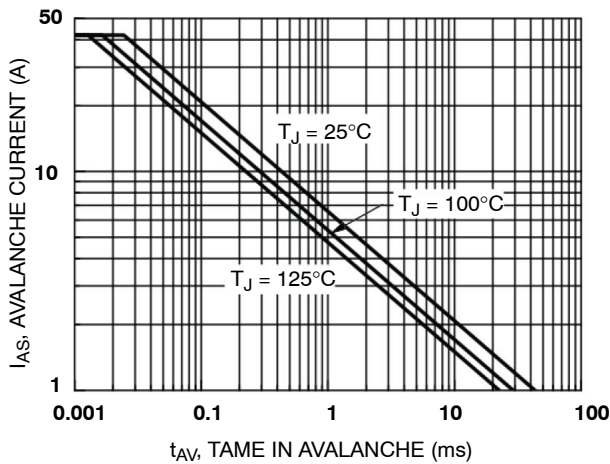


Figure 9. Unclamped Inductive Switching Capability

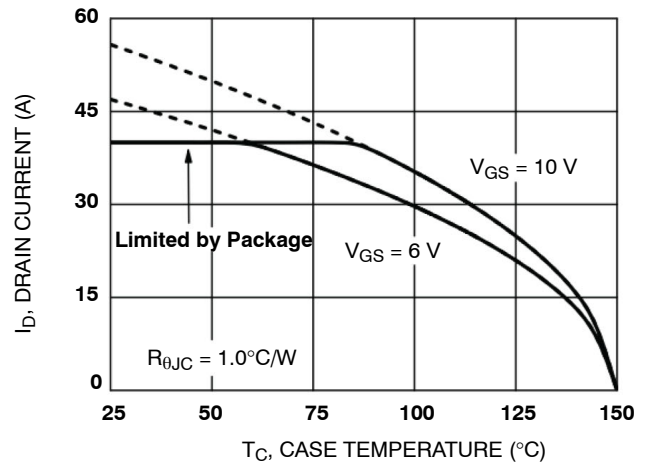


Figure 10. Maximum Continuous Drain Current vs Case Temperature

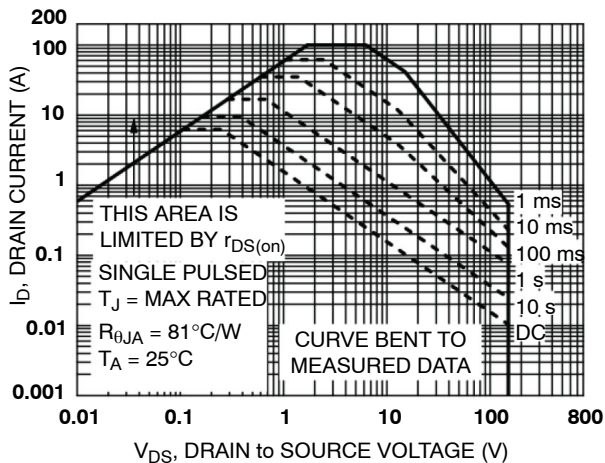


Figure 11. Forward Bias Safe Operating Area

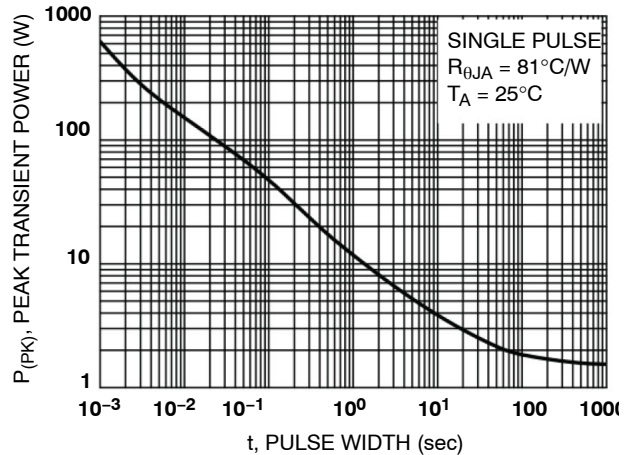


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

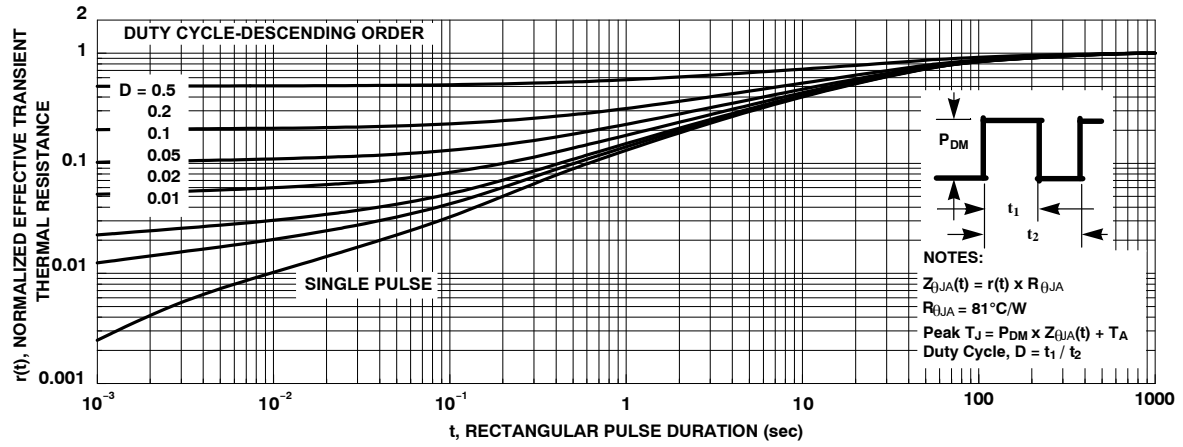


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

POWERTRENCH is a registered trademark and SyncFET is a trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

DUAL COOL is a trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

MECHANICAL CASE OUTLINE

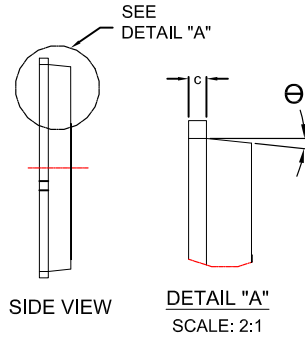
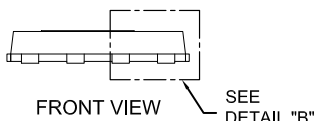
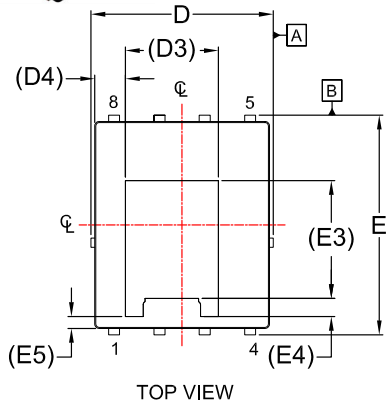
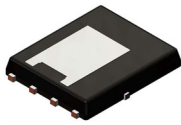
PACKAGE DIMENSIONS

ON Semiconductor®



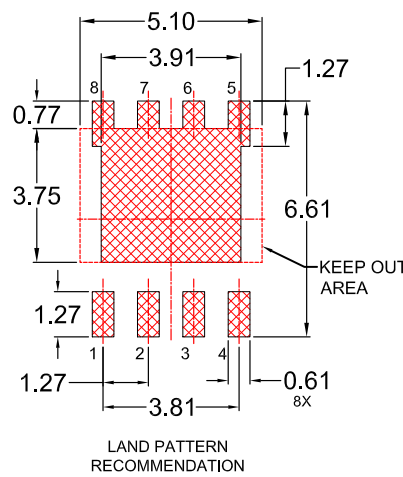
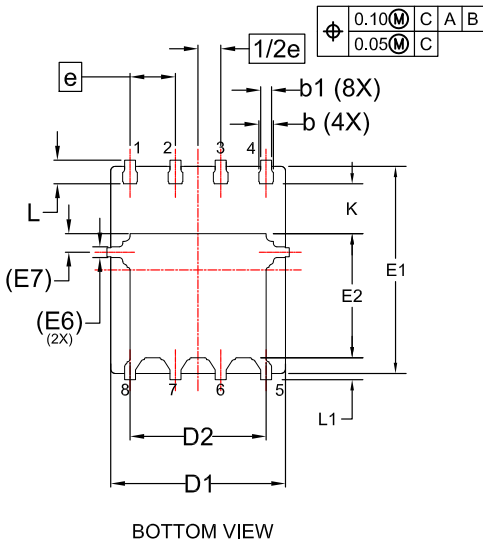
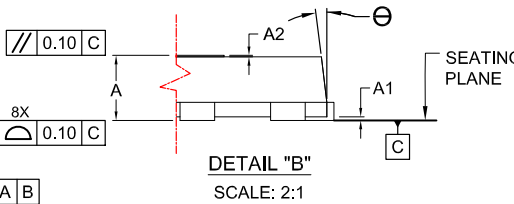
DFN8 5x6.15, 1.27P, DUAL COOL CASE 506EG ISSUE D

DATE 25 AUG 2020



NOTES:

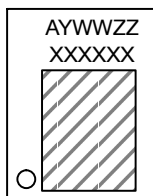
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

| DIM | MILLIMETERS | | |
|------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.85 | 0.90 | 0.95 |
| A1 | - | - | 0.05 |
| A2 | - | - | 0.05 |
| b | 0.31 | 0.41 | 0.51 |
| b1 | 0.21 | 0.31 | 0.41 |
| c | 0.20 | 0.25 | 0.30 |
| D | 4.90 | 5.00 | 5.10 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.67 | 3.82 | 3.97 |
| D3 | 2.60 REF | | |
| D4 | 0.86 REF | | |
| E | 6.05 | 6.15 | 6.25 |
| E1 | 5.70 | 5.80 | 5.90 |
| E2 | 3.38 | 3.48 | 3.58 |
| E3 | 3.30 REF | | |
| E4 | 0.50 REF | | |
| E5 | 0.34 REF | | |
| E6 | 0.30 REF | | |
| E7 | 0.52 REF | | |
| e | 1.27 BSC | | |
| 1/2e | 0.635 BSC | | |
| K | 1.30 | 1.40 | 1.50 |
| L | 0.56 | 0.66 | 0.76 |
| L1 | 0.52 | 0.62 | 0.72 |
| θ | 0° | --- | 12° |

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|------------------|-------------------------------|--|
| DOCUMENT NUMBER: | 98AON84257G | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | DFN8 5x6.15, 1.27P, DUAL COOL | PAGE 1 OF 1 |

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative