NB7V586M

1.8V Differential 2:1 Mux Input to 1.2V/1.8V 1:6 CML Clock/Data Fanout Buffer / Translator

Multi−Level Inputs w/ Internal Termination

Description

The NB7V586M is a differential 1−to−6 CML Clock/Data Distribution chip featuring a 2:1 Clock/Data input multiplexer with an input select pin. The INx/$\overline{\text{INx}}$ inputs incorporate internal 50 Ω termination resistors and will accept differential LVPECL, CML, or LVDS logic levels (see Figure 12). The INx/$\overline{\text{INx}}$ inputs and core logic are powered with a 1.8 V supply. The NB7V586M produces six identical differential CML output copies of Clock or Data. The outputs are configured as three banks of two differential pair. Each bank (or all three banks) have the flexibility of being powered by any combination of either a 1.8 V or 1.2 V supply.

The 16 mA differential CML output structure provides matching internal 50 Ω source terminations and 400 mV output swings when externally terminated with a 50 Ω resistor to $V_{CCO}x$ (see Figure 11).

The 1:6 fanout design was optimized for low output skew and minimal jitter and is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications operating up to 6 GHz or 10 Gb/s typical. The V_{REFAC} reference outputs can be used to rebias capacitor−coupled differential or single−ended input signals.

The NB7V586M is offered in a low profile 5x5 mm 32−pin Pb−Free QFN package. Application notes, models, and support documentation are available at www.onsemi.com.

The NB7V586M is a member of the GigaComm™ family of high performance clock products.

Features

- Maximum Input Data Rate > 10 Gb/s Typical
- Data Dependent Jitter < 10 ps
- Maximum Input Clock Frequency > 6 GHz Typical
- Random Clock Jitter < 0.8 ps RMS, Max
- Low Skew 1:6 CML Outputs, 20 ps Max
- 2:1 Multi−Level Mux Inputs
- 175 ps Typical Propagation Delay
- 50 ps Typical Rise and Fall Times
- Differential CML Outputs, 330 mV Peak−to−Peak, Typical
- Operating Range: V_{CC} = 1.71 V to 1.89 V
- Operating Range: $V_{CCO}x$ = 1.14 V to 1.89 V
- Internal 50 Ω Input Termination Resistors
- V_{REFAC} Reference Output
- QFN32 Package, 5 mm x 5 mm
- −40°C to +85°C Ambient Operating Temperature
- These are Pb−Free Devices

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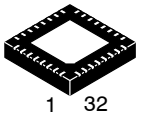
MARKING DIAGRAM*

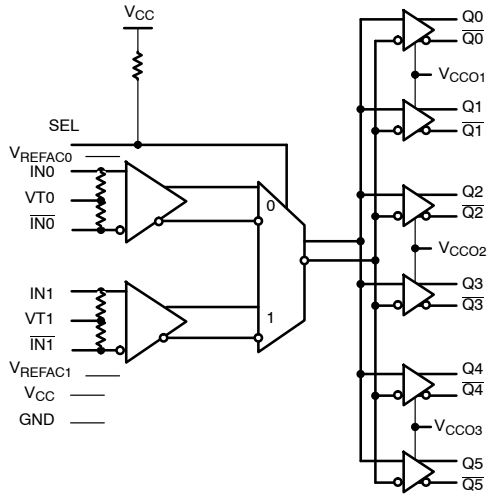


QFN32
MN SUFFIX
CASE 488AM

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G or ▪	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

SIMPLIFIED LOGIC DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

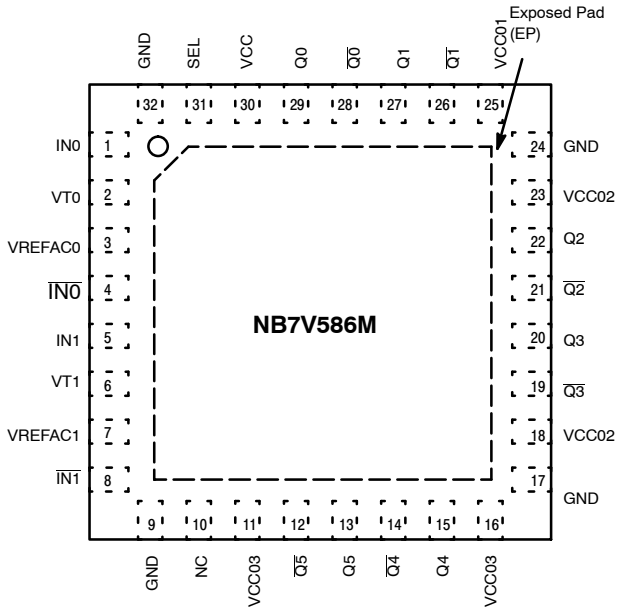


Figure 1. 32−Lead QFN Pinout (Top View)

Table 1. INPUT SELECT FUNCTION TABLE

SEL*	CLK Input Selected
0	IN0
1	IN1

*Defaults HIGH when left open.

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1,4 5,8	IN0, $\overline{IN0}$ IN1, $\overline{IN1}$	LVPECL, CML, LVDS Input	Non−inverted, Inverted, Differential Inputs
2,6	VT0, VT1		Internal 100 Ω Center−tapped Termination Pin for IN0/$\overline{IN0}$ and IN1/$\overline{IN1}$
31	SEL	LVTTL/LVCMOS Input	Input Select pin; LOW for IN0 Inputs, HIGH for IN1 Inputs; defaults HIGH when left open
10	NC	−	No Connect
30	VCC	−	1.8 V Positive Supply Voltage for the Inputs and Core Logic.
25	VCCO1		1.2 V or 1.8 V Positive Supply Voltage for the Q0, $\overline{Q0}$, Q1, $\overline{Q1}$ CML Outputs
18, 23	VCCO2	−	1.2 V or 1.8 V Positive Supply Voltage for the Q2, $\overline{Q2}$, Q3, $\overline{Q3}$ CML Outputs
11, 16	VCCO3		1.2 V or 1.8 V Positive Supply Voltage for the Q4, $\overline{Q4}$, Q5, $\overline{Q5}$ CML Outputs
29, 28 27, 26	Q0, $\overline{Q0}$ Q1, $\overline{Q1}$	1.2 V or 1.8 V CML Output	Non−inverted, Inverted Differential Outputs; powered by VCCO1 (Notes 1 and 2).
22, 21 20, 19	Q2, $\overline{Q2}$ Q3, $\overline{Q3}$	1.2 V or 1.8 V CML Output	Non−inverted, Inverted Differential Outputs; powered by VCCO2 (Notes 1 and 2).
15, 14 13, 12	Q4, $\overline{Q4}$ Q5, $\overline{Q5}$	1.2 V or 1.8 V CML Output	Non−inverted, Inverted Differential Outputs; powered by VCCO3 (Notes 1 and 2).
9, 17, 24, 32	GND		Negative Supply Voltage, connected to Ground
3 7	VREFAC0 VREFAC1	−	Output Voltage Reference for Capacitor−Coupled Inputs, only
−	EP	−	The Exposed Pad (EP) on the QFN−32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to the die, and must be electrically and thermally connected to GND on the PC board.

1. In the differential configuration when the input termination pins (VT0, VT1) are connected to a common termination voltage or left open, and if no signal is applied on INn/$\overline{INn}$ input, then, the device will be susceptible to self−oscillation. Qn/$\overline{Qn}$ outputs have internal 50 Ω source termination resistors.
2. All V_{CC}, VCC0x and GND pins must be externally connected to a power supply for proper operation.

Table 3. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
Input Pullup Resistor (R_{PU})		75 kΩ
Moisture Sensitivity (Note 3)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		308
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		3.0	V
V_{CCOx}	Positive Power Supply	GND = 0 V		3.0	V
V_{IO}	Input/Output Voltage	GND = 0 V	$-0.5 \le V_{IO} \le V_{CC} + 0.5$	-0.5 to $V_{CC} + 0.5$	V
V_{INPP}	Differential Input Voltage $\lvert IN_x - \overline{IN_x}\rvert$			1.89	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)			±40	mA
I_{OUT}	Output Current	Continuous Surge		34 40	mA
$I_{VFREFAC}$	V_{REFAC} Sink/Source Current			±1.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 4)	0 lfpm 500 lfpm	QFN−32 QFN−32	31 27	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case) (Note 4)	Standard Board	QFN−32	12	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS – CML OUTPUT V_{CC} = 1.8 V ±5%, V_{CCO1} = 1.2 V ±5% or 1.8 V ±5%, V_{CCO2} = 1.2 V ±5% or 1.8 V ±5%, V_{CCO3} = 1.2 V ±5% or 1.8 V ±5%, GND = 0 V, T_A = −40°C to 85°C (Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY CURRENT (Inputs and Outputs open)					
I_{CC} I_{CCO}	Power Supply Current for V_{CC} (Inputs and Outputs Open) Power Supply Current for VCCOx (Inputs and Outputs Open)		75 95	125 105	mA
CML OUTPUTS (Note 6)					
V_{OH}	Output HIGH Voltage V_{CC} = 1.8 V, VCCOx = 1.8 V V_{CC} = 1.8 V, VCCOx = 1.2 V	V_{CCOx} − 40 1760 1160	V_{CCOx} − 20 1780 1180	V_{CCOx} 1800 1200	mV
V_{OL}	Output LOW Voltage V_{CC} = 1.8 V, VCCOx = 1.8 V V_{CC} = 1.8 V, VCCOx = 1.2 V	V_{CCOx} − 500 1300 700	V_{CCOx} − 400 1400 800	V_{CCOx} − 275 1525 925	mV
DIFFERENTIAL INPUTS DRIVEN SINGLE−ENDED (Note 7) (Figure 6)					
V_{th}	Input Threshold Reference Voltage Range (Note 8)	1050		V_{CC} − 100	mV
V_{IH}	Single−Ended Input HIGH Voltage	V_{th} + 100		V_{CC}	mV
V_{IL}	Single−Ended Input LOW Voltage	GND		V_{th} − 100	mV
V_{ISE}	Single−Ended Input Voltage (V_{IH} − V_{IL})	200		1200	mV
V_{REFAC}					
V_{REFAC}	Output Reference Voltage @ 100 μA for Capacitor − Coupled Inputs, Only	V_{CC} − 550	V_{CC} − 450	V_{CC} − 300	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Note 9) (Figures 4 and 7)					
V_{IHD}	Differential Input HIGH Voltage (IN, $\overline{IN}$)	1100		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage (IN, $\overline{IN}$)	GND		V_{CC} − 100	mV
V_{ID}	Differential Input Voltage (IN, $\overline{IN}$) (V_{IHD} − V_{ILD})	100		1200	mV
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 10) (Figure 9)	1050		V_{CC} − 50	mV
I_{IH}	Input HIGH Current IN/$\overline{IN}$ (VTO / VT1 Open)	−150		150	μA
I_{IL}	Input LOW Current IN/$\overline{IN}$ (VTO / VT1 Open)	−150		150	μA
CONTROL INPUT (SEL Pin)					
V_{IH}	Input HIGH Voltage for Control Pin	V_{CC} x 0.65		V_{CC}	mV
V_{IL}	Input LOW Voltage for Control Pin	GND		V_{CC} x 0.35	mV
I_{IH}	Input HIGH Current	−150	20	+150	μA
I_{IL}	Input LOW Current	−150	5	+150	μA
TERMINATION RESISTORS					
R_{TIN}	Internal Input Termination Resistor (Measured from INx to VTx)	45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor	45	50	55	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input parameters vary 1:1 with V_{CC}. and output parameters vary 1:1 with V_{CCOx}.
6. CML outputs (Qn/$\overline{Qn}$) have internal 50 Ω source termination resistors and must be externally terminated with 50 Ω to V_{CCOx} for proper operation.
7. V_{th}, V_{IH}, V_{IL} and V_{ISE} parameters must be complied with simultaneously.
8. V_{th} is applied to the complementary input when operating in single−ended mode.
9. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.
10. V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.

Table 6. AC CHARACTERISTICS V_{CC} = 1.8 V ±5%, V_{CCO1} = 1.2 V ±5% or 1.8 V ±5%, V_{CCO2} = 1.2 V ±5% or 1.8 V ±5%, V_{CCO3} = 1.2 V ±5% or 1.8 V ±5%, GND = 0 V, T_A = −40°C to 85°C (Note 11)

Symbol	Characteristic		Min	Typ	Max	Unit
f_{MAX}	Maximum Input Clock Frequency, $V_{OUTPP} \geq$ 200 mV		4.0	6.0		GHz
$f_{DATAMAX}$	Maximum Operating Input Data Rate (PRBS23)		10			Gbps
V_{OUTPP}	Output Voltage Amplitude (See Figures 4, Note 15)	$f_{in} \leq$ 4.0 GHz	200	330		mV
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential @ 1 GHz, Measured at Differential Crosspoint	$IN_x/\overline{IN_x}$ to $Q_n/\overline{Q_n}$ SEL to Q_n	125 125	175	250 300	ps
t_{PLH} TC	Propagation Delay Temperature Coefficient			100		fs/°C
t_{SKEW}	Output − Output Skew (Within Device) (Note 12) Device − Device Skew (t_{pd} Max − t_{pdmin})				30 50	ps
t_{DC}	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	$f_{in} \leq$ 4.0 GHz	45	50	55	%
t_{JITTER}	Output Random Jitter (RJ) (Note 13) Deterministic Jitter (DJ) (Note 14)	$f_{in} \leq$ 4.0 GHz 10 Gbps		0.2	0.8 10	ps rms ps pk−pk
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 15)		100		1200	mV
t_r, t_f	Output Rise/Fall Times @ 1 GHz (20% − 80%)	Q_n, $\overline{Q_n}$		50	65	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Measured using a 400 mV source, 50% duty cycle clock source. All outputs must be loaded with external 50 Ω to V_{CCOx}. Input edge rates 40 ps (20% − 80%).
12. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from cross−point of the inputs to the crosspoint of the outputs.
13. Additive RMS jitter with 50% duty cycle clock signal.
14. Additive Peak−to−Peak data dependent jitter with input NRZ data at PRBS23.
15. Input and output voltage swing is a single−ended measurement operating in differential mode.

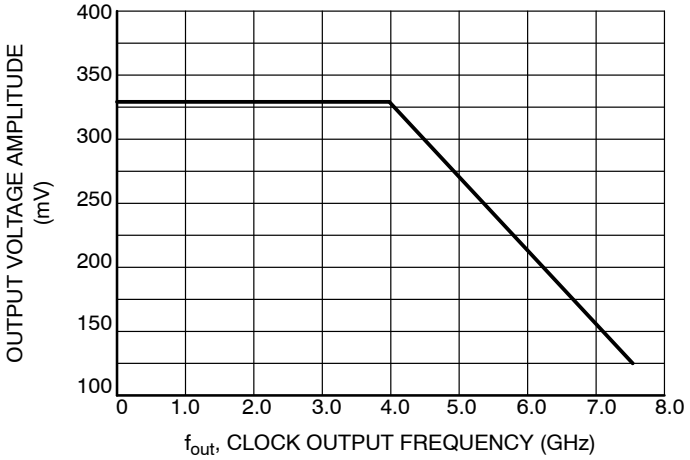


Figure 2. Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)

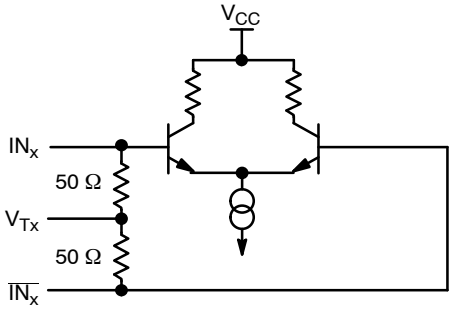


Figure 3. Input Structure

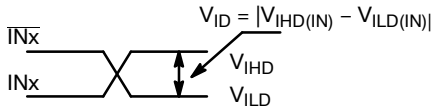


Figure 4. Differential Inputs Driven Differentially

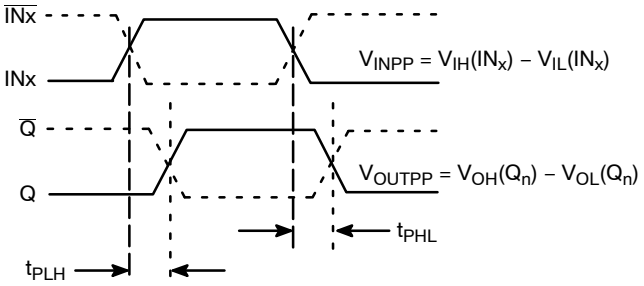


Figure 5. AC Reference Measurement

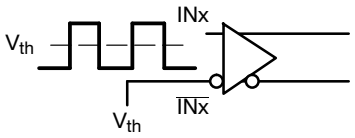


Figure 6. Differential Input Driven Single−Ended

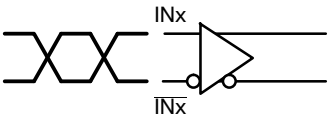


Figure 7. Differential Inputs Driven Differentially

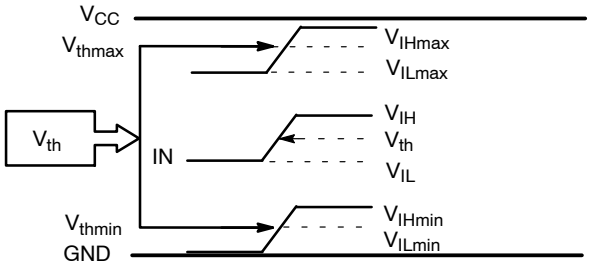


Figure 8. V_{th} Diagram

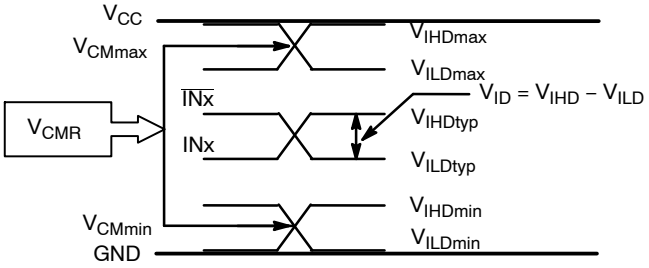


Figure 9. V_{CMR} Diagram

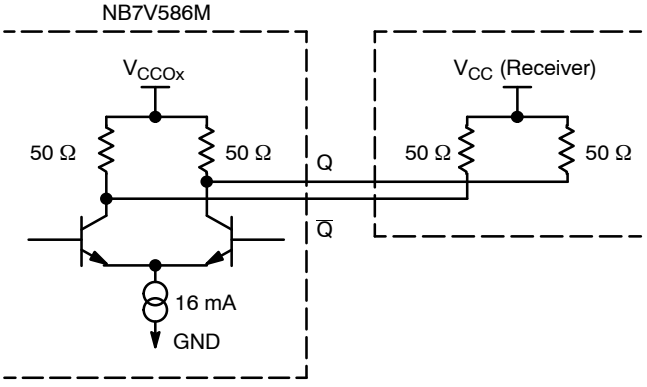


Figure 10. Typical CML Output Structure and Termination

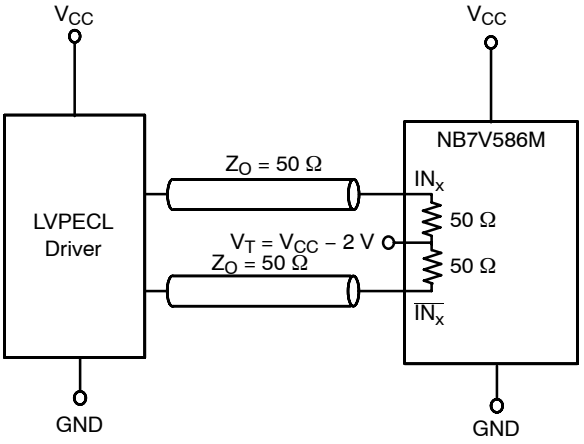


Figure 11. LVPECL Interface

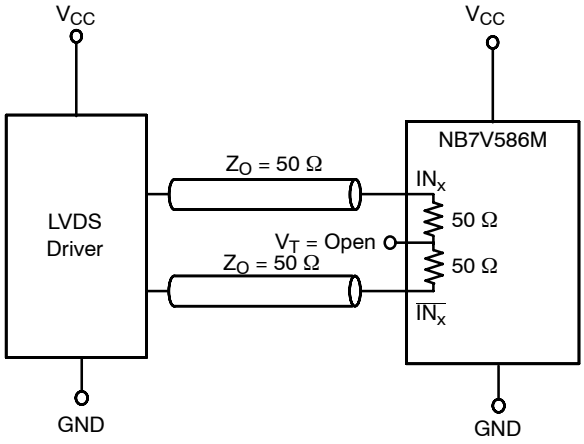


Figure 12. LVDS Interface

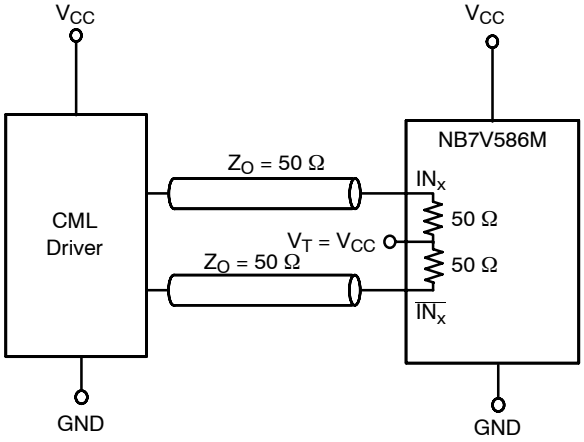


Figure 13. Standard 50 Ω Load CML Interface

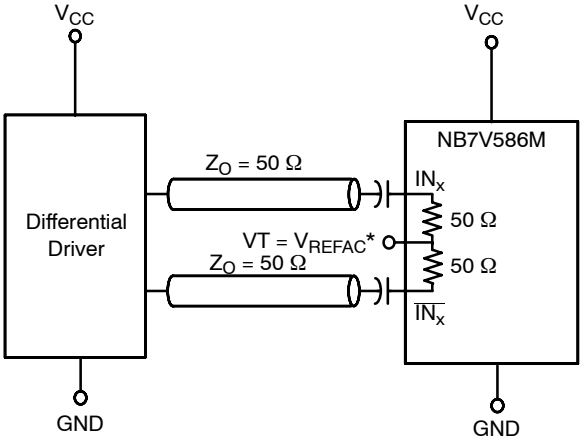


Figure 14. Capacitor−Coupled Differential Interface (V_T Connected to V_{REFAC})

*V_{REFAC} bypassed to ground with a 0.01 μF capacitor

ORDERING INFORMATION

Device	Package	Shipping†
NB7V586MMNG	QFN32 (Pb−Free)	74 Units / Rail
NB7V586MMNR4G	QFN32 (Pb−Free)	1000 / Tape & Reel

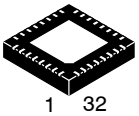
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

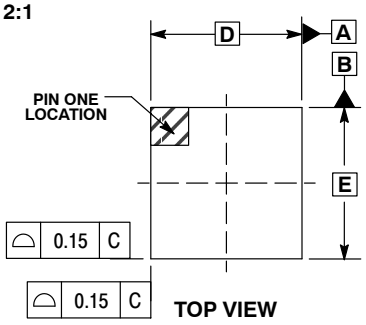
ON Semiconductor®

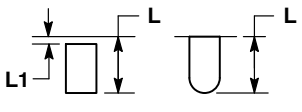
QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

DATE 23 OCT 2013

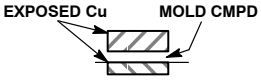


SCALE 2:1

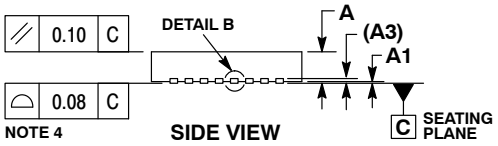


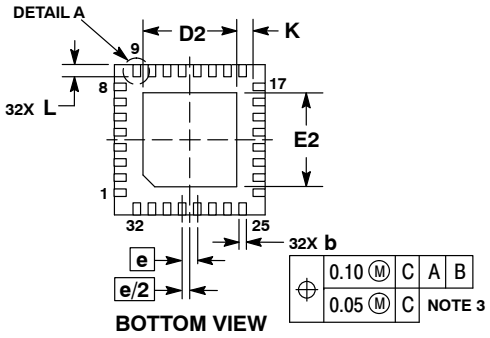


DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION

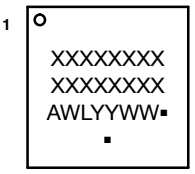




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*

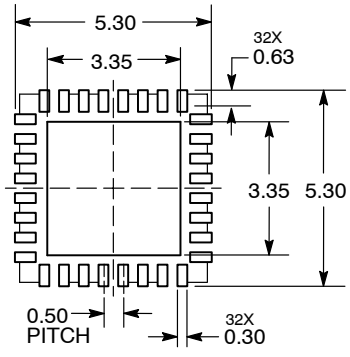


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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