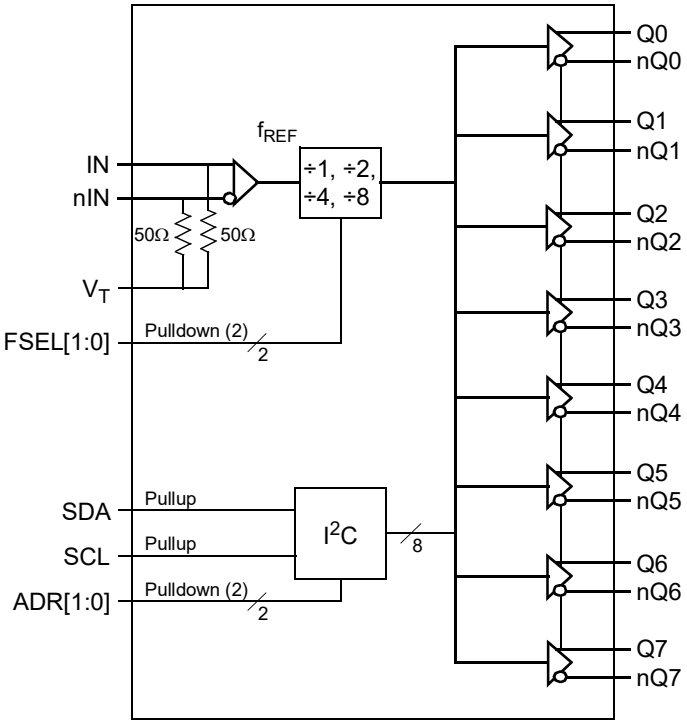
General Description

The 8T73S208B-01 is a high-performance differential LVPECL clock divider and fanout buffer. The device is designed for the frequency division and signal fanout of high-frequency, low phase-noise clocks. The 8T73S208B-01 is characterized to operate from a 2.5V and 3.3V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the 8T73S208B-01 ideal for those clock distribution applications demanding well-defined performance and repeatability. The integrated input termination resistors make interfacing to the reference source easy and reduce passive component count. Each output can be individually enabled or disabled in the high-impedance state controlled by a I^2C register. On power-up, all outputs are disabled.

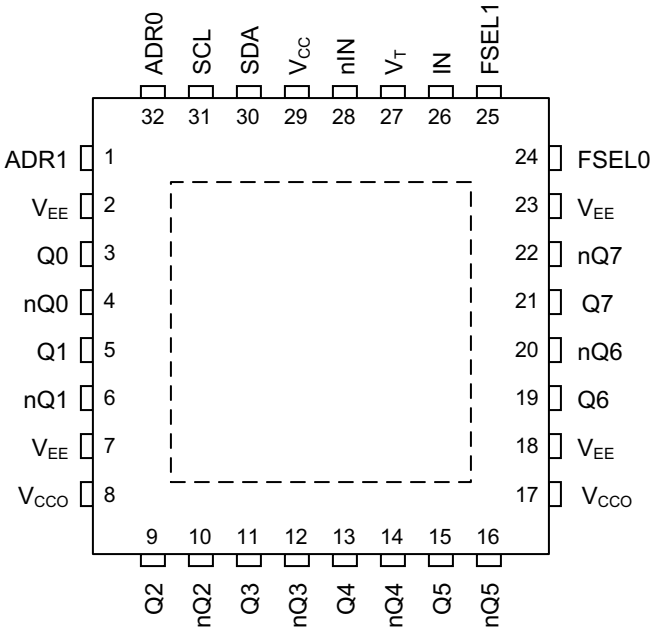
Features

- One differential input reference clock
- Differential pair can accept the following differential input levels: LVDS, LVPECL, CML
- Integrated input termination resistors
- Eight LVPECL outputs
- Selectable clock frequency division of ÷1, ÷2, ÷4 and ÷8
- Maximum input clock frequency: 1GHz
- LVCMOS interface levels for the control inputs
- Individual output enable/disabled by I^2C interface
- Power-up state: all outputs disabled
- Output skew: 60ps (maximum)
- Output rise/fall times: 350ps (maximum)
- Low additive phase jitter, RMS: 182fs (typical)
- Full 2.5V and 3.3V supply voltages
- Lead-free (RoHS 6) 32-VFQFPN packaging
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



5 × 5 mm, 32-VFQFPN

Pin Descriptions and Pin Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 32	ADR1, ADR0	Input	Pulldown	I^2C Address inputs. LVCMOS/LVTTL interface levels.
2, 7, 18, 23	V_{EE}	Power		Negative supply pins.
3, 4	Q0, nQ0	Output		Differential output pair 0. LVPECL interface levels.
5, 6	Q1, nQ1	Output		Differential output pair 1. LVPECL interface levels.
8, 17	V_{CCO}	Power		Output supply pins.
9, 10	Q2, nQ2	Output		Differential output pair 2. LVPECL interface levels.
11, 12	Q3, nQ3	Output		Differential output pair 3. LVPECL interface levels.
13, 14	Q4, nQ4	Output		Differential output pair 4. LVPECL interface levels.
15, 16	Q5, nQ5	Output		Differential output pair 5. LVPECL interface levels.
19, 20	Q6, nQ6	Output		Differential output pair 6. LVPECL interface levels.
21, 22	Q7, nQ7	Output		Differential output pair 7. LVPECL interface levels.
24, 25	FSEL0, FSEL1	Input	Pulldown	Frequency divider select controls. See Table 3A for function. LVCMOS/LVTTL interface levels.
26	IN	Input		Non-inverting differential clock input. RT = 50Ω termination to V_T.
27	V_T	Termination Input		Input for termination. Both IN and nIN inputs are internally terminated 50Ω to this pin. See input termination information in Section, “Applications Information”.
28	nIN	Input		Inverting differential clock input. RT = 50Ω termination to V_T.
29	V_{CC}	Power		Power supply pin.
30	SDA	I/O	Pullup	I^2C Data Input/Output. Input: LVCMOS/LVTTL interface levels. Output: open drain.
31	SCL	Input	Pullup	I^2C Clock Input. LVCMOS/LVTTL interface levels.

NOTE: *Pulldown* and *Pullup* refers to an internal input resistors. See Section, “Table 2. Pin Characteristics” values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Tables

Input Frequency Divider Operation

The FSEL1 and FSEL0 control pins configure the input frequency divider. In the default state (FSEL[1:0] are set to logic 0:0 or left open) the output frequency is equal to the input frequency (divide-by-1). The other FSEL[1:0] settings configure the input divider to divide-by-2, 4 or 8, respectively.

Table 3A. FSEL[1:0] Input Selection Function Table

Input		
FSEL1	**FSEL0**	**Operation**
0 (default)	0 (default)	$f_{Q[7:0]} = f_{REF} \div 1$
0	1	$f_{Q[7:0]} = f_{REF} \div 2$
1	0	$f_{Q[7:0]} = f_{REF} \div 4$
1	1	$f_{Q[7:0]} = f_{REF} \div 8$

NOTE: FSEL1, FSEL0 are asynchronous controls

Output Enable Operation

The output enable/disable state of each individual differential output Qx, nQx can be set by the content of the I^2C register (see Table 3C). A logic zero to an I^2C bit in register 0 enables the corresponding differential output, while a logic one disables the differential output (see Table 3B). After each power cycle, the device resets all I^2C bits (Dn) to its default state (logic 1) and all Qx, nQx outputs are disabled. After the first valid I^2C write, the output enable state is controlled by the I^2C register. Setting and changing the output enable state through the I^2C interface is asynchronous to the input reference clock.

Table 3B. Individual Output Enable Control

Bit	
Dn	**Operation**
0	Output Qx, nQx is enabled.
1 (default)	Output Qx, nQx is disabled in high-impedance state.

Table 3C. Individual output enable control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Output	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Default	1	1	1	1	1	1	1	1

I^2C Interface Protocol

The 8T73S208B-01 uses an I^2C slave interface for writing and reading the device configuration to and from the on-chip configuration registers. This device uses the standard I^2C write format for a write transaction, and a standard I^2C read format for a read transaction. Figure 1 defines the I^2C elements of the standard I^2C transaction.

These elements consist of a start bit, data bytes, an acknowledge or Not-Acknowledge bit and the stop bit. These elements are arranged to make up the complete I^2C transactions as shown in Figure 2 and Figure 3. Figure 2 is a write transaction while Figure 3 is read transaction.The 7-bit I^2C slave address of the 8T73S208B-01 is a combination of a 5-bit fixed addresses and two variable bits which are set by the hardware pins ADR[1:0] (binary 11010, ADR1, ADR0). Bit 0 of slave address is used by the bus controller to select either the read or write mode. The hardware pins ADR1 and ADR0 and should be individually set by the user to avoid address conflicts of multiple 8T73S208B-01 devices on the same bus.

Table 3D. I^2C Slave Address

7	6	5	4	3	2	1	0
1	1	0	1	0	ADR1	ADR0	R/W

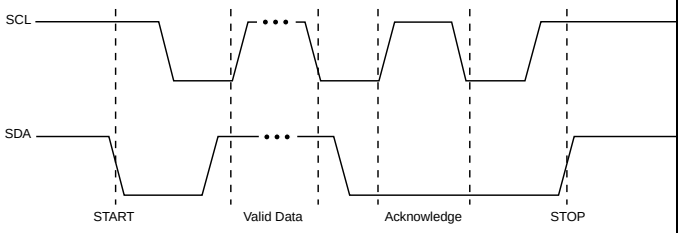


Figure 1: Standard I^2C Transaction

START (S) – defined as high-to-low transition on SDA while holding SCL HIGH.

DATA – between START and STOP cycles, SDA is synchronous with SCL. Data may change only when SCL is LOW and must be stable when SCL is HIGH.

ACKNOWLEDGE (A) – SDA is driven LOW before the SCL rising edge and held LOW until the SCL falling edge.

STOP (S) – defined as low-to-high transition on SDA while holding SCL HIGH

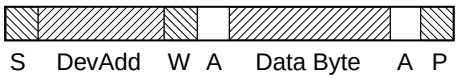


Figure 2: Write Transaction

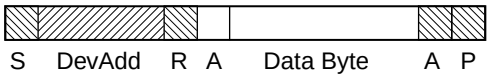


Figure 3: Read Transaction

S –Start or Repeated Start
W –R/W is set for Write
R –R/W is set for Read
A –Ack
DevAdd –7 bit Device Address
P –Stop

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Input Termination Current, I_{VT}	±35mA
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Storage Temperature, T_{STG}	-65°C to 150°C
Maximum Junction Temperature, T_{JMAX}	125°C
ESD - Human Body Model[a]	2000V
ESD - Charged Device Model	500V

[a] According to JEDEC/JS-001-2012/JESD22-C101E.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = V_{CCO} = 2.5V ± 5% or 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5V	2.625	V
V_{CC}	Power Supply Voltage		3.135	3.3V	3.465	V
V_{CCO}	Output Supply Voltage		2.375	2.5V	2.625	V
V_{CCO}	Output Supply Voltage		3.135	3.3V	3.465	V
I_{EE}	Power Supply Current			92	110	mA

Table 4B. LVCMOS/LVTTL Input DC Characteristics, V_{CC} = V_{CCO} = 2.5V ± 5% or 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage[a]	FSEL[1:0], ADR[1:0]	V_{CC} = 3.3V ±5%	2.2		V_{CC} + 0.3V	V
		SCL, SDA	V_{CC} = 3.3V ±5%	2.4		V_{CC} + 0.3V	V
		FSEL[1:0], ADR[1:0]	V_{CC} = 2.5V ±5%	1.7		V_{CC} + 0.3V	V
		SCL, SDA	V_{CC} = 2.5V ±5%	1.9		V_{CC} + 0.3V	V
V_{IL}	Input Low Voltage[a]	FSEL[1:0], ADR[1:0]	V_{CC} = 3.3V ±5%	-0.3		0.8	V
		SCL, SDA	V_{CC} = 3.3V ±5%	-0.3		0.8	V
		FSEL[1:0], ADR[1:0]	V_{CC} = 2.5V ±5%	-0.3		0.7	V
		SCL, SDA	V_{CC} = 2.5V ±5%	-0.3		0.5	V
I_{IH}	Input High Current	FSEL[1:0], ADR[1:0]	V_{CC} = V_{IN} = 2.625 or 3.465V			150	µA
		SCL, SDA	V_{CC} = V_{IN} = 2.625 or 3.465V			10	µA
I_{IL}	Input Low Current	FSEL[1:0], ADR[1:0]	V_{CC} = 2.625 or 3.465V, V_{IN} = 0V	-10			µA
		SCL, SDA	V_{CC} = 2.625 or 3.465V, V_{IN} = 0V	-150			µA

[a] V_{IL} should not be lower than -0.3V and V_{IH} should not be higher than V_{CC} + 0.3V.

Table 4C. Differential Input DC Characteristics, V_{CC} = V_{CCO} = 2.5V ± 5% or 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IN}	Input Voltage Swing[a]	IN, nIN		0.15		1.2	V
V_{CMR}	Common Mode Input Voltage[b]			1.2		V_{CC} – (V_{IN}/2)	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3		2.4	V
R_{IN}	Input Resistance	IN, nIN	IN, nIN to V_T	40	50	60	Ω
R_{IN_DIFF}	Differential Input Resistance	IN, nIN	IN to nIN, V_T = Open	80	100	120	Ω

[a] V_{IL} should not be less than -0.3V and V_{IH} should not be greater than V_{CC}

[b] *Common Mode Input Voltage* is defined as the cross point.

Table 4D. LVPECL DC Characteristics, V_{CC} = V_{CCO} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[a]		V_{CCO} – 1.102	V_{CCO} – 0.95	V_{CCO} – 0.775	V
V_{OL}	Output Low Voltage[a]		V_{CCO} – 1.802	V_{CCO} – 1.6	V_{CCO} – 1.367	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6	0.7	1.0	V

[a] Outputs terminated with 50Ω to V_{CCO} – 2V.

Table 4E. LVPECL DC Characteristics, V_{CC} = V_{CCO} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[a]		V_{CCO} – 1.125	V_{CCO} – 0.95	V_{CCO} – 0.767	V
V_{OL}	Output Low Voltage		V_{CCO} – 1.799	V_{CCO} – 1.6	V_{CCO} – 1.359	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.60	0.65	1.00	V

[a] Outputs terminated with 50Ω to V_{CCO} – 2V.

AC Electrical Characteristics

Table 5. AC Electrical Characteristics, V_{CC} = V_{CCO} = 2.5V ± 5% or 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter[a]		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency	IN, nIN				1	GHz
f_{SCL}	I^2C Clock Frequency					400	kHz
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, measured with FSEL[1:0] = 00		f_{REF} =156.25MHz, Integration Range: 12kHz – 20MHz VCCO_SEL[i] = 3.3V ±5%		94	145	fs
			f_{REF} =156.25MHz, Integration Range: 12kHz – 20MHz VCCO_SEL[i] = 2.5V ±5%		106	163	fs
t_{PD}	Propagation Delay[b]	IN, nIN to Qx, nQx	FSEL[1:0] = 00	350		750	ps
			FSEL[1:0] = 01	500		870	ps
			FSEL[1:0] = 10	550		1052	ps
			FSEL[1:0] = 11	650		1230	ps
*t*sk(o)	Output Skew[c], [d]					60	ps
*t*sk(p)	Pulse Skew					50	ps
*t*sk(pp)	Part-to-Part Skew[3], [e], [f]					500	ps
odc	Output Duty Cycle[g]		Any Frequency		50		%
			at f_{REF} = 100MHz	48	50	52	%
			at f_{REF} = 125MHz	48	50	52	%
			at f_{REF} = 156.25MHz	48	50	52	%
t_{PDZ}	Output Enable and Disable Time[h]		Output Enable/ Disable State from/ to Active/ Inactive		1		µs
t_R / t_F	Output Rise/Fall Time		20% to 80%		140	205	ps
			10% to 90%		180	350	ps

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Measured from the differential input crossing point to the differential output cross point.

[c] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross point.

[d] This parameter is defined in accordance with JEDEC Standard 65.

[e] Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross point.

[f] Part-to-part skew specification does not guarantee divider synchronization among devices.

[g] If FSEL[1:0] = 00 (divide-by-one), the output duty cycle will depend on the input duty cycle.

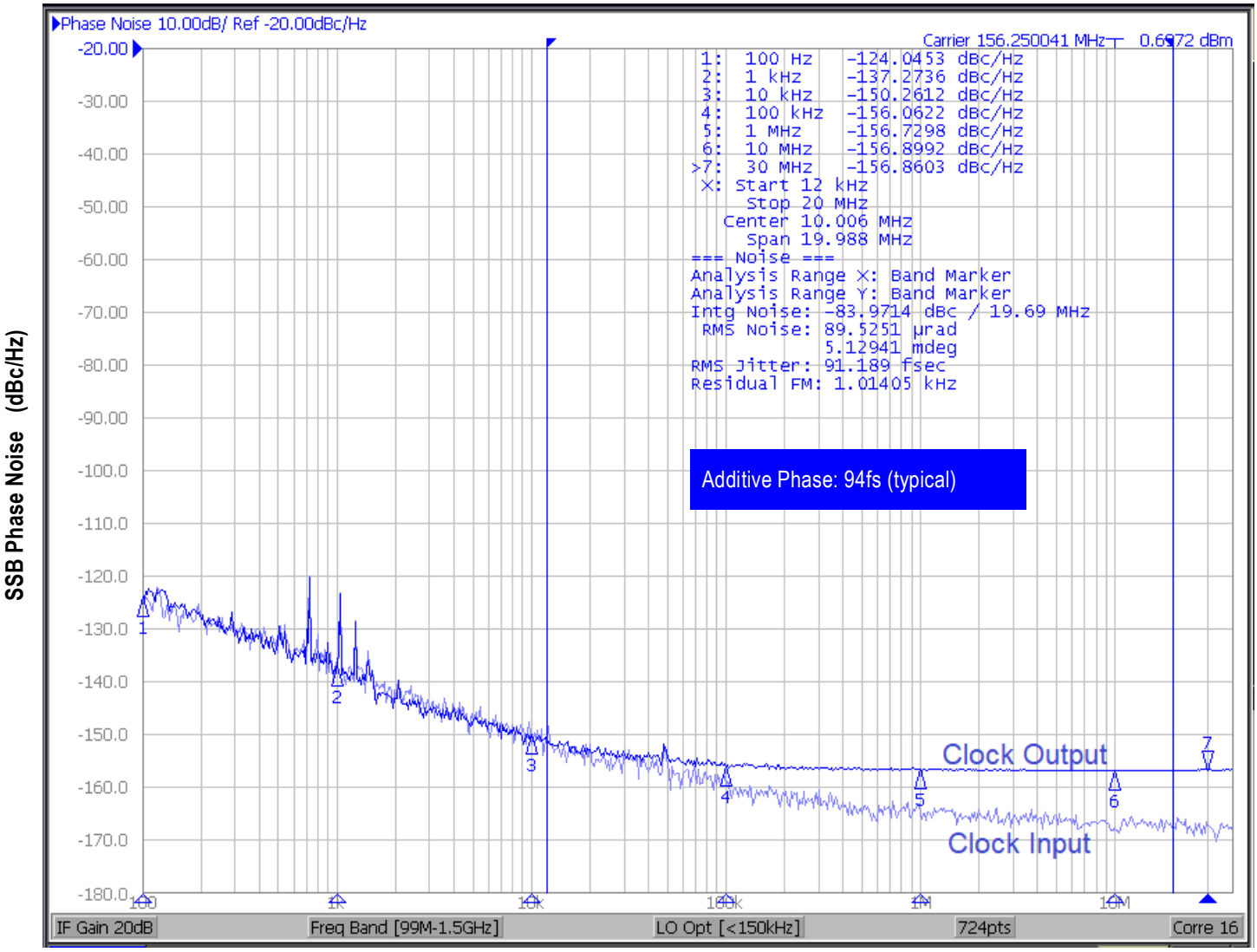
[h] Measured from SDA rising edge of I^2C stop command.

[I] Characterized using the Wenzel 156.25MHz Model: 500-23697 Clock Generator as the input source.

Additive Phase Jitter

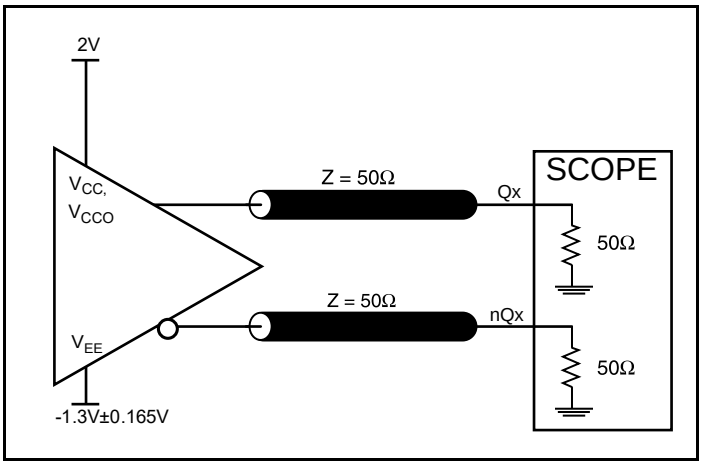
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

Typical Phase Jitter at 156.25MHz

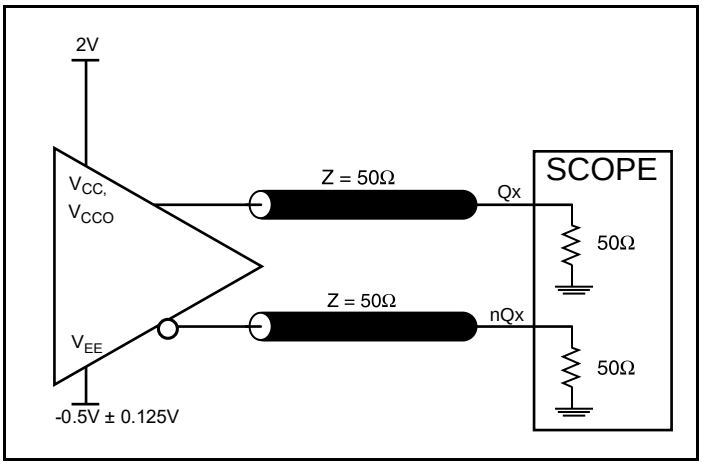


Input source: Wenzel 156.25MHz Model: 500-23697 Clock Generator.

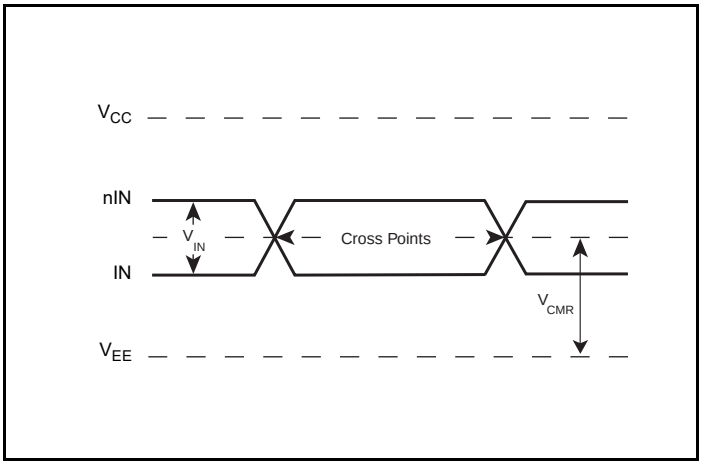
Parameter Measurement Information



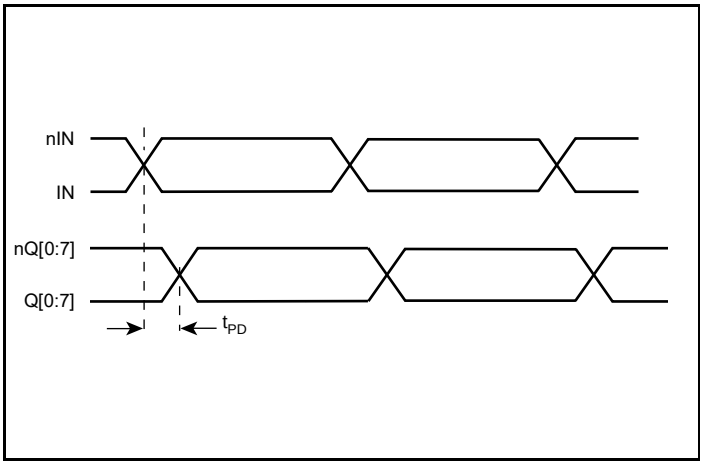
3.3V Core/3.3V LVPECL Output Load AC Test Circuit



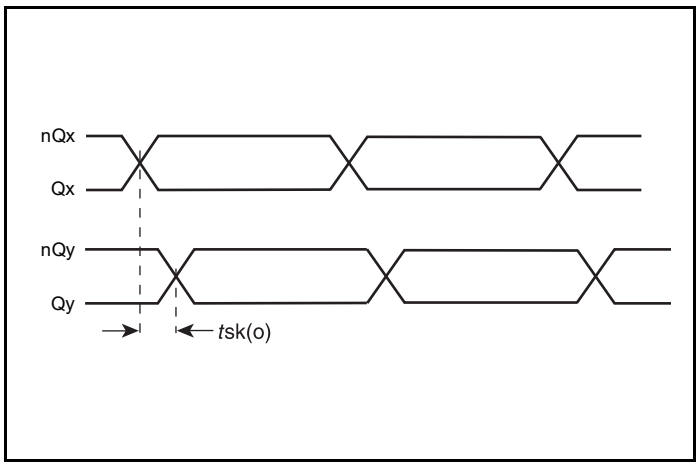
2.5V Core/2.5V LVPECL Output Load AC Test Circuit



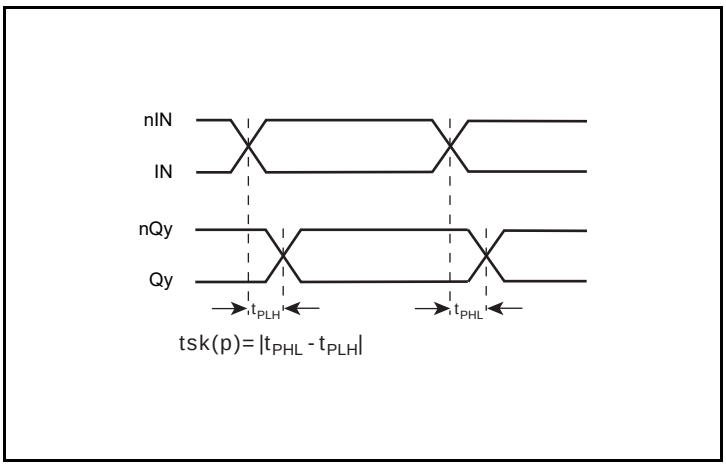
Differential Input Level



Propagation Delay

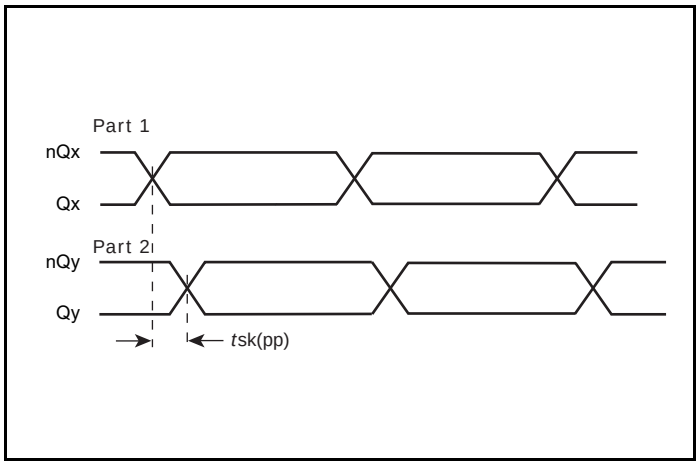


Output Skew

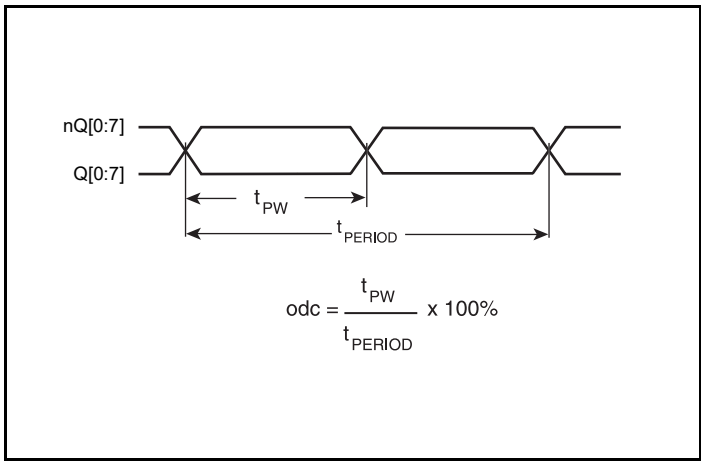


Pulse Skew

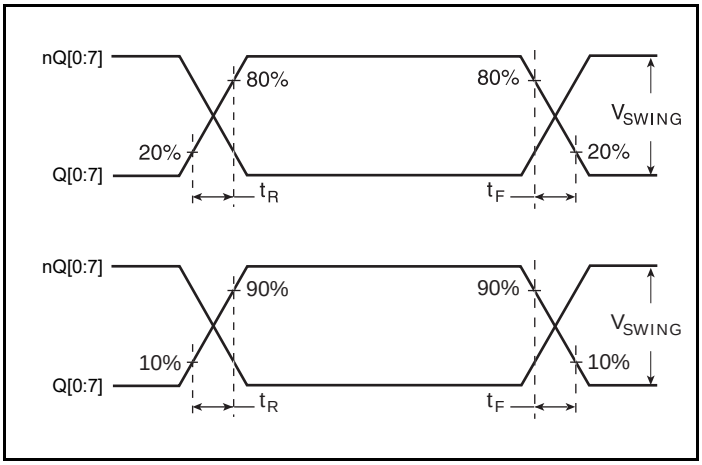
Parameter Measurement Information, continued



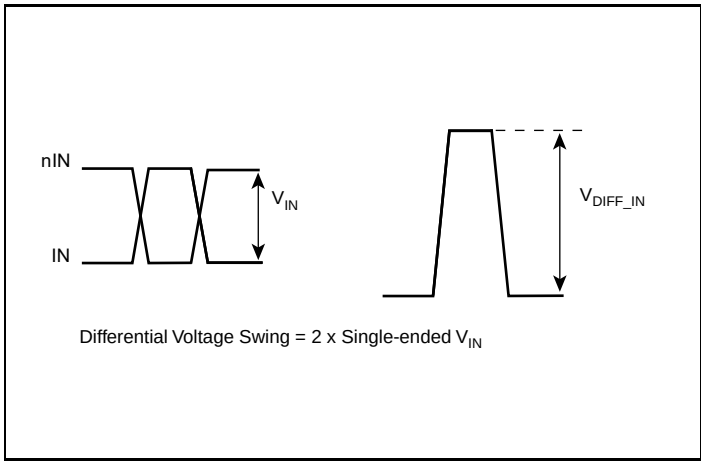
Part-to-Part Skew



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Times



Single-Ended and Differential Input Voltage Swing

Applications Information

3.3V Differential Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the V_{IN} and V_{CMR} input requirements. *Figures 4A* to 4*C* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

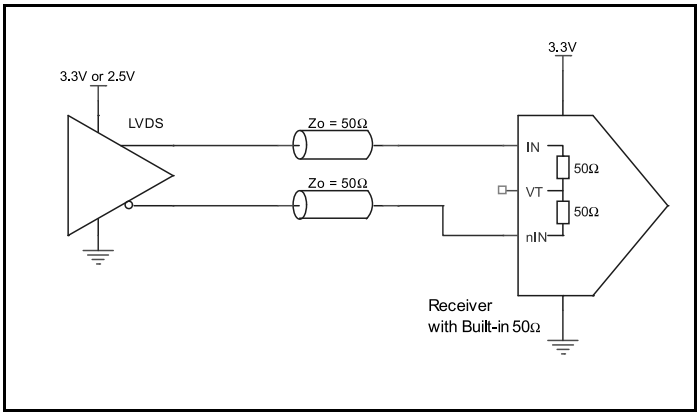


Figure 4A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

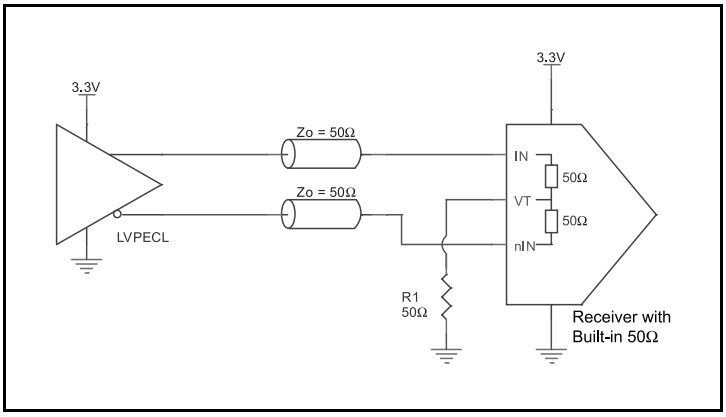


Figure 4B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

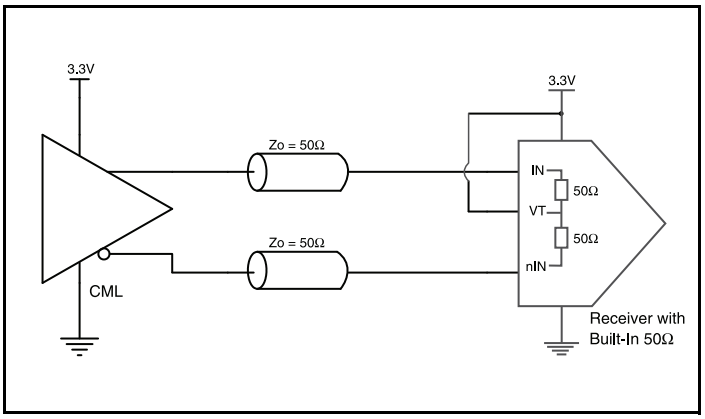


Figure 4C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver

2.5V LVPECL Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the V_{IN} and V_{CMR} input requirements. *Figures 5A* to *5C* show interface examples for the IN/nIN with built-in 50Ω termination input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

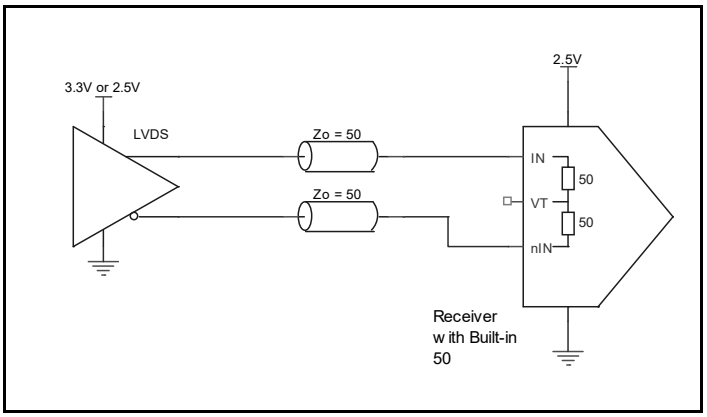


Figure 5A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

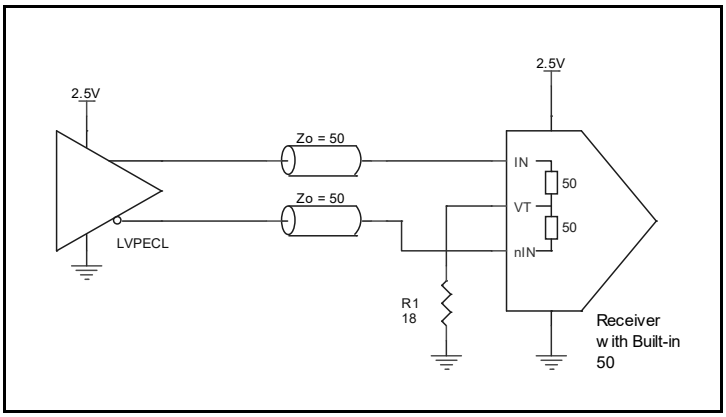


Figure 5B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

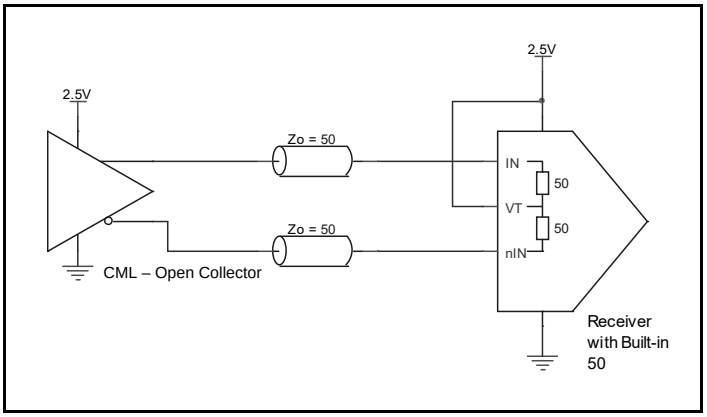


Figure 5C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

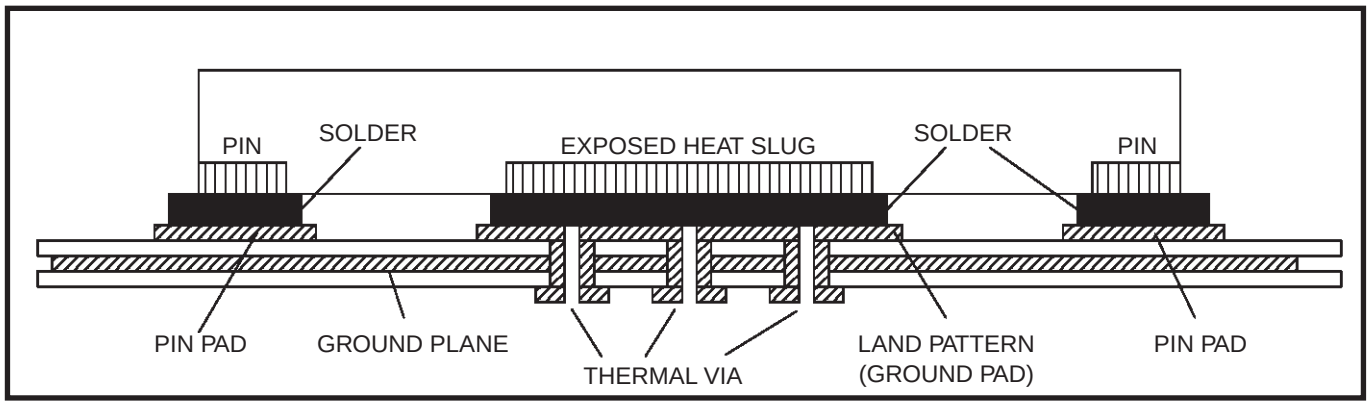


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

Any unused LVPECL output pair can be left floating. We recommend that there is no trace attached.

Termination for 3.3V LVPECL Outputs

Figures 7A and *7B* are examples of 3.3V LVPECL output DC terminations.

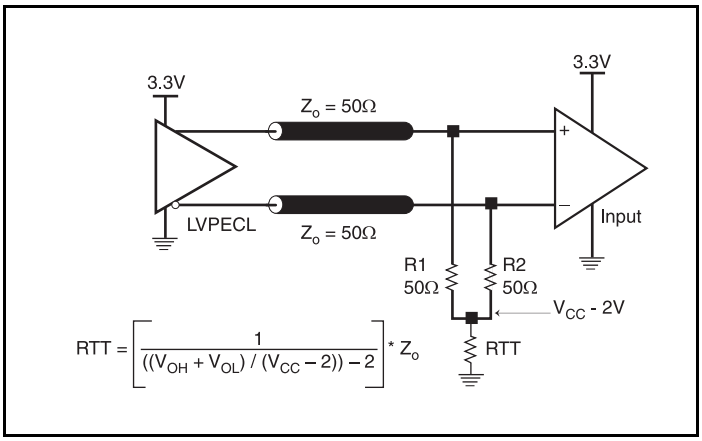


Figure 7A. 3.3V LVPECL Output Termination

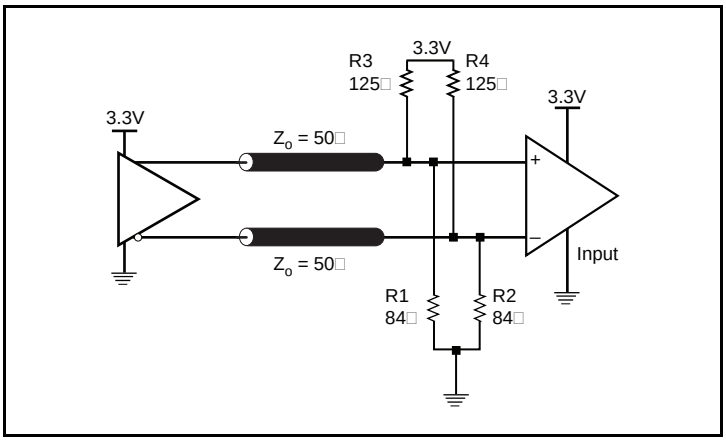


Figure 7B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 8A and *Figure 8B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 8B can be eliminated and the termination is shown in *Figure 8C.*

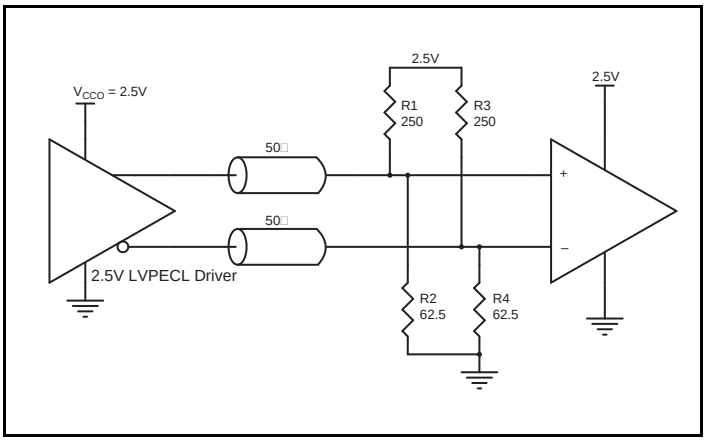


Figure 8A. 2.5V LVPECL Driver Termination Example

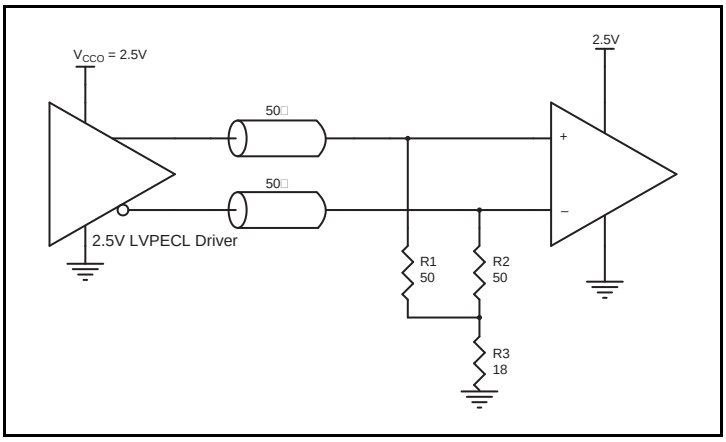


Figure 8B. 2.5V LVPECL Driver Termination Example

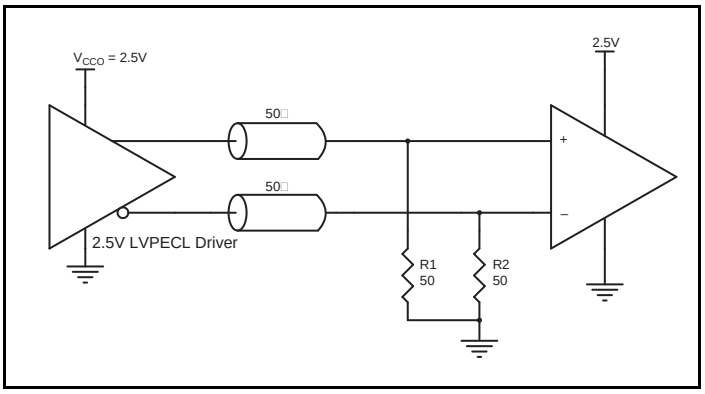


Figure 8C. 2.5V LVPECL Driver Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8T73S208B-01 Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8T73S208B-01 is the sum of the core power plus the power dissipated due to loading. The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

NOTE: Refer to Section, "3. Calculations and Equations." for details on calculating power dissipated due to loading.

I_{EE_MAX} at 85°C = 106.52mA

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 106.52mA = **369.09mW**
- Power $(outputs)_{MAX}$ = **36.3mW/Loaded Output pair**
  If all outputs are loaded, the total power is 8 * 36.3mW = **290.4mW**
- Power Dissipation for Internal Termination R_T with V_T floating
  Power $(R_T)_{Max} = (V_{IN\_MAX})^2 / R_{T\_MIN} = (1.2)^2 /80$ = 18mW

Total Power$_{MAX}$ = (3.465V, with all outputs switching) = 369.09mW + 290.4mW + 18mW = **677.49mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 42.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.678W * 42.7°C/W = 113.93°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32-Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 9.*

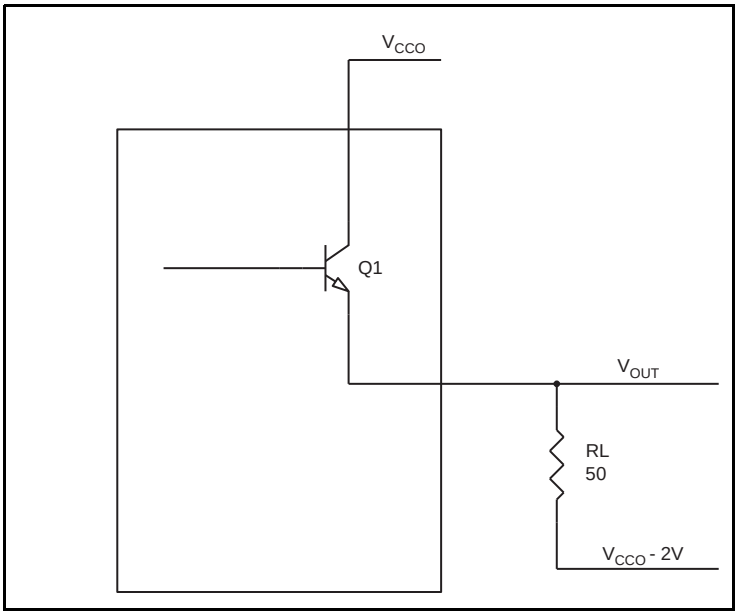


Figure 9. LVPECL Driver Circuit and Termination

To calculate power dissipation due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.775V}$
  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.775V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.367V}$
  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.367V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – 0.775V)/50Ω] * 0.775V =$ **18.99mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – 1.367V)/50Ω] * 1.367V =$ **17.31mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **36.3mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32-VFQFPN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

Transistor Count

The transistor count for 8T73S208B-01 is: 5153

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/us/en/document/psc/32-vfqfpn-package-outline-drawing-50-x-50-x-090-mm-body-epad-315-x-315-mm-nlg32p1

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T73S208B-01NLGI	IDT8T73S208B-01NLGI	5.0 × 5.0 × 0.90 mm, 32-VFQFPN	Tray	-40°C to 85°C
8T73S208B-01NLGI8	IDT8T73S208B-01NLGI	5.0 × 5.0 × 0.90 mm, 32-VFQFPN	Tape and Reel	-40°C to 85°C

Revision History

Date	Description
April 8, 2020	• Updated t_{JIT} parameters in AC Electrical Characteristics table. • Updated Typical Phase Jitter at 156.25MHz plot. • Updated Package Outline Drawings section. • Reformatted document.

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