

NB4N111K

Clock Fanout Buffer, 1:10 Differential, 3.3 V, with HCSL Level Output

Description

The NB4N111K is a differential input clock 1 to 10 HCSL fanout buffer, optimized for ultra low propagation delay variation. The NB4N111K is designed with HCSL clock distribution for FBDIMM applications in mind.

Inputs can accept differential ∇ PECL, CML, or ∇ DS levels. Single-ended ∇ PECL, CML, ∇ CMOS or ∇ TTL levels are accepted with the proper V_{REFAC} supply (see Figures 5, 10, 11, 12, and 13). Clock input pins incorporate an internal 50 Ω on die termination resistors. Outputs can interface with LVDS with proper termination (See Figure 15).

The NB4N111K specifically guarantees low output-to-output skews. Optimal design, layout, and processing minimize skew within a device and from device to device. System designers can take advantage of the NB4N111K's performance to distribute low skew clocks across the backplane or the motherboard.

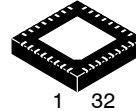
Features

- Typical Input Clock Frequencies: 100, 133, 166, 200, 266, 333, and 400 MHz
- 340 ps Typical Rise and Fall Times
- 800 ps Typical Propagation Delay
- Δt_{pd} 100 ps Maximum Propagation Delay Variation Per Each Differential Pair
- <1 ps RMS Additive Clock jitter
- Operating Range: $V_{CC} = 3.0\text{ V}$ to 3.6 V with $V_{EE} = 0\text{ V}$
- Differential HCSL Output Level or LVDS with Proper Termination
- These are Pb-Free Devices



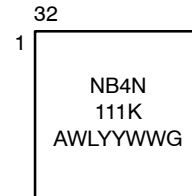
ON Semiconductor®

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QFN32
MN SUFFIX
CASE 488AM

MARKING DIAGRAM*



- A = Assembly Site
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

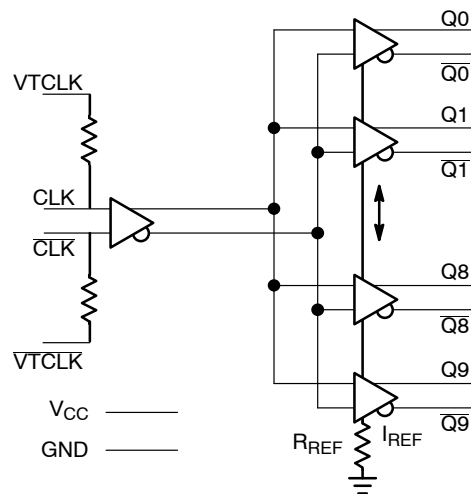


Figure 1. Pin Configuration (Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

NB4N111K

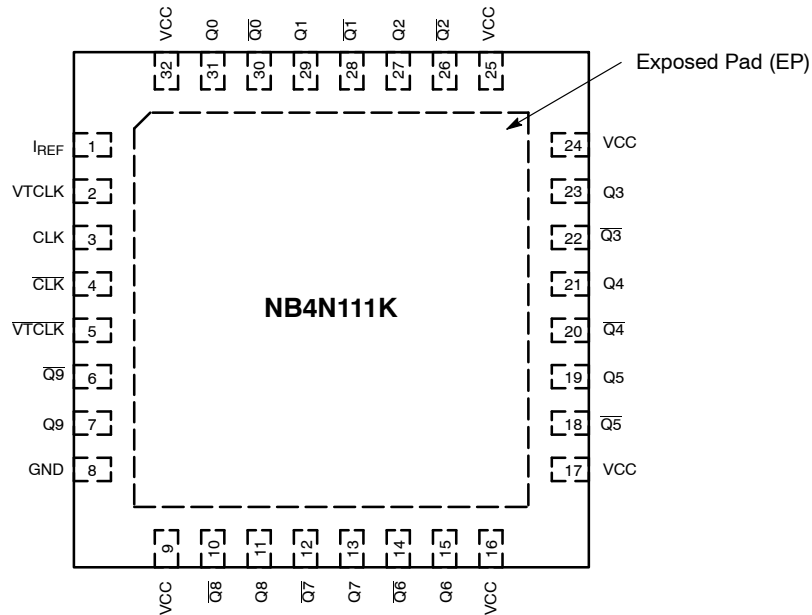


Figure 2. Pinout Configuration (Top View)

Table 1. PIN DESCRIPTION

| Pin | Name | I/O | Description |
|--|------------------|------------------------|--|
| 1 | I _{REF} | Output | Output current programming pin. Connect to GND. (See Figure 9). |
| 2, 5 | VTCLK, VTCLK | - | Internal 50 Ω Termination Resistor connection Pins. In the differential configuration when the input termination pins are connected to the common termination voltage, and if no signal is applied then the device may be susceptible to self-oscillation. |
| 3 | CLK | LVPECL Input | CLOCK Input (TRUE) |
| 4 | CLK | LVPECL Input | CLOCK Input (INVERT) |
| 8 | GND | - | Supply Ground. GND pin must be externally connected to power supply to guarantee proper operation. |
| 9, 16, 17, 24, 25, 32 | V _{CC} | - | Positive Supply pins. V _{CC} pins must be externally connected to a power supply to guarantee proper operation. |
| 6, 10, 12, 14, 18, 20, 22, 26, 28, 30 | Q[09-0] | HCSL or LVDS Output | Noninverted Clock Output. (For LVDS levels see Figure 15) |
| 7, 11, 13, 15, 19, 21, 23, 27, 29, 31 | Q[09-0] | HCSL or LVDS Output | Inverted Clock Output. (For LVDS levels see Figure 15) |
| Exposed Pad | EP | GND | Exposed Pad. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a sufficient heat-sinking conduit for proper thermal operation. (Note 1) |

1. The exposed pad must be connected to the circuit board ground.

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Table 2. ATTRIBUTES

| Characteristic | Value |
|--|----------------------|
| Input Default State Resistors | None |
| ESD Protection Human Body Model | >2 kV |
| Moisture Sensitivity (Note 2) QFN32 | Level 1 |
| Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | 622 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

2. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS (Note 3)

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|-------------------|---|--------------------|----------------|--|--------------|
| V _{CC} | Positive Power Supply | GND = 0 V | | 4.6 | V |
| V _I | Positive Input | GND = 0 V | | GND - 0.3 ≤ V _I ≤ V _{CC} | V |
| V _{INPP} | Differential Input Voltage CLK - $\overline{\text{CLK}}$ | | | V _{CC} | V |
| I _{OUT} | Output Current | Continuous Surge | | 50 100 | mA mA |
| T _A | Operating Temperature Range | QFN32 | | -40 to +70 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) (Note 3) | 0 lfpm 500 lfpm | QFN32 QFN32 | 31 27 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | 2S2P (Note 4) | QFN32 | 12 | °C/W |
| T _{sol} | Wave Solder Pb-Free | | | 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard 51-6, multilayer board - 2S2P (2 signal, 2 power).

4. JEDEC standard multilayer board - 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

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Table 4. DC CHARACTERISTICS ($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$ Note 5)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|-----------|---|------|------|-----|---------------|
| I_{GND} | GND Supply Current (All Outputs Loaded) | 70 | 98 | 120 | mA |
| I_{CC} | Power Supply Current (All Outputs Loaded) | | | 300 | mA |
| I_{IH} | Input HIGH Current CLKx, $\overline{\text{CLKx}}$ | | 2.0 | 150 | μA |
| I_{IL} | Input LOW Current CLKx, $\overline{\text{CLKx}}$ | -150 | -2.0 | | μA |

DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (Figures 5 and 7)

| | | | | | |
|----------|--|----------------|--|----------------|----|
| V_{th} | Input Threshold Reference Voltage Range (Note 6) | 1050 | | $V_{CC} - 150$ | mV |
| V_{IH} | Single-Ended Input HIGH Voltage | $V_{th} + 150$ | | V_{CC} | mV |
| V_{IL} | Single-Ended Input LOW Voltage | GND | | $V_{th} - 150$ | mV |

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 6 and 8)

| | | | | | |
|-----------|--|------|--|---------------|----|
| V_{IHD} | Differential Input HIGH Voltage | 1200 | | V_{CC} | mV |
| V_{ILD} | Differential Input LOW Voltage | GND | | $V_{CC} - 75$ | mV |
| V_{ID} | Differential Input Voltage ($V_{IHD} - V_{ILD}$) | 75 | | 2400 | mV |
| V_{CMR} | Input Common Mode Range | 1163 | | $V_{CC} - 75$ | |

HCSL OUTPUTS (Figure 4)

| | | | | | |
|----------|---------------------|------|-----|-----|----|
| V_{OH} | Output HIGH Voltage | 600 | 740 | 900 | mV |
| V_{OL} | Output LOW Voltage | -150 | 0 | 150 | mV |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input parameters vary 1:1 with V_{CC} . Measurements taken with all outputs loaded 50 Ω to GND, see Figure 9.
- V_{th} is applied to the complementary input when operating in single ended mode.

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Table 5. AC CHARACTERISTICS $V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$; $-40^{\circ}\text{C to }+70^{\circ}\text{C}$ (Note 7)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|--|---|-----|-----|------------------|----------------|
| V_{OUTPP} | Output Voltage Amplitude (@ $V_{INPPmin}$) $f_{in} = 400\text{ MHz}$ | | 725 | 1000 | mV |
| t_{PLH} , t_{PHL} | Propagation Delay to (See Figure 3) CLK/\overline{CLK} to Qx/\overline{Qx} | 550 | 800 | 1100 | ps |
| Δt_{PLH} , Δt_{PHL} | Propagation Delay Variations Variation Per Each Diff Pair CLK/\overline{CLK} to Qx/\overline{Qx} (Note 8) (See Figure 3) | | | 100 | ps |
| t_{SKEW} | Duty Cycle Skew (Note 9) Within-Device Skew Device-to-Device Skew (Note 10) | | | 20 100 150 | ps ps ps |
| t_{JITTER} | RMS Random Clock Jitter (Note 11) $f_{in} = 400\text{ MHz}$ | | | 1 | ps |
| V_{cross} | Absolute Crossing Magnitude Voltage | 250 | | 550 | mV |
| ΔV_{cross} | Variation in Magnitude of V_{cross} | | | 150 | mV |
| t_r , t_f | Absolute Magnitude in Output Risetime and Falltime (From 175 mV to 525 mV) Qx , \overline{Qx} | 175 | 340 | 700 | ps |
| Δt_r , Δt_f | Variation in Magnitude of Risetime and Falltime (Single-Ended) (See Figure 4) Qx , \overline{Qx} | | | 125 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Measured by forcing V_{INPP} (MIN) from a 50% duty cycle clock source. Measurements taken with all outputs loaded $50\ \Omega$ to GND, see Figure 9. Typical gain is 20 dB.
8. Measured from the input pair crosspoint to each single output pair crosspoint across temp and voltage ranges.
9. Duty cycle skew is measured between differential outputs using the deviations of the sum of $Tpw-$ and $Tpw+$.
10. Skew is measured between outputs under identical transition @ 400 MHz.
11. Additive RMS jitter with 50% duty cycle clock signal using phase noise integrated from 12 KHz to 33 MHz

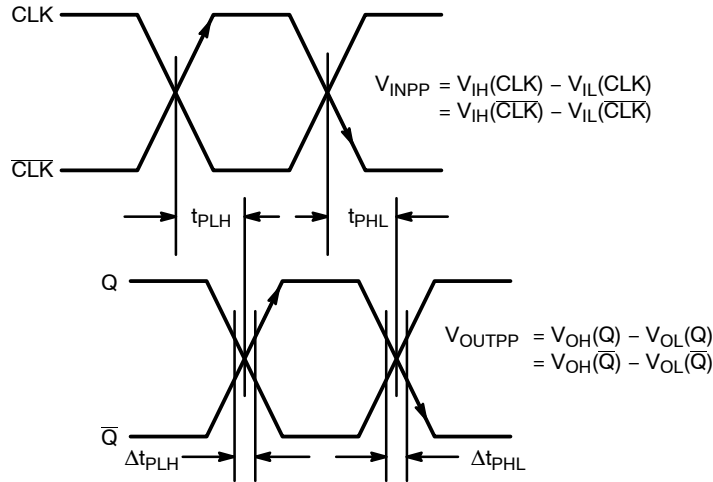


Figure 3. AC Reference Measurement

NB4N111K

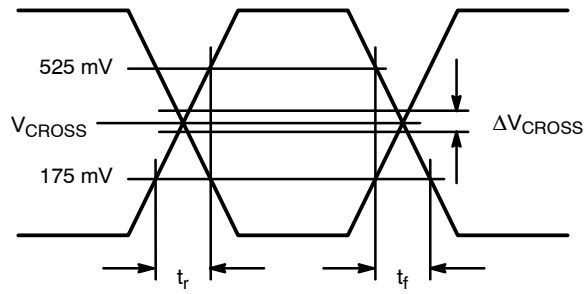


Figure 4. HCSL Output Parameter Characteristics

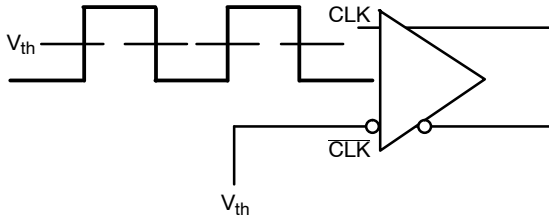


Figure 5. Differential Input Driven Single-Ended ($V_{th} = V_{REFAC}$)

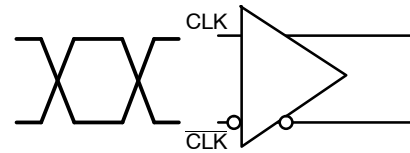


Figure 6. Differential Inputs Driven Differentially

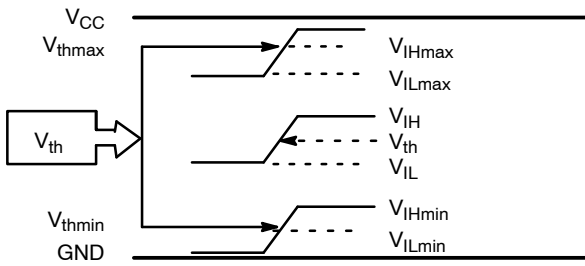


Figure 7. V_{th} Diagram

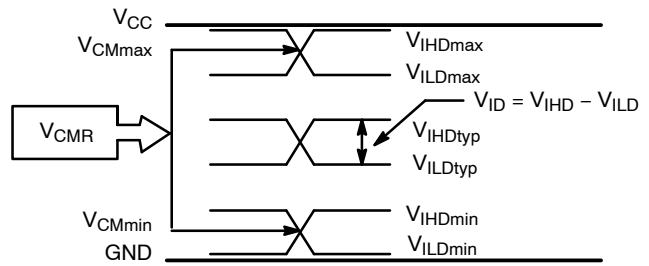
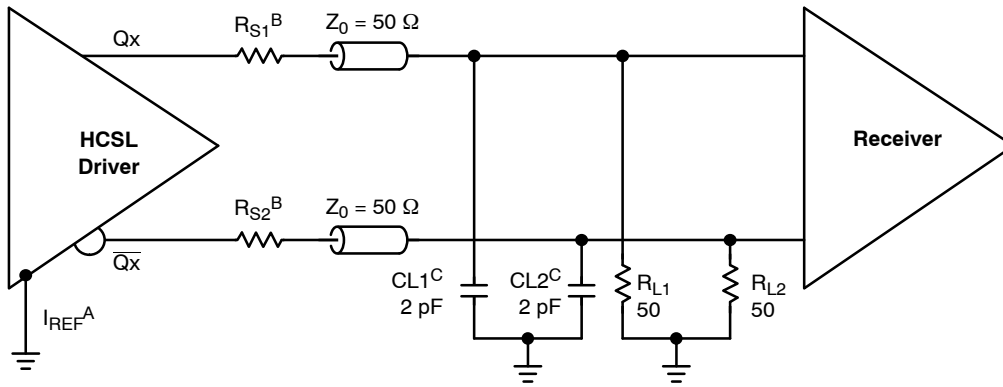


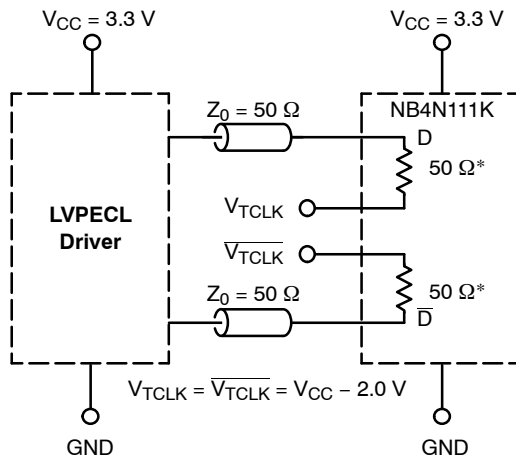
Figure 8. V_{CMR} Diagram

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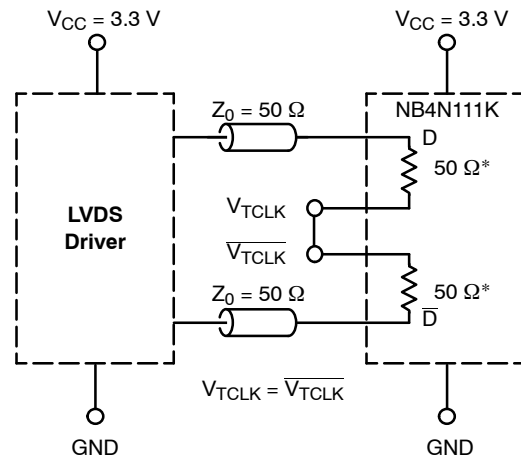
- A. Connect IREF pin to GND.
- B. RS1, RS2: 0 Ω for Test and Evaluation. Select to Minimizing Ringing.
- C. CL1, CL2: Receiver Input Simulation Load Capacitance Only.

Figure 9. Typical Termination Configuration for Output Driver and Device Evaluation C_{Lx} for Test Only (Representing Receiver Input Loading); Not Added to Application



*RTIN, Internal Input Termination Resistor

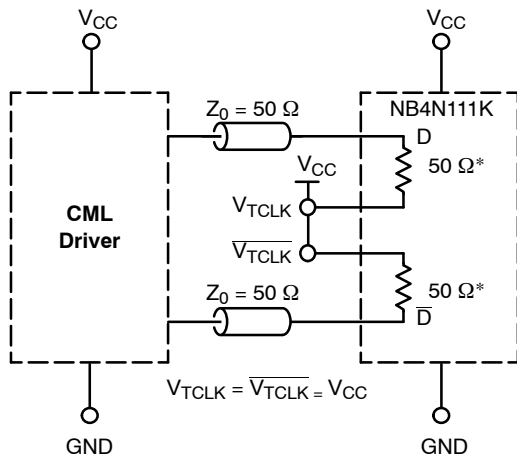
Figure 10. LVPECL Interface



*RTIN, Internal Input Termination Resistor

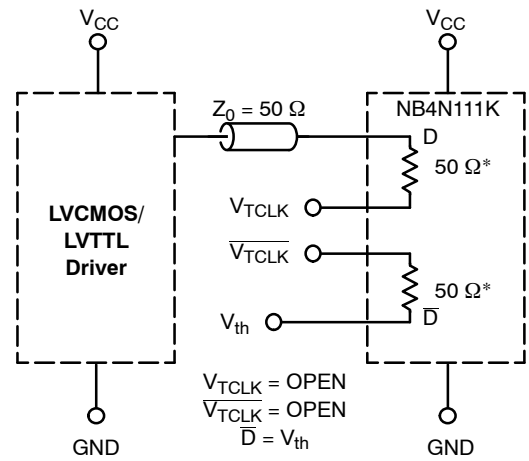
Figure 11. LVDS Interface

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*RTIN, Internal Input Termination Resistor

Figure 12. Standard 50 Ω Load CML Interface



*RTIN, Internal Input Termination Resistor

Figure 13. LVCMOS/LVTTL Interface

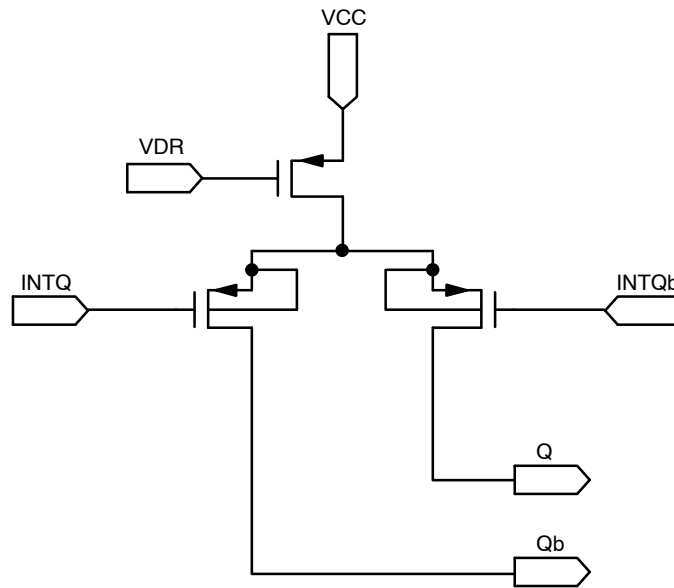


Figure 14. HCSL Output Structure

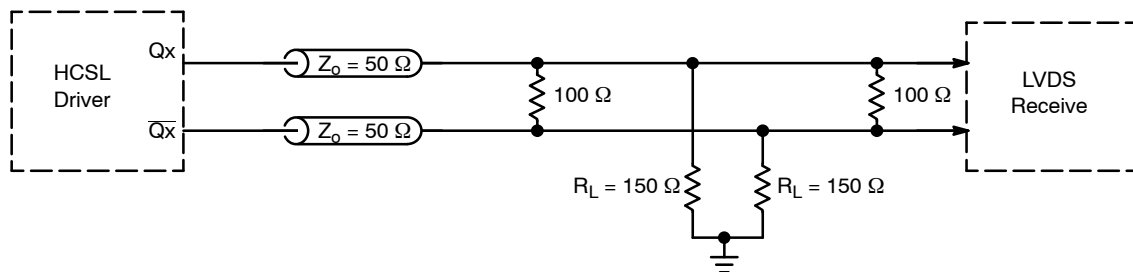


Figure 15. HCSL Interface Termination to LVDS

NB4N111K

ORDERING INFORMATION

| Device | Package | Shipping† |
|---------------|--------------------|--------------------|
| NB4N111KMNG | QFN32 (Pb-Free) | 79 Units / Rail |
| NB4N111KMNR4G | QFN32 (Pb-Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

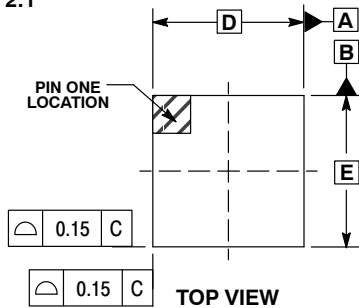


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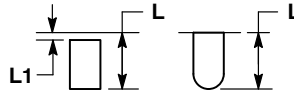
SCALE 2:1

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

DATE 23 OCT 2013



TOP VIEW

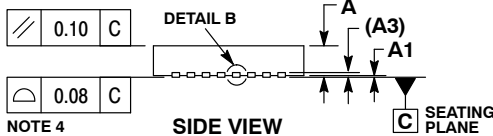


DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS

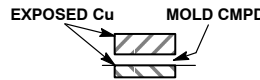
NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | |
|-------------|------|------|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | --- | 0.05 |
| A3 | 0.20 | REF |
| b | 0.18 | 0.30 |
| D | 5.00 | BSC |
| D2 | 2.95 | 3.25 |
| E | 5.00 | BSC |
| E2 | 2.95 | 3.25 |
| e | 0.50 | BSC |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |
| L1 | --- | 0.15 |

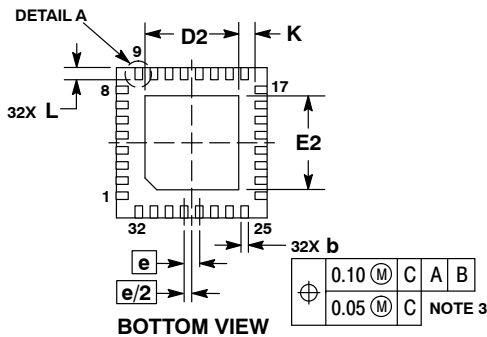


SIDE VIEW

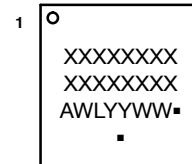


DETAIL B
ALTERNATE
CONSTRUCTION

GENERIC
MARKING DIAGRAM*



BOTTOM VIEW



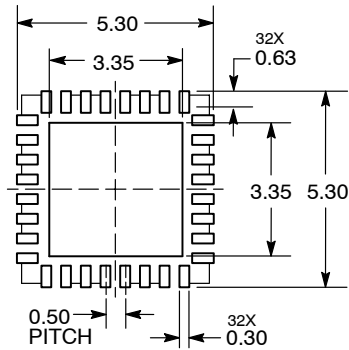
- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.

Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|------------------|----------------|--|
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| DESCRIPTION: | QFN32 5x5 0.5P | PAGE 1 OF 1 |

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