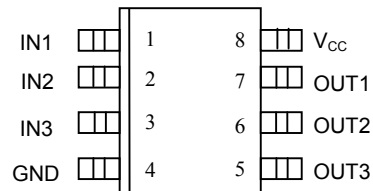


## FEATURES

- All-silicon timing circuit
- Three independent buffered delays
- Stable and precise over temperature and voltage
- Leading and trailing edge precision preserves the input symmetry
- Standard 8-pin SO (150mil), and 8-Pin  $\mu$ SOP (118mil)
- Vapor phase and IR reflow solderable
- Available in Tape and Reel
- Delays specified over both commercial and industrial temperature ranges
- 3V operation
- Recommended replacement for DS1033

## PIN ASSIGNMENT



DS1135LZ 8-Pin SO (150mil)  
 DS1135LU 8-Pin  $\mu$ SOP (118mil)  
 See Mech. Drawings Section

## PIN DESCRIPTION

|                 |                  |
|-----------------|------------------|
| IN1-IN3         | - Input Signals  |
| OUT1-OUT3       | - Output Signals |
| V <sub>CC</sub> | - +3V Supply     |
| GND             | - Ground         |

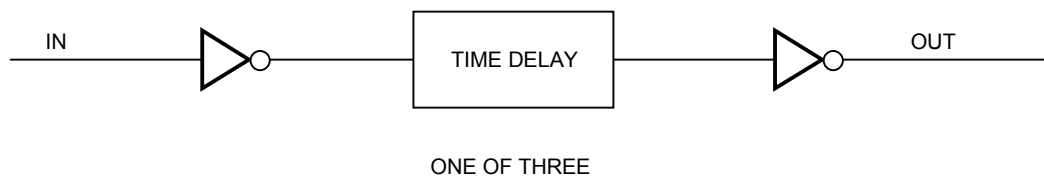
## DESCRIPTION

The DS1135L series is a low-power, 3V high-speed version of the popular DS1013, DS1033, DS1035 series.

The DS1135L series of delay lines have three independent logic buffered delays in a single package. The device is Dallas Semiconductor's fastest 3-in-1 delay line. It is available in a standard 8-pin 118mil  $\mu$ SOP and 150mil 8-pin Mini-SO.

The device features precise leading and trailing edge accuracy. It has the inherent reliability of an all-silicon delay line solution.

Standard delay values are indicated in Table 1. Customers may contact Dallas Semiconductor at (972) 371-4348 for further information on custom delay values.

**LOGIC DIAGRAM** Figure 1**PART NUMBER DELAY TABLE ( $t_{PLH}$ ,  $t_{PHL}$ )** Table 1

| PART NUMBER | DELAY PER OUTPUT (ns) | INITIAL TOLERANCE (Note 1) | TOLERANCE OVER TEMP AND VOLTAGE (Note 2) |                |
|-------------|-----------------------|----------------------------|--|----------------|
|             |                       |                            | 0°C to +70°C                             | -40°C to +85°C |
| DS1135LX-10 | 10/10/10              | ±1.0ns                     | ±2.0ns                                   | ±3.0ns         |
| DS1135LX-12 | 12/12/12              | ±1.0ns                     | ±2.0ns                                   | ±3.0ns         |
| DS1135LX-15 | 15/15/15              | ±1.0ns                     | ±2.5ns                                   | ±4.0ns         |
| DS1135LX-20 | 20/20/20              | ±1.0ns                     | ±2.5ns                                   | ±4.0ns         |
| DS1135LX-25 | 25/25/25              | ±1.5ns                     | ±3.0ns                                   | ±5.0ns         |
| DS1135LX-30 | 30/30/30              | ±1.5ns                     | ±3.0ns                                   | ±5.0ns         |

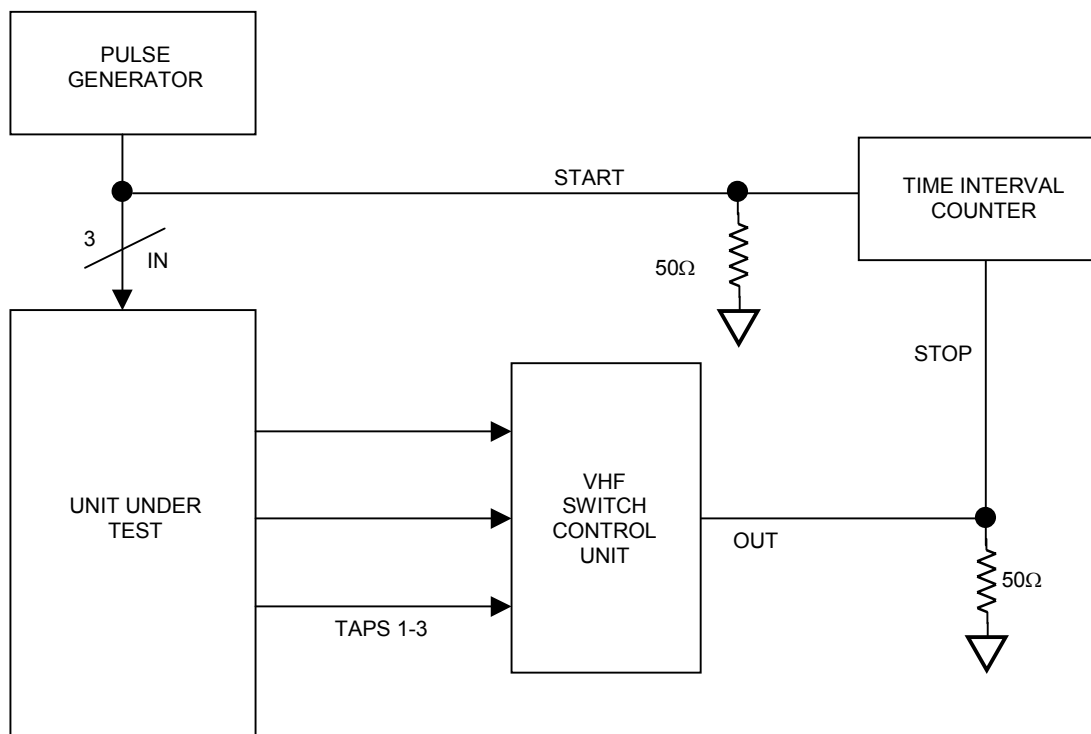
**NOTES:**

1. Nominal conditions are +25°C and  $V_{CC} = +3.3V$ .
2. Voltage range of 2.7V to 3.6V.
3. Delay accuracies is for both leading and trailing edges.
4. X in Part number denotes package: U indicates  $\mu$ SOP, Z indicates SO.

**TEST SETUP DESCRIPTION**

Figure 2 illustrates the hardware configuration used for measuring the timing parameters of the DS1135L. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1135L output taps are selected and connected to the interval counter by a VHF switch control unit. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

## DS1135L TEST CIRCUIT Figure 2



**ABSOLUTE MAXIMUM RATINGS\***

|                                       |                              |
|---------------------------------------|------------------------------|
| Voltage on Any Pin Relative to Ground | -1.0V to +6.0 V              |
| Operating Temperature                 | -40°C to +85°C               |
| Storage Temperature                   | -55°C to +125°C              |
| Soldering Temperature                 | See J-STD-020A specification |
| Short Circuit Output Current          | 50mA for 1 second            |

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**DC ELECTRICAL CHARACTERISTICS** (-40°C to +85°C;  $V_{CC}=2.7-3.6V$ )

| PARAMETER                 | SYMBOL   | TEST CONDITION                    | MIN  | TYP | MAX          | UNITS   |
|---------------------------|----------|-----------------------------------|------|-----|--------------|---------|
| Supply Voltage            | $V_{CC}$ |                                   | 2.7  | 3.3 | 3.6          | V       |
| Active Current            | $I_{CC}$ | $V_{CC}=3.6V$<br>Period=1 $\mu$ s |      |     | 10           | mA      |
| High Level Input Voltage  | $V_{IH}$ |                                   | 2.0  |     | $V_{CC}+0.5$ | V       |
| Low Level Input Voltage   | $V_{IL}$ |                                   | -0.5 |     | 0.8          | V       |
| Input Leakage             | $I_L$    | $0V \leq V_I \leq V_{CC}$         | -1.0 |     | +1.0         | $\mu$ A |
| High Level Output Current | $I_{CC}$ | $V_{CC}=2.7V$<br>$V_{OH}=2V$      |      |     | -1.0         | mA      |
| Low Level Output Current  | $I_{CC}$ | $V_{CC}=2.7V$<br>$V_{OL}=0.4V$    | 8    |     |              | mA      |

**AC ELECTRICAL CHARACTERISTICS** (-40°C to +85°C;  $V_{CC}=2.7-3.6V$ )

| PARAMETER                | SYMBOL             | MIN                 | TYP | MAX | UNITS | NOTES |
|--------------------------|--------------------|---------------------|-----|-----|-------|-------|
| Period                   | $t_{PERIOD}$       | 2 ( $t_{WI}$ )      |     |     | ns    |       |
| Input Pulse Width        | $t_{WI}$           | 100% of Delay Value |     |     | ns    |       |
| Input-to-Output Delay    | $t_{PLH}, t_{PHL}$ | See Table 1         |     |     | ns    |       |
| Output Rise or Fall Time | $t_{OF}, t_{OR}$   |                     | 2.0 | 2.5 | ns    |       |
| Power-up Time            | $t_{PU}$           |                     |     | 1   | ms    | 2     |

**CAPACITANCE** ( $T_A=25^\circ C$ )

| PARAMETER         | SYMBOL   | MIN | TYP | MAX | UNITS | NOTES |
|-------------------|----------|-----|-----|-----|-------|-------|
| Input Capacitance | $C_{IN}$ |     |     | 10  | pF    |       |

## TEST CONDITIONS

Ambient Temperature:  $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$

Supply Voltage ( $V_{\text{CC}}$ ):  $3.3\text{V} \pm 0.1\text{V}$

Input Pulse:

High:  $3.0\text{V} \pm 0.1\text{V}$

Low:  $0.0\text{V} \pm 0.1\text{V}$

Source Impedance:  $50\Omega$  Max.

Rise and Fall Time:  $3.0\text{ns}$  Max. — Measured between  $0.6\text{V}$  and  $2.4\text{V}$ .

Pulse Width:  $500\text{ns}$

Pulse Period:  $1\mu\text{s}$

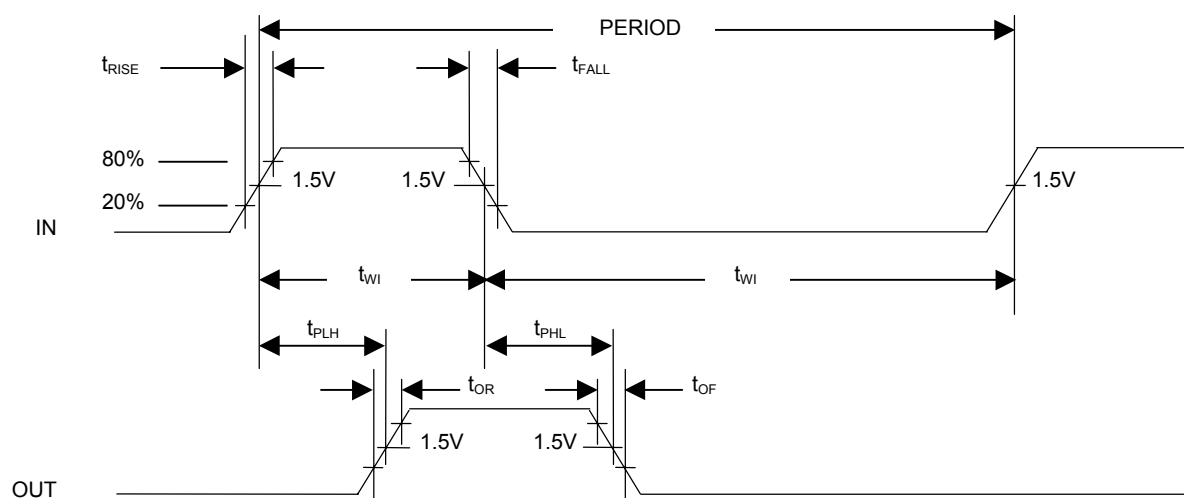
Output Load Capacitance:  $15\text{pF}$

Output: Each output is loaded with the equivalent of one 74F04 input gate.

Data is measured at the  $1.5\text{V}$  level on the rising and falling edges.

**Note:** The above conditions are for test only and do not restrict the devices under other data sheet conditions.

## TIMING DIAGRAM



## NOTES:

1. All voltages are referenced to ground.
2. Power-up time is the time from the application of power to the time stable delays are being produced at the output.

## TERMINOLOGY

**Period:** The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

**$t_{WI}$  (Pulse Width):** The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

**$t_{RISE}$  (Input Rise Time):** The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

**$t_{FALL}$  (Input Fall Time):** The elapsed time between the 80% and the 20% point on the trailing edge on the input pulse.

**$t_{PLH}$  (Time Delay, Rising):** The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the output pulse.

**$t_{PHL}$  (Time Delay, Falling):** The elapsed time between the 1.5V point on the falling edge of the input pulse and the 1.5V point on the falling edge of the output pulse.

## ORDERING INFORMATION

