

## FEATURES

### HIGHLIGHTS

- Single PLL chip:
  - Features 0.5 mHz to 560 Hz bandwidth
  - Provides node clock for ITU-T G.8261/G.8262 Synchronous Ethernet (SyncE)
  - Exceeds GR-253-CORE (OC-192) and ITU-T G.813 (STM-64) jitter generation requirements
  - Provides node clocks for Cellular and WLL base-station (GSM and 3G networks)
  - Provides clocks for DSL access concentrators (DSLAM), especially for Japan TCM-ISDN network timing based ADSL equipments
  - Provides clocks for 1 Gigabit and 10 Gigabit Ethernet application
  - It supports clock generation for IEEE-1588 applications

### MAIN FEATURES

- Provides an integrated single-chip solution for Synchronous Equipment Timing Source, including Stratum 3, 4E, 4, SMC, EEC-Option 1 and EEC-Option 2 Clocks
- Provides SONET clocks with less than 1.5 ps of RMS Phase Jitter (12 KHz - 20 MHz)
- Supports 1 pps input and output
- Employs PLL architecture to feature excellent jitter performance and minimize the number of the external components
- Supports programmable DPLL bandwidth from 0.5 mHz to 560 Hz
- Supports  $1.1 \times 10^{-5}$  ppm absolute holdover accuracy and  $4.4 \times 10^{-8}$  ppm instantaneous holdover accuracy
- Supports hitless reference switching to minimize phase transients on the DPLL output to be no more than 0.61 ns
- Supports programmable input-to-output phase offset adjustment
- Limits the phase and frequency offset of the outputs
- Provides OUT1~OUT6 output clocks whose frequencies cover from 1 Hz (1PPS) to 644.53125 MHz
  - 1PPS, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1, N x T1, N x 13.0 MHz, N x 3.84 MHz, 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 25MHz, 25.78125 MHz, 125 MHz, 128.90625 MHz, 155.52 MHz or 156.25 MHz or 161.1328125 MHz for CMOS outputs
  - 1PPS, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1, N x T1, N x 13.0 MHz, N x 3.84 MHz, 5 MHz, 10 MHz, 20 MHz, 25 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125 MHz, 128.90625 MHz, 155.52 MHz, 156.25 MHz, 161.1328125 MHz, 311.04 MHz, 312.5 MHz, 322.265625 MHz, 622.08 MHz, 625 MHz or 644.53125 MHz for differential Outputs

- Provides IN1~IN6 input clocks whose frequencies cover from 1 Hz (1PPS) to 625 MHz
  - 1PPS, 2 kHz, 4 kHz, N x 8 kHz, 1.544 MHz, 2.048 MHz, 6.25 MHz, 6.48MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125MHz, 155.52 MHz or 156.25 MHz for CMOS inputs
  - 1PPS, 2 kHz, 4 kHz, N x 8 kHz, 1.544 MHz, 2.048 MHz, 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125MHz, 155.52 MHz, 156.25 MHz, 311.04 MHz, 312.5 MHz, 622.08 MHz or 625 MHz for differential inputs
- Internal DCO can be controlled by an external processor to be used for IEEE-1588 clock generation
- Supports Forced or Automatic operating mode switch controlled by an internal state machine. It supports Free- Run, Locked and Hold-over modes
- Supports manual and automatic selected input clock switch
- Supports automatic hitless selected input clock switch on clock failure
- Provides a 2 kHz, 4 kHz, 8 kHz, or 1PPS frame sync input signal, and a 2 kHz, 8 kHz, or 1PPS frame sync output signals
- Provides output clocks for BITS, GPS, 3G, GSM, etc.
- Supports PECL/LVDS and CMOS input/output technologies
- Supports master clock calibration
- Supports Master/Slave application (two chips used together) to enable system protection against single chip failure
- Supports Telcordia GR-1244-CORE, Telcordia GR-253-CORE, ITU-T G.812, ITU-T G.8262, ITU-T G.813 and ITU-T G.783 Recommendations

### OTHER FEATURES

- I2C and Serial microprocessor interface modes
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation with 5 V tolerant CMOS I/Os
- 72-pin QFN package, Green package options available

### APPLICATIONS

- 1 Gigabit Ethernet and 10 Gigabit Ethernet
- BITS / SSU
- SMC / SEC (SONET / SDH)
- DWDM cross-connect and transmission equipments
- Synchronous Ethernet equipments
- Central Office Timing Source and Distribution
- Core and access IP switches / routers
- Gigabit and Terabit IP switches / routers
- IP and ATM core switches and access equipments
- Cellular and WLL base-station node clocks
- Broadband and multi-service access equipments

## DESCRIPTION

The IDT82V3398 is an integrated, single-chip solution for the Synchronous Equipment Timing Source for Stratum 3, 4E, 4, SMC, EEC-Option1, EEC-Option2 clocks in SONET / SDH / Synchronous Ethernet equipment, DWDM and Wireless base station.

The device consists of a highly quality and configurable DPLL to provide system clock for node timing synchronization within a SONET / SDH / Synchronous Ethernet network.

An input clock is automatically or manually selected for the DPLL. The DPLL has three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode, the DPLL refers to the master clock. In Locked mode, the DPLL locks to the selected input clock. In Holdover mode, the DPLL resorts to the frequency data acquired in Locked mode. Whatever the operating mode is, the DPLL gives a stable performance without being affected by operating conditions or silicon process variations.

There is also a high performance APLL that is used for low jitter SONET and Ethernet Clocks

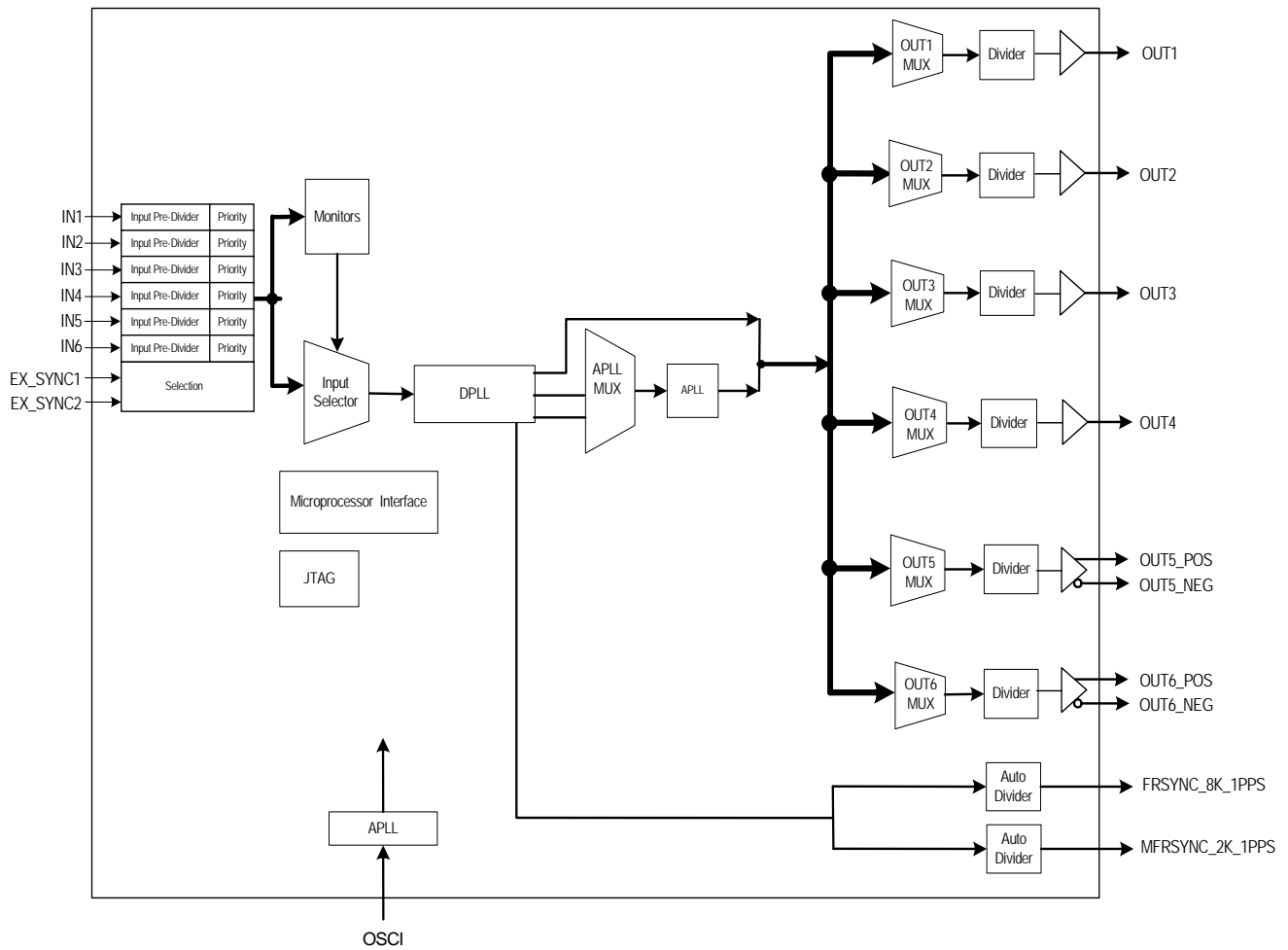
The device provides programmable DPLL bandwidths: 0.5 mHz to 560 Hz. Different settings cover all SONET / SDH clock synchronization requirements.

A highly stable input is required for the master clock in different applications. The master clock is used as a reference clock for all the internal circuits in the device. It can be calibrated within  $\pm 741$  ppm.

All the read/write registers are accessed through a microprocessor interface. The device supports I2C and serial microprocessor interface modes.

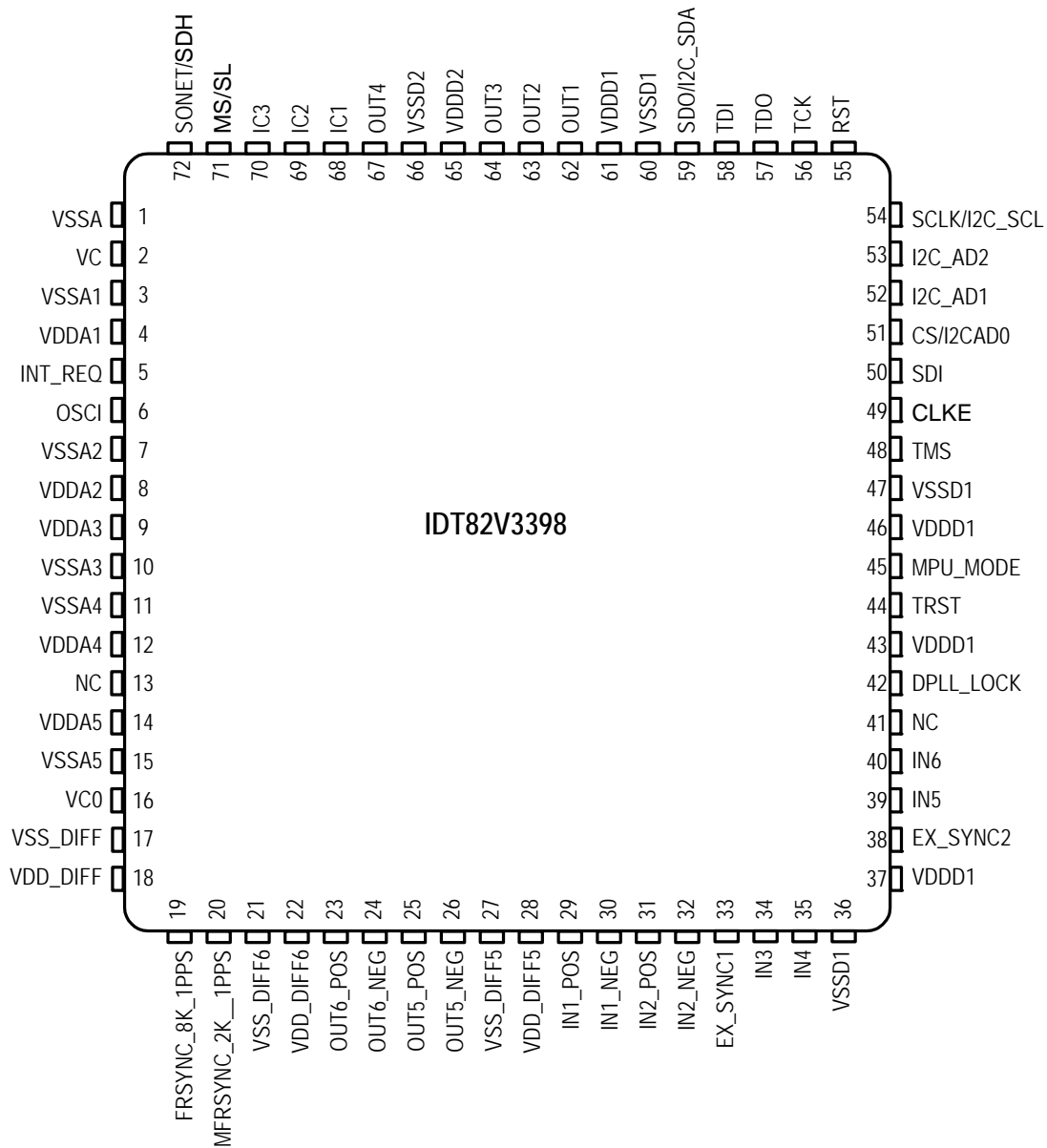
In general, the device can be used in Master/Slave application. In this application, two devices should be used together to enable system protection against single chip failure.

# FUNCTIONAL BLOCK DIAGRAM



**Figure 1. Functional Block Diagram**

# 1 PIN ASSIGNMENT



**Figure 2. Pin Assignment (Top View)**

## 2 PIN DESCRIPTION

Table 1: Pin Description

| Name                                      | Pin No.  | I/O            | Type      | Description <sup>1,2</sup>   |
|---|----------|----------------|-----------|--|
| <b>Global Control Signal</b>              |          |                |           |  |
| OSCI                                      | 6        | I              | CMOS      | <b>OSCI: Crystal Oscillator Master Clock</b><br>A nominal 12.8000 MHz clock provided by a crystal oscillator is input on this pin. It is the master clock for the device.  |
| MS/SL                                     | 71       | I<br>pull-up   | CMOS      | <b>MS/SL: Master / Slave Selection</b><br>This pin, together with the MS_SL_CTRL bit (b0, 13H), controls whether the device is configured as the Master or as the Slave. Refer to <a href="#">Chapter 3.14 Master / Slave Configuration</a> for details.<br>The signal level on this pin is reflected by the MASTER_SLAVE bit (b1, 09H).   |
| SONET/SDH                                 | 72       | I<br>pull-down | CMOS      | <b>SONET/SDH: SONET / SDH Frequency Selection</b><br>During reset, this pin determines the default value of the IN_SONET_SDH bit (b2, 09H):<br>High: The default value of the IN_SONET_SDH bit is '1' (SONET);<br>Low: The default value of the IN_SONET_SDH bit is '0' (SDH).<br>After reset, the value on this pin takes no effect.  |
| RST                                       | 55       | I<br>pull-up   | CMOS      | <b>RST: Reset</b><br>A low pulse of at least 50 $\mu$ s on this pin resets the device. After this pin is high, the device will still be held in reset state for 500 ms (typical).  |
| <b>Frame Synchronization Input Signal</b> |          |                |           |  |
| EX_SYNC1                                  | 33       | I<br>pull-down | CMOS      | <b>EX_SYNC1: External Sync Input 1</b><br>A 2 kHz, 4 kHz, 8 kHz, or 1PPS signal is input on this pin.  |
| EX_SYNC2                                  | 38       | I<br>pull-down | CMOS      | <b>EX_SYNC2: External Sync Input 1</b><br>A 2 kHz, 4 kHz, 8 kHz, or 1PPS signal is input on this pin.  |
| <b>Input Clock</b>                        |          |                |           |  |
| IN1_POS<br>IN1_NEG                        | 29<br>30 | I              | PECL/LVDS | <b>IN1_POS / IN1_NEG: Positive / Negative Input Clock 1</b><br>A 1PPS, 2 kHz, 4 kHz, N x 8 kHz <sup>3</sup> , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 156.25 MHz, 311.04 MHz, 312.5 MHz, 622.08 MHz or 625 MHz clock is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected.<br>Single-ended input for differential input is also supported. Refer to <a href="#">Chapter 9.3.2.3 Single-Ended Input for Differential Input</a> .  |
| IN2_POS<br>IN2_NEG                        | 31<br>32 | I              | PECL/LVDS | <b>IN2_POS / IN2_NEG: Positive / Negative Input Clock 2</b><br>A 1PPS, 2 kHz, 4 kHz, N x 8 kHz <sup>3</sup> , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 156.25 MHz, 311.04 MHz or 312.5 MHz, 622.08 MHz or 625 MHz clock is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected.<br>Single-ended input for differential input is also supported. Refer to <a href="#">Chapter 9.3.2.3 Single-Ended Input for Differential Input</a> . |
| IN3                                       | 34       | I<br>pull-down | CMOS      | <b>IN3: Input Clock 3</b><br>A 1PPS, 2 kHz, 4 kHz, N x 8 kHz <sup>3</sup> , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.   |
| IN4                                       | 35       | I<br>pull-down | CMOS      | <b>IN4: Input Clock 4</b><br>A 1PPS, 2 kHz, 4 kHz, N x 8 kHz <sup>3</sup> , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.   |

Table 1: Pin Description (Continued)

| Name                                       | Pin No. | I/O            | Type      | Description <sup>1,2</sup>   |
|--|---------|----------------|-----------|--|
| IN5  | 39      | I<br>pull-down | CMOS      | <b>IN5: Input Clock 5</b><br>A 1PPS, 2 kHz, 4 kHz, N x 8 kHz <sup>3</sup> , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.   |
| IN6  | 40      | I<br>pull-down | CMOS      | <b>IN6: Input Clock 6</b><br>A 1PPS, 2 kHz, 4 kHz, N x 8 kHz <sup>3</sup> , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.   |
| <b>Output Frame Synchronization Signal</b> |         |                |           |  |
| FRSYNC_8K_1PPS                             | 19      | O              | CMOS      | <b>FRSYNC_8K_1PPS: 8 kHz Frame Sync Output</b><br>An 8 kHz signal or a 1PPS sync signal is output on this pin.   |
| MFRSYNC_2K_1PPS                            | 20      | O              | CMOS      | <b>MFRSYNC_2K_1PPS: 2 kHz Multiframe Sync Output</b><br>A 2 kHz signal or a 1PPS sync signal is output on this pin.  |
| <b>Output Clock</b>                        |         |                |           |  |
| OUT1                                       | 62      | O              | CMOS      | <b>OUT1 ~ OUT4: Output Clock 1 ~ 4</b><br>A 1PPS, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 <sup>4</sup> , N x T1 <sup>5</sup> , N x 13.0 MHz <sup>6</sup> , N x 3.84 MHz <sup>7</sup> , 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 25MHz, 25.78125 MHz, 125 MHz, 128.90625 MHz, 155.52 MHz or 156.25 MHz or 161.1328125 MHz clock is output on these pins.  |
| OUT2                                       | 63      |                |           |  |
| OUT3                                       | 64      |                |           |  |
| OUT4                                       | 67      |                |           |  |
| OUT5_POS                                   | 25      | O              | PECL/LVDS | <b>OUT5_POS / OUT5_NEG: Positive / Negative Output Clock 5</b><br>A 1PPS, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 <sup>4</sup> , N x T1 <sup>5</sup> , N x 13.0 MHz <sup>6</sup> , N x 3.84 MHz <sup>7</sup> , 5 MHz, 10 MHz, 20 MHz, 25 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125 MHz, 128.90625 MHz, 155.52 MHz, 156.25 MHz, 161.1328125 MHz, 311.04 MHz, 312.5 MHz, 322.265625 MHz, 622.08 MHz, 625 MHz or 644.53125 MHz clock is differentially output on these pair of pins. |
| OUT5_NEG                                   | 26      |                |           |  |
| OUT6_POS                                   | 23      | O              | PECL/LVDS | <b>OUT6_POS / OUT6_NEG: Positive / Negative Output Clock 6</b><br>A 1PPS, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 <sup>4</sup> , N x T1 <sup>5</sup> , N x 13.0 MHz <sup>6</sup> , N x 3.84 MHz <sup>7</sup> , 5 MHz, 10 MHz, 20 MHz, 25 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125 MHz, 128.90625 MHz, 155.52 MHz, 156.25 MHz, 161.1328125 MHz, 311.04 MHz, 312.5 MHz, 322.265625 MHz, 622.08 MHz, 625 MHz or 644.53125MHz clock is differentially output on these pair of pins.  |
| OUT6_NEG                                   | 24      |                |           |  |
| VC   | 2       | O              | Analog    | <b>VC:</b> This pin must be connected to ground.   |
| VC0  | 16      | O              | Analog    | <b>VC0: APLL VC Output</b><br>External RC filter<br>See "APLL" on page 35 for details.   |
| <b>Lock Signal</b>                         |         |                |           |  |
| DPLL_LOCK                                  | 42      | O              | CMOS      | <b>DPLL_LOCK</b><br>This pin goes high when DPLL is locked   |
| <b>Microprocessor Interface</b>            |         |                |           |  |
| CS / I2C_AD0                               | 51      | I/O<br>pull-up | CMOS      | <b>CS: Chip Selection</b><br>In Serial mode, this pin is an input. A transition from high to low must occur on this pin for each read or write operation and this pin should remain low until the operation is over.<br><b>I2C_AD0: Device Address Bit 0</b><br>In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.   |
| INT_REQ                                    | 5       | O              | CMOS      | <b>INT_REQ: Interrupt Request</b><br>This pin is used as an interrupt request. The output characteristics are determined by the HZ_EN bit (b1, 0CH) and the INT_POL bit (b0, 0CH).   |

Table 1: Pin Description (Continued)

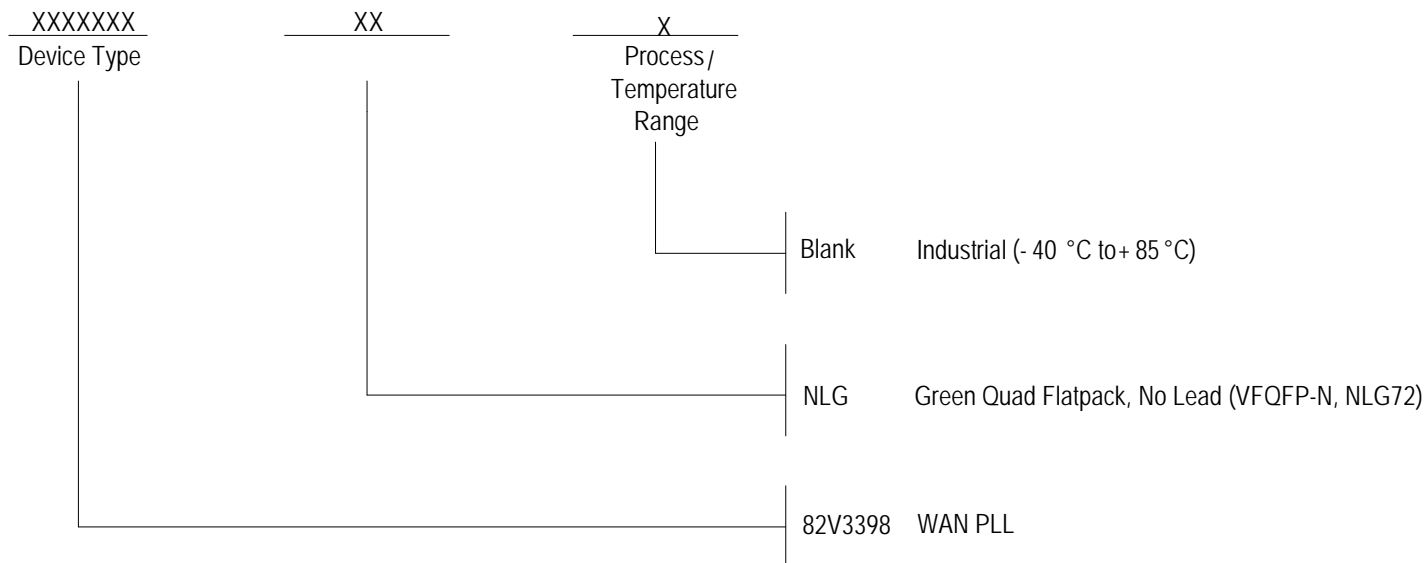
| Name                          | Pin No. | I/O              | Type | Description <sup>1,2</sup>  |
|-------------------------------|---------|------------------|------|---|
| MPU_MODE                      | 45      | I<br>pull-down   | CMOS | <b>MPU_MODE: Microprocessor Interface Mode Selection</b><br>The device supports 2 microprocessor interface modes: I2C and Serial.<br>During reset, these pins determine the default value of the MPU_SEL_CNFG[0] bit(b0, 7FH) as follows:<br>0: I2C mode<br>1: Serial mode<br>After reset, these pins are general purpose inputs. The microprocessor interface mode is selected by the MPU_SEL_CNFG[0] bits (b0, 7FH).<br>After reset de-assertion, wait 10 $\mu$ s for the mode to be active.<br>The value of this pin is always reflected by the MPU_PIN_STS[0] bits (b0, 02H). |
| CLKE                          | 49      | I/O<br>pull-down | CMOS | <b>CLKE: SCLK Active Edge Selection</b><br>In Serial mode, this pin is an input, it selects the active edge of SCLK to update the SDO:<br>High - The falling edge;<br>Low - The rising edge.<br><br>See <a href="#">Table 28</a> for details.   |
| SDI                           | 50      | I/O<br>pull-down | CMOS | <b>SDI: Serial Data Input</b><br>In Serial mode, this pin is used as the serial data input. Address and data on this pin are serially clocked into the device on the rising edge of SCLK.<br><br>See <a href="#">Table 28</a> for details.  |
| SDO / I2C_SDA                 | 59      | I/O<br>pull-down | CMOS | <b>SDO: Serial Data Output</b><br>In Serial mode, this pin is used as the serial data output. Data on this pin is serially clocked out of the device on the active edge of SCLK.<br><br><b>I2C_SDA: Serial Data Input/Output</b><br>In I2C mode, this pin is used as the input/output for the serial data.  |
| I2C_AD1                       | 52      | I<br>pull-up     | CMOS | <b>I2C_AD1: Device Address Bit 1</b><br>In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.<br>In Serial mode, this pin should be connected to ground.   |
| I2C_AD2                       | 53      | I<br>pull-up     | CMOS | <b>I2C_AD2: Device Address Bit 2</b><br>In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.<br>In Serial mode, this pin should be connected to ground.   |
| SCLK / I2C_SCL                | 54      | I<br>pull-down   | CMOS | <b>SCLK: Shift Clock</b><br>In Serial mode, a shift clock is input on this pin.<br>Data on SDI is sampled by the device on the rising edge of SCLK. Data on SDO is updated on the active edge of SCLK. The active edge is determined by the CLKE.<br><br><b>I2C_SCL: Serial Clock Line</b><br>In I2C mode, the serial clock is input on this pin.   |
| <b>JTAG (per IEEE 1149.1)</b> |         |                  |      |   |
| TRST                          | 44      | I<br>pull-down   | CMOS | <b>TRST: JTAG Test Reset (Active Low)</b><br>A low signal on this pin resets the JTAG test port.<br>This pin should be connected to ground when JTAG is not used.   |
| TMS                           | 48      | I<br>pull-up     | CMOS | <b>TMS: JTAG Test Mode Select</b><br>The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.  |
| TCK                           | 56      | I<br>pull-down   | CMOS | <b>TCK: JTAG Test Clock</b><br>The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK.<br>If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.  |

Table 1: Pin Description (Continued)

| Name   | Pin No.       | I/O          | Type | Description <sup>1, 2</sup>  |
|--|---------------|--------------|------|--|
| TDI  | 58            | I<br>pull-up | CMOS | <b>TDI: JTAG Test Data Input</b><br>The test data are input on this pin. They are clocked into the device on the rising edge of TCK.   |
| TDO  | 57            | O            | CMOS | <b>TDO: JTAG Test Data Output</b><br>The test data are output on this pin. They are clocked out of the device on the falling edge of TCK.<br>TDO pin outputs a high impedance signal except during the process of data scanning. This pin can indicate the interrupt of DPLL selected input clock fail, as determined by the LOS_FLAG_ON_TDO bit (b6, 0BH). Refer to <a href="#">Chapter 3.8.1 Input Clock Validity</a> for details. |
| <b>Power &amp; Ground</b>  |               |              |      |  |
| VDDD1  | 37,43, 46, 61 | Power        | -    | <b>VDDD1: Digital Core Power.</b>  |
| VDDD2  | 65            | Power        | -    | <b>VDDD2: CMOS CLK Output Power</b>  |
| VDD_DIFF   | 18            | Power        | -    | <b>VDD_DIFF: Differential I/O Power Supply</b>   |
| VDD_DIFF6  | 22            | Power        | -    | <b>VDD_DIFF6: Differential I/O Power Supply</b>  |
| VDD_DIFF5  | 28            | Power        | -    | <b>VDD_DIFF5: Differential I/O Power Supply</b>  |
| VSSD1  | 36, 47, 60    | Ground       | -    | <b>VSSD1: Digital Core Ground</b>  |
| VSSD2  | 66            | Ground       | -    | <b>VSSD2: CMOS CLK Output Ground</b>   |
| VSS_DIFF   | 17            | Ground       | -    | <b>VSS_DIFF: Differential I/O Ground</b>   |
| VSS_DIFF6  | 21            | Ground       | -    | <b>VSS_DIFF6: Differential I/O Ground</b>  |
| VSS_DIFF5  | 27            | Ground       | -    | <b>VSS_DIFF5: Differential I/O Ground</b>  |
| VSSA   | 1             | Ground       | -    | <b>VSSA: Common Ground</b>   |
| VSSA1  | 3             | Ground       | -    | <b>VSSAn: APLL Ground</b>  |
| VSSA2  | 7             |              |      |  |
| VSSA3  | 10            |              |      |  |
| VSSA4  | 11            |              |      |  |
| VSSA5  | 15            |              |      |  |
| VDDA1  | 4             | Power        | -    | <b>VDDAn: APLL Power</b>   |
| VDDA2  | 8             |              |      |  |
| VDDA3  | 9             |              |      |  |
| VDDA4  | 12            |              |      |  |
| VDDA5  | 14            |              |      |  |
| <b>Others</b>  |               |              |      |  |
| IC1  | 68            | -            | -    | <b>IC: Internal Connected</b><br>Internal Use. These pins should be left open for normal operation.  |
| IC2  | 69            |              |      |  |
| IC3  | 70            |              |      |  |
| NC   | 13, 41        | -            | -    | <b>NC: Not connected</b>   |
| <b>Note:</b>   |               |              |      |  |
| 1. All the unused input pins should be connected to ground; the output of all the unused output pins are don't-care. |               |              |      |  |
| 2. The contents in the brackets indicate the position of the register bit/bits.                                      |               |              |      |  |
| 3. N x 8 kHz: $1 \leq N \leq 19440$ .  |               |              |      |  |
| 4. N x E1: N = 1, 2, 3, 4, 6, 8, 12, 16  |               |              |      |  |
| 5. N x T1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24  |               |              |      |  |
| 6. N x 13.0 MHz: N = 1, 2  |               |              |      |  |
| 7. N x 3.84 MHz: N = 1, 2, 4, 8  |               |              |      |  |



## ORDERING INFORMATION



## REVISION HISTORY

August 01, 2012 Initial Release



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