# 5-Output 1.5V PCIe Gen1-2-3 Fanout Buffer with Zo=100ohms

9DBU0541

DATASHEET

## Description

The 9DBU0541 is a member of IDT's 1.5V Ultra-Low-Power (ULP) PCIe family. It has integrated terminations for direct connection to 100Ω transmission lines. The device has 5 output enables for clock management, and 3 selectable SMBus addresses.

## Recommended Application

1.5V PCIe Gen1-2-3 Fanout Buffer (FOB)

## Output Features

- 5 1–167MHz Low-Power (LP) HCSL DIF pairs with $Z_O$=100Ω

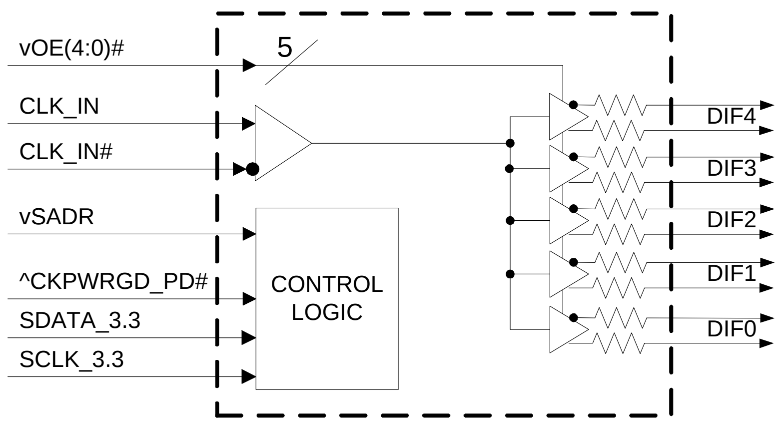
## Key Specifications

- DIF *additive* cycle-to-cycle jitter < 5ps
- DIF output-to-output skew < 60ps
- DIF *additive* phase jitter is < 300fs rms for PCIe Gen3
- DIF *additive* phase jitter < 350fs rms for SGMII

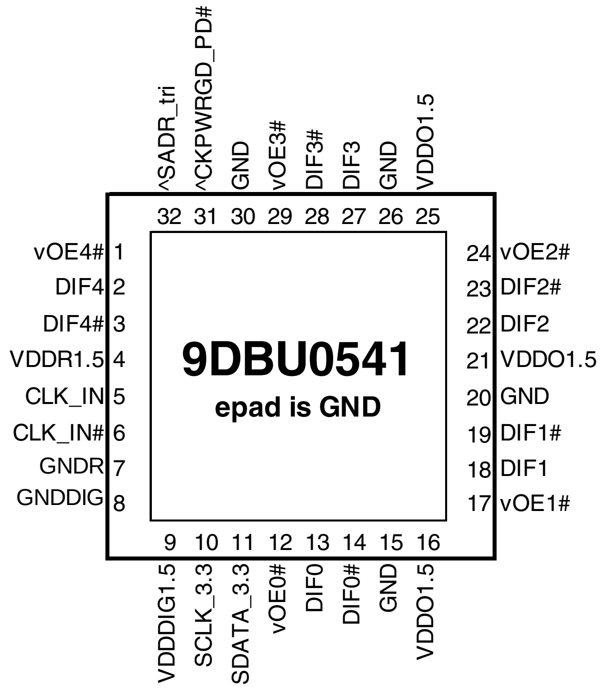
## Features/Benefits

- Integrated terminations; save 20 resistors compared to standard HCSL outputs
- 35mW typical power consumption; eliminates thermal concerns
- Spread Spectrum (SS) compatible; allows SS for EMI reduction
- OE# pins; support DIF power management
- HCSL-compatible differential input; can be driven by common clock sources
- SMBus-selectable features; optimize signal integrity to application
  - slew rate for each output
  - differential output amplitude
- Device contains default configuration; SMBus interface not required for device control
- 3.3V tolerant SMBus interface works with legacy controllers
- Selectable SMBus addresses; multiple devices can easily share an SMBus segment
- 5 × 5 mm 32-VFQFPN; minimal board space

## Block Diagram



## Pin Configuration




**32-pin VFQFPN, 5x5 mm, 0.5mm pitch**

^ prefix indicates internal 120KOhm pull up resistor
^v prefix indicates internal 120KOhm pull up AND pull down resistor (biased to VDD/2)
v prefix indicates internal 120KOhm pull down resistor

### SMBus Address Selection Table

| | SADR | Address | + Read/Write bit |
|---|---|---|---|
| State of SADR on first application of CKPWRGD_PD# | 0 | 1101011 | x |
| | M | 1101100 | x |
| | 1 | 1101101 | x |

### Power Management Table

| CKPWRGD_PD# | CLK_IN | SMBus OEx bit | OEx# Pin | DIFx | |
|---|---|---|---|---|---|
| | | | | True O/P | Comp. O/P |
| 0 | X | X | X | Low | Low |
| 1 | Running | 0 | X | Low | Low |
| 1 | Running | 1 | 0 | Running | Running |
| 1 | Running | 1 | 1 | Low | Low |

### Power Connections

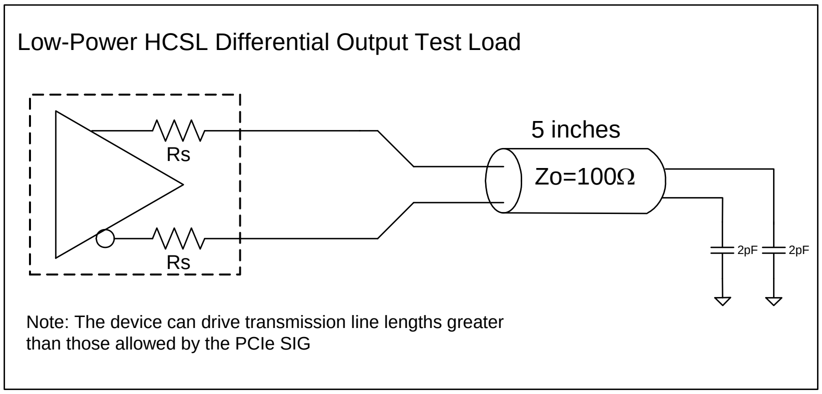
| Pin Number | | Description |
|---|---|---|
| VDD | GND | |
| 4 | 7 | Input receiver analog |
| 9 | 8 | Digital power |
| 16, 21, 25 | 15,20,26,30 | DIF outputs |

Note: EPAD on this device is not electrically connected to the die.
It should be connected to ground for best thermal performance.

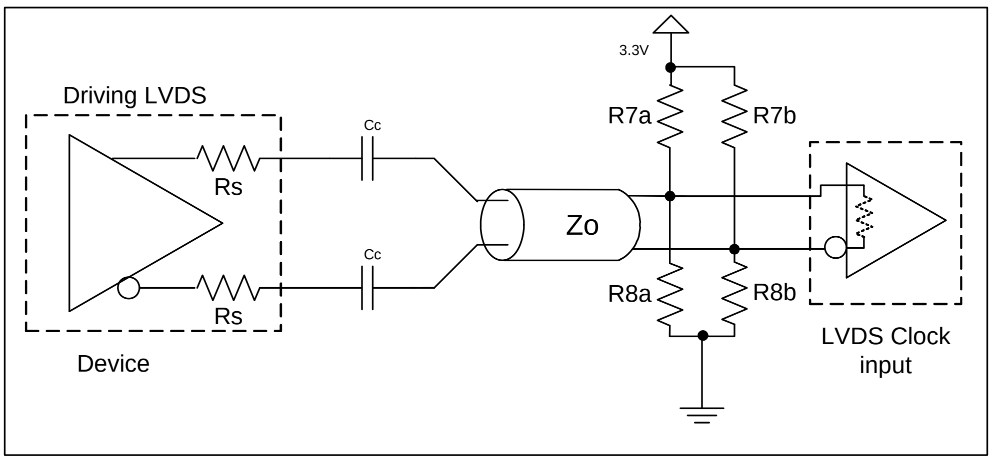
## Pin Descriptions

| Pin# | Pin Name | Type | Pin Description |
|---|---|---|---|
| 1 | vOE4# | IN | Active low input for enabling output 4. This pin has an internal 120kohm pull-down.<br>1 = disable outputs, 0 = enable outputs. |
| 2 | DIF4 | OUT | Differential true clock output. |
| 3 | DIF4# | OUT | Differential complementary clock output. |
| 4 | VDDR1.5 | PWR | 1.5V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately. |
| 5 | CLK_IN | IN | True input for differential reference clock. |
| 6 | CLK_IN# | IN | Complementary input for differential reference clock. |
| 7 | GNDR | GND | Analog ground pin for the differential input (receiver) |
| 8 | GNDDIG | GND | Ground pin for digital circuitry. |
| 9 | VDDDIG1.5 | PWR | 1.5V digital power (dirty power) |
| 10 | SCLK_3.3 | IN | Clock pin of SMBus circuitry, 3.3V tolerant. |
| 11 | SDATA_3.3 | I/O | Data pin for SMBus circuitry, 3.3V tolerant. |
| 12 | vOE0# | IN | Active low input for enabling output 0. This pin has an internal 120kohm pull-down.<br>1 = disable outputs, 0 = enable outputs. |
| 13 | DIF0 | OUT | Differential true clock output. |
| 14 | DIF0# | OUT | Differential complementary clock output. |
| 15 | GND | GND | Ground pin. |
| 16 | VDDO1.5 | PWR | Power supply for outputs, nominally 1.5V. |
| 17 | vOE1# | IN | Active low input for enabling output 1. This pin has an internal 120kohm pull-down.<br>1 = disable outputs, 0 = enable outputs. |
| 18 | DIF1 | OUT | Differential true clock output. |
| 19 | DIF1# | OUT | Differential complementary clock output. |
| 20 | GND | GND | Ground pin. |
| 21 | VDDO1.5 | PWR | Power supply for outputs, nominally 1.5V. |
| 22 | DIF2 | OUT | Differential true clock output. |
| 23 | DIF2# | OUT | Differential complementary clock output. |
| 24 | vOE2# | IN | Active low input for enabling output 2. This pin has an internal 120kohm pull-down.<br>1 = disable outputs, 0 = enable outputs. |
| 25 | VDDO1.5 | PWR | Power supply for outputs, nominally 1.5V. |
| 26 | GND | GND | Ground pin. |
| 27 | DIF3 | OUT | Differential true clock output. |
| 28 | DIF3# | OUT | Differential complementary clock output. |
| 29 | vOE3# | IN | Active low input for enabling output 3. This pin has an internal 120kohm pull-down.<br>1 = disable outputs, 0 = enable outputs. |
| 30 | GND | GND | Ground pin. |
| 31 | ^CKPWRGD_PD# | IN | Input notifies device to sample latched inputs and start up on first high assertion.<br>Low enters Power Down Mode, subsequent high assertions exit Power Down Mode.<br>This pin has internal 120kohm pull-up resistor. |
| 32 | ^SADR_tri | LATCHED IN | Tri-level latch to select SMBus Address. It has an internal 120kohm pull up resistor.<br>See SMBus Address Selection Table. |
| 33 | EPAD | GND | Connect EPAD to ground. |

## Test Loads




## Driving LVDS




**Driving LVDS Inputs**

| Component | Value | |
|---|---|---|
| | Receiver has termination | Receiver does not have termination |
| R7a, R7b | 10K ohm | 140 ohm |
| R8a, R8b | 5.6K ohm | 75 ohm |
| Cc | 0.1µF | 0.1µF |
| Vcm | 1.2 volts | 1.2 volts |

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBU0541. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | VDDx | Applies to all VDD pins | -0.5 | | 2 | V | 1,2 |
| Input Voltage | $V_{IN}$ | | -0.5 | | $V_{DD}$+0.5 | V | 1, |
| Input High Voltage, SMBus | $V_{IHSMB}$ | SMBus clock and data pins | | | 3.3 | V | 1 |
| Storage Temperature | Ts | | -65 | | 150 | °C | 1 |
| Junction Temperature | Tj | | | | 125 | °C | 1 |
| Input ESD Protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 2.0V.

## Electrical Characteristics–Clock Input Parameters

TA = $T_{AMB}$; Supply voltages per normal operation conditions; see Test Loads for loading conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Common Mode Voltage - DIF_IN | $V_{COM}$ | Common mode input voltage | 200 | | 725 | mV |
| Input Swing - DIF_IN | $V_{SWING}$ | Differential value | 300 | | 1450 | mV |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns |
| Input Leakage Current | $I_{IN}$ | $V_{IN} = V_{DD}$ , $V_{IN}$ = GND | -5 | | 5 | uA |
| Input Duty Cycle | $d_{tin}$ | Measurement from differential waveform | 45 | 50 | 55 | % |
| Input Jitter - Cycle to Cycle | $J_{DIFIn}$ | Differential measurement | 0 | | 150 | ps |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through +/-75mV window centered around differential zero.

# Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = $T_{AMB}$; Supply voltages per normal operation conditions; see Test Loads for loading conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | VDDx | Supply voltage for core and analog | 1.425 | 1.5 | 1.575 | V | |
| Ambient Operating Temperature | $T_{AMB}$ | Commercial range | 0 | 25 | 70 | °C | 1 |
| | | Industrial range | -40 | 25 | 85 | °C | 1 |
| Input High Voltage | $V_{IH}$ | Single-ended inputs, except SMBus | 0.75 $V_{DD}$ | | $V_{DD}$ + 0.3 | V | |
| Input Mid Voltage | $V_{IM}$ | Single-ended tri-level inputs ('_tri' suffix) | 0.4 $V_{DD}$ | | 0.6 $V_{DD}$ | V | |
| Input Low Voltage | $V_{IL}$ | Single-ended inputs, except SMBus | -0.3 | | 0.25 $V_{DD}$ | V | |
| Input Current | $I_{IN}$ | Single-ended inputs, $V_{IN}$ = GND, $V_{IN}$ = VDD | -5 | | 5 | µA | |
| | $I_{INP}$ | Single-ended inputs<br>$V_{IN}$ = 0 V; inputs with internal pull-up resistors<br>$V_{IN}$ = VDD; inputs with internal pull-down resistors | -200 | | 200 | µA | |
| Input Frequency | $F_{in}$ | | 1 | | 167 | MHz | 2 |
| Pin Inductance | $L_{pin}$ | | | | 7 | nH | 1 |
| Capacitance | $C_{IN}$ | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | $C_{INDIF\_IN}$ | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,5 |
| | $C_{OUT}$ | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | $T_{STAB}$ | From $V_{DD}$ power-up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1 | ms | 1,2 |
| Input SS Modulation Frequency PCIe | $f_{MODINPCIe}$ | Allowable frequency for PCIe applications (Triangular modulation) | 30 | | 33 | kHz | |
| Input SS Modulation Frequency non-PCIe | $f_{MODIN}$ | Allowable frequency for non-PCIe applications (Triangular modulation) | 0 | | 66 | kHz | |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion<br>DIF stop after OE# deassertion | 1 | | 3 | clocks | 1,3 |
| Tdrive_PD# | $t_{DRVPD}$ | DIF output enable after PD# de-assertion | | | 300 | µs | 1,3 |
| Tfall | $t_F$ | Fall time of single-ended control inputs | | | 5 | ns | 2 |
| Trise | $t_R$ | Rise time of single-ended control inputs | | | 5 | ns | 2 |
| SMBus Input Low Voltage | $V_{ILSMB}$ | | | | 0.6 | V | |
| SMBus Input High Voltage | $V_{IHSMB}$ | $V_{DDSMB}$ = 3.3V, see note 4 for $V_{DDSMB}$ < 3.3V | 2.1 | | 3.3 | V | 4 |
| SMBus Output Low Voltage | $V_{OLSMB}$ | at $I_{PULLUP}$ | | | 0.4 | V | |
| SMBus Sink Current | $I_{PULLUP}$ | at $V_{OL}$ | 4 | | | mA | |
| Nominal Bus Voltage | $V_{DDSMB}$ | Bus voltage | 1.425 | | 3.3 | V | |
| SCLK/SDATA Rise Time | $t_{RSMB}$ | (Max VIL - 0.15V) to (Min VIH + 0.15V) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | $t_{FSMB}$ | (Min VIH + 0.15V) to (Max VIL - 0.15V) | | | 300 | ns | 1 |
| SMBus Operating Frequency | $f_{MAXSMB}$ | Maximum SMBus operating frequency | | | 400 | kHz | 6 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200 mV.

[4] For $V_{DDSMB}$ < 3.3V, $V_{IHSMB}$ >= 0.8x$V_{DDSMB}$

[5] DIF_IN input.

[6] The differential input clock must be running for the SMBus to be active.

## Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = $T_{AMB}$; Supply voltages per normal operation conditions; see Test Loads for loading conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Slew Rate | dV/dt | Scope averaging on, fast setting | 1 | 2.4 | 3.5 | V/ns | 1,2,3 |
| | dV/dt | Scope averaging on, slow setting | 0.7 | 1.7 | 2.5 | V/ns | 1,2,3 |
| Slew Rate Matching | ΔdV/dt | Slew rate matching, scope averaging on | | 9 | 20 | % | 1,2,4 |
| Voltage High | $V_{HIGH}$ | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 630 | 750 | 850 | mV | 7 |
| Voltage Low | $V_{LOW}$ | | -150 | 26 | 150 | | 7 |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. (Scope averaging off) | | 763 | 1150 | mV | 7 |
| Min Voltage | Vmin | | -300 | 22 | | | 7 |
| Vswing | Vswing | Scope averaging off | 300 | 1448 | | mV | 1,2 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 250 | 390 | 550 | mV | 1,5 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off | | 11 | 140 | mV | 1,6 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

## Electrical Characteristics–Current Consumption

TA = $T_{AMB}$; Supply voltages per normal operation conditions; see Test Loads for loading conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Operating Supply Current | $I_{DDR}$ | VDDR at 100MHz | | 1.9 | 3 | mA | |
| | $I_{DDDIG}$ | VDDIG, all outputs at 100MHz | | 0.1 | 0.5 | mA | |
| | $I_{DDAO}$ | VDDO1.5+VDDO, all outputs at 100MHz | | 20 | 25 | mA | |
| Powerdown Current | $I_{DDRPD}$ | VDDR, CKPWRGD_PD# = 0 | | 0.001 | 0.3 | mA | 2 |
| | $I_{DDDIGPD}$ | VDDDIG, CKPWRGD_PD# = 0 | | 0.1 | 0.2 | mA | 2 |
| | $I_{DDAOPD}$ | VDDO1.5+VDDO, CKPWRGD_PD# = 0 | | 0.5 | 1 | mA | 2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Input clock stopped.

## Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = $T_{AMB}$; Supply voltages per normal operation conditions; see Test Loads for loading conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Duty Cycle Distortion | $t_{DCD}$ | Measured differentially, at 100MHz | -1 | -0.2 | 0.5 | % | 1,3 |
| Skew, Input to Output | $t_{pdBYP}$ | $V_T$ = 50% | 2400 | 2862 | 3700 | ps | 1 |
| Skew, Output to Output | $t_{sk3}$ | $V_T$ = 50% | | 30 | 50 | ps | 1,4 |
| Jitter, Cycle to Cycle | $t_{jcyc\text{-}cyc}$ | *Additive* Jitter | | 0.1 | 5 | ps | 1,2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock.

[4] All outputs at default slew rate.

## Electrical Characteristics–Phase Jitter Parameters

TA = $T_{AMB}$; Supply voltages per normal operation conditions; see Test Loads for loading conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | INDUSTRY LIMIT | UNITS | Notes |
|---|---|---|---|---|---|---|---|---|
| Additive Phase Jitter | $t_{jphPCIeG1}$ | PCIe Gen 1 | | 0.1 | 5 | N/A | ps (p-p) | 1,2,3,5 |
| | $t_{jphPCIeG2}$ | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.1 | 0.4 | N/A | ps (rms) | 1,2,3,4, 5 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 0.1 | 0.7 | N/A | ps (rms) | 1,2,3,4 |
| | $t_{jphPCIeG3}$ | PCIe Gen 3 (2-4MHz or 2-5MHz, CDR = 10MHz) | | 0.1 | 0.3 | N/A | ps (rms) | 1,2,3,4 |
| | $t_{jphSGMIIM0}$ | 125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz | | 200 | 250 | N/A | fs (rms) | 1,6 |
| | $t_{jphSGMIIM1}$ | 125MHz, 12kHz to 20MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz | | 313 | 350 | N/A | fs (rms) | 1,6 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] See http://www.pcisig.com for complete specs.

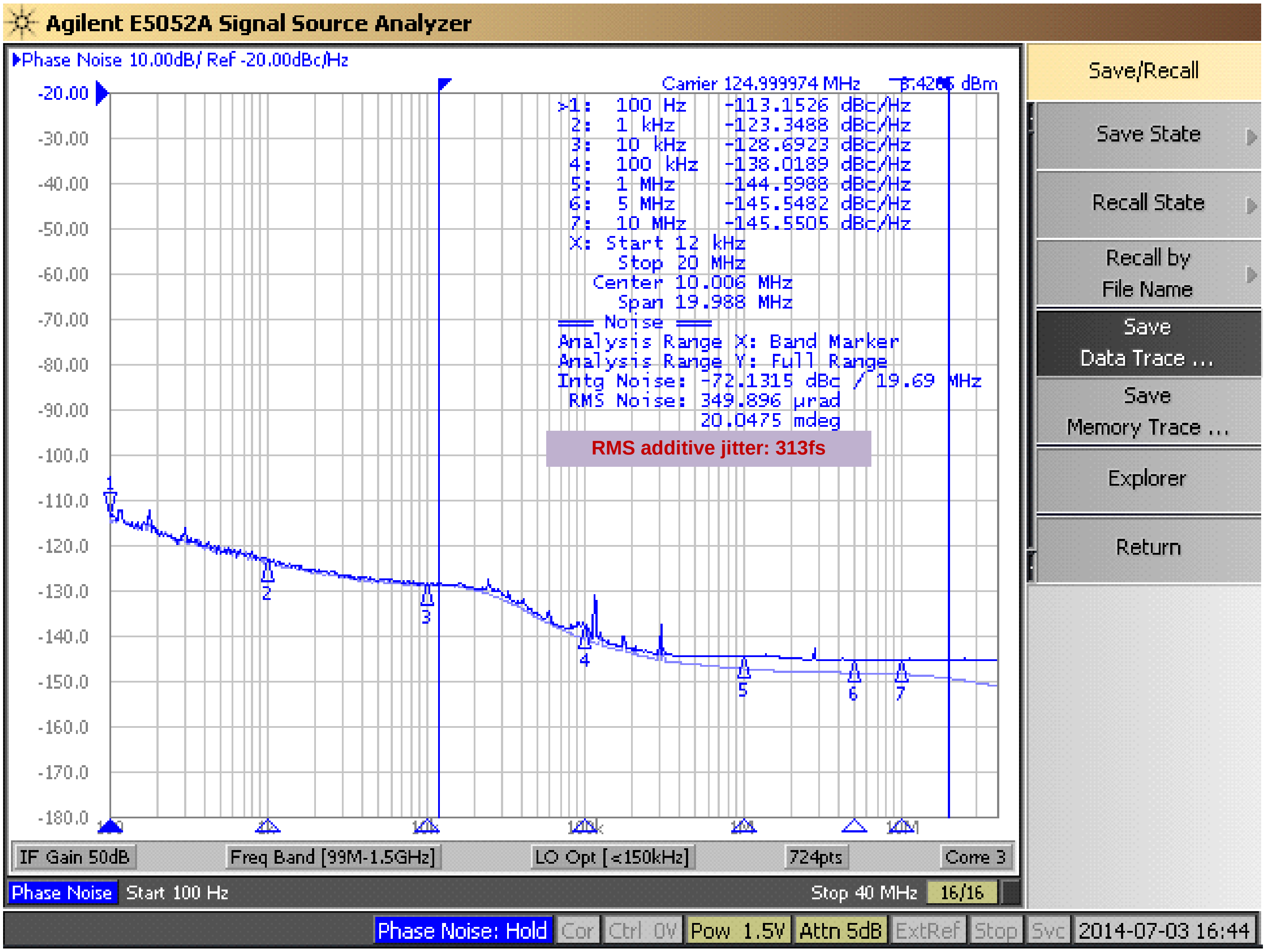
[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1-12.

[4] For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)^2 - (input jitter)^2].

[5] Driven by 9FGV0831 or equivalent.

[6] Rohde & Schwarz SMA100.

## Additive Phase Jitter Plot: 125M (12kHz to 20MHz)



# General SMBus Serial Interface Information

## How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

## How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation | | | |
|---|---|---|---|
| **Controller (Host)** | | | **IDT (Slave/Receiver)** |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

| Index Block Read Operation | | | |
|---|---|---|---|
| **Controller (Host)** | | | **IDT (Slave/Receiver)** |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | |
| | | | Data Byte Count=X |
| ACK | | | |
| | | X Byte | Beginning Byte N |
| ACK | | | |
| | | | O |
| O | | | O |
| O | | | O |
| O | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

**Note: SMBus Address is Latched on SADR pin.**

**SMBus Table: Output Enable Register [1]**

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 1 |
| Bit 6 | DIF OE3 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 5 | DIF OE2 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 4 | Reserved | | | | | 1 |
| Bit 3 | DIF OE1 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 2 | Reserved | | | | | 1 |
| Bit 1 | DIF OE0 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 0 | Reserved | | | | | 1 |

1. A low on these bits will override the OE# pin and force the differential output Low/Low

**SMBus Table: PLL Operating Mode and Output Amplitude Control Register**

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 1 |
| Bit 5 | DIF OE4 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | Reserved | | | | | 1 |
| Bit 2 | Reserved | | | | | 1 |
| Bit 1 | AMPLITUDE 1 | Controls Output Amplitude | RW | 00 = 0.55V | 01= 0.65V | 1 |
| Bit 0 | AMPLITUDE 0 | | RW | 10 = 0.7V | 11 = 0.8V | 0 |

1. A low on the DIF OE bit will override the OE# pin and force the differential output Low/Low

**SMBus Table: DIF Slew Rate Control Register**

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 1 |
| Bit 6 | SLEWRATESEL DIF3 | Slew Rate Selection | RW | Slow Setting | Fast Setting | 1 |
| Bit 5 | SLEWRATESEL DIF2 | Slew Rate Selection | RW | Slow Setting | Fast Setting | 1 |
| Bit 4 | Reserved | | | | | 1 |
| Bit 3 | SLEWRATESEL DIF1 | Slew Rate Selection | RW | Slow Setting | Fast Setting | 1 |
| Bit 2 | Reserved | | | | | 1 |
| Bit 1 | Slow Setting | Fast Setting | RW | Slow Setting | Fast Setting | 1 |
| Bit 0 | Reserved | | | | | 1 |

**Note: See "DIF 0.7V Low-Power HCSL Outputs" table for slew rates.**

**SMBus Table: DIF Slew Rate Control Register**

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 1 |
| Bit 6 | Reserved | | | | | 1 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | Reserved | | | | | 0 |
| Bit 2 | Reserved | | | | | 1 |
| Bit 1 | Reserved | | | | | 1 |
| Bit 0 | SLEWRATESEL DIF4 | Adjust Slew Rate of DIF4 | RW | Slow Setting | Fast Setting | 1 |

**Note: See "DIF 0.7V Low-Power HCSL Outputs" table for slew rates.**

**Byte 4 is Reserved and reads back 'hFF**

**SMBus Table: Revision and Vendor ID Register**

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | RID3 | Revision ID | R | A rev = 0000 | | 0 |
| Bit 6 | RID2 | | R | | | 0 |
| Bit 5 | RID1 | | R | | | 0 |
| Bit 4 | RID0 | | R | | | 0 |
| Bit 3 | VID3 | VENDOR ID | R | 0001 = IDT/ICS | | 0 |
| Bit 2 | VID2 | | R | | | 0 |
| Bit 1 | VID1 | | R | | | 0 |
| Bit 0 | VID0 | | R | | | 1 |

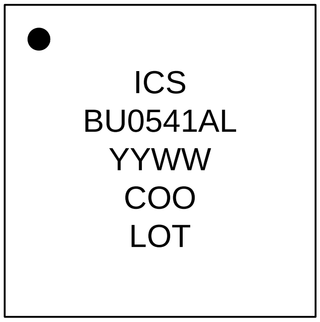
**SMBus Table: Device Type/Device ID**

| Byte 6 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Device Type1 | Device Type | R | 00 = FGx, 01 = DBx, 10 = DMx, 11= DBx w/oPLL | | 1 |
| Bit 6 | Device Type0 | | R | | | 1 |
| Bit 5 | Device ID5 | Device ID | R | 000101 binary or 05 hex | | 0 |
| Bit 4 | Device ID4 | | R | | | 0 |
| Bit 3 | Device ID3 | | R | | | 0 |
| Bit 2 | Device ID2 | | R | | | 1 |
| Bit 1 | Device ID1 | | R | | | 0 |
| Bit 0 | Device ID0 | | R | | | 1 |

**SMBus Table: Byte Count Register**

| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | BC4 | Byte Count Programming | RW | Writing to this register will configure how many bytes will be read back, default is = 8 bytes. | | 0 |
| Bit 3 | BC3 | | RW | | | 1 |
| Bit 2 | BC2 | | RW | | | 0 |
| Bit 1 | BC1 | | RW | | | 0 |
| Bit 0 | BC0 | | RW | | | 0 |

## Marking Diagrams





Notes:

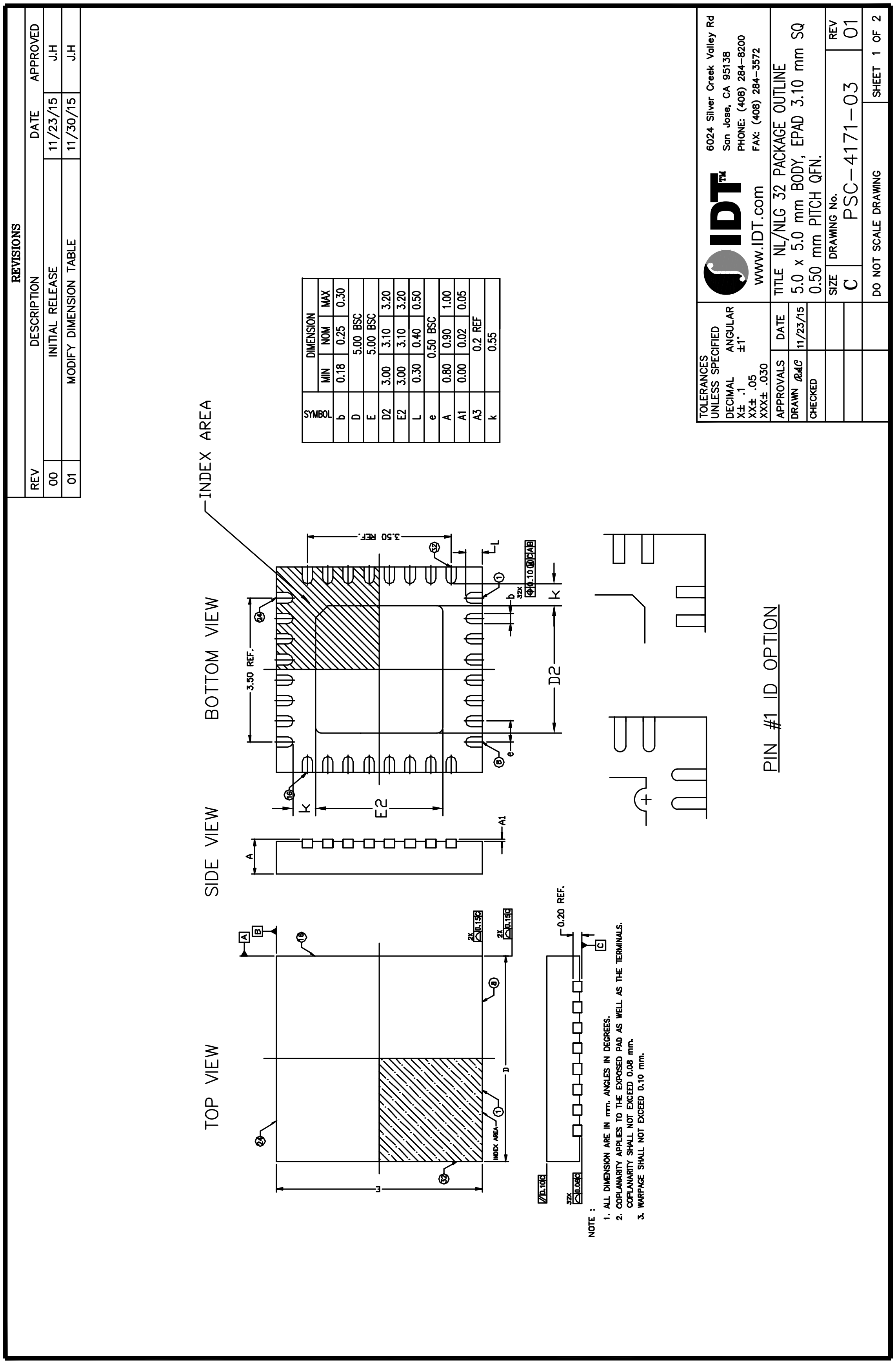
1. “LOT” is the lot sequence number.
2. “COO” denotes country of origin.
3. YYWW is the last two digits of the year and week that the part was assembled.
4. Line 2: truncated part number
5. “L” denotes RoHS compliant package.
6. “I” denotes industrial temperature range device.

## Thermal Characteristics

| PARAMETER | SYMBOL | CONDITIONS | PKG | TYP VALUE | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Thermal Resistance | $\theta_{JC}$ | Junction to Case | NLG32 | 42 | °C/W | 1 |
| | $\theta_{Jb}$ | Junction to Base | | 2.4 | °C/W | 1 |
| | $\theta_{JA0}$ | Junction to Air, still air | | 39 | °C/W | 1 |
| | $\theta_{JA1}$ | Junction to Air, 1 m/s air flow | | 33 | °C/W | 1 |
| | $\theta_{JA3}$ | Junction to Air, 3 m/s air flow | | 28 | °C/W | 1 |
| | $\theta_{JA5}$ | Junction to Air, 5 m/s air flow | | 27 | °C/W | 1 |

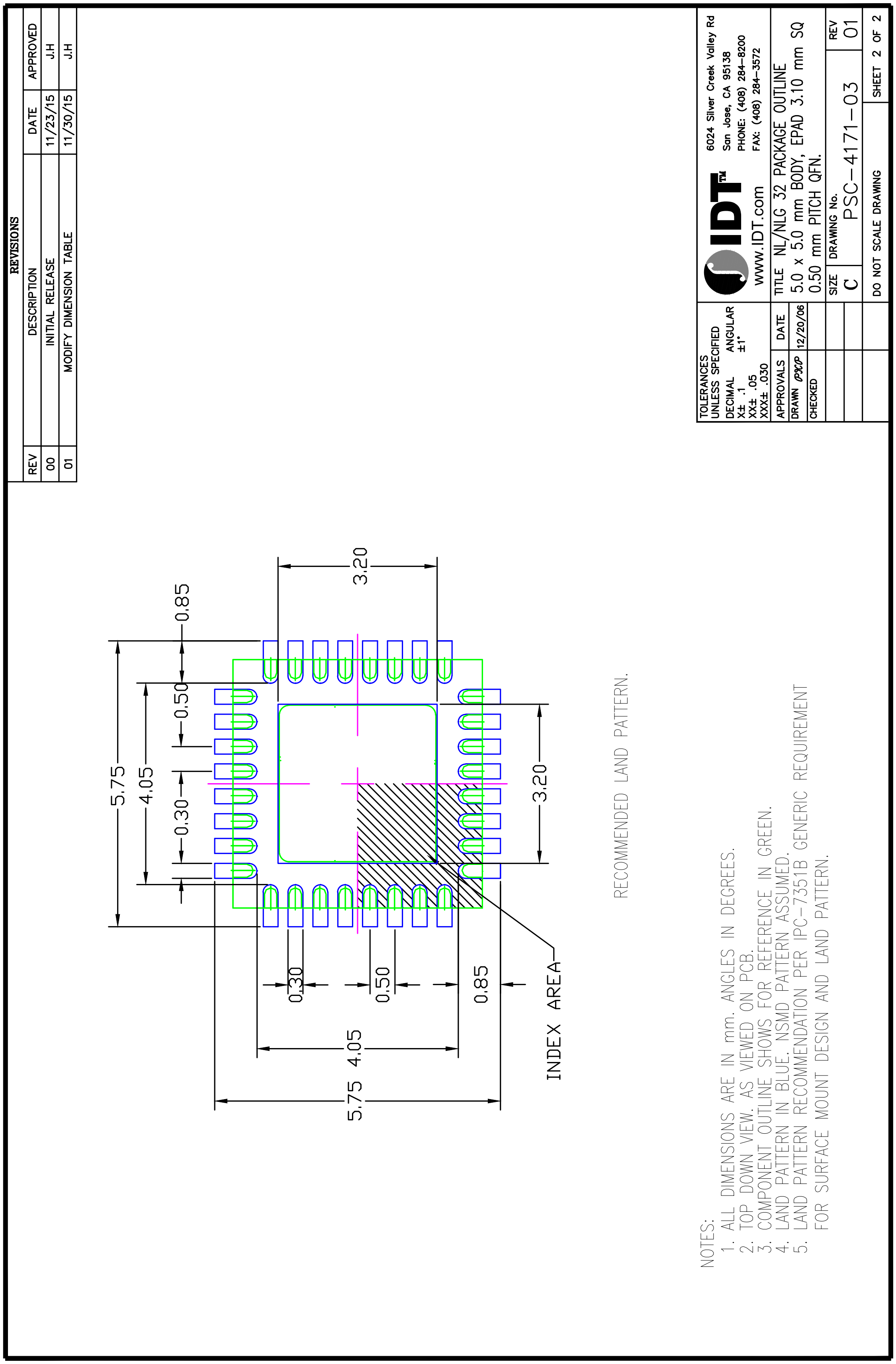
[1]ePad soldered to board

## Package Outline and Dimensions (NLG32)




| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| b | 0.18 | 0.25 | 0.30 |
| D | | 5.00 BSC | |
| E | | 5.00 BSC | |
| D2 | 3.00 | 3.10 | 3.20 |
| E2 | 3.00 | 3.10 | 3.20 |
| L | 0.30 | 0.40 | 0.50 |
| e | | 0.50 BSC | |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.2 REF | |
| k | | 0.55 | |

# Package Outline and Dimensions (NLG32), cont.



## Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---|---|---|---|
| 9DBU0541AKLF | Trays | 32-pin VFQFPN | 0 to +70° C |
| 9DBU0541AKLFT | Tape and Reel | 32-pin VFQFPN | 0 to +70° C |
| 9DBU0541AKILF | Trays | 32-pin VFQFPN | -40 to +85° C |
| 9DBU0541AKILFT | Tape and Reel | 32-pin VFQFPN | -40 to +85° C |

**“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.**
**“A” is the device revision designator (will not correlate with the datasheet revision).**

## Revision History

| Rev. | Initiator | Issue Date | Description | Page # |
|---|---|---|---|---|
| A | RDW | 7/15/2014 | Final update and release - front page and electrical tables. | Various |
| B | RDW | 7/24/2014 | 1. Removed VDDIO reference in the Electrical Characteristics - Input/Supply/Common Parameters and Absolute Maximum Ratings tables. This power rail does not exist on this device. The pinout and the pin descriptions are correct. | 6 |
| C | RDW | 9/19/2014 | Updated SMBus Input High/Low parameters conditions, MAX values, and footnotes. | 6 |
| D | RDW | 4/22/2015 | 1. Updated Key Specifications to be consistent across the family.<br>2. Updated pin out and pin descriptions to show ePad on package connected to ground.<br>3. Updated Clock Input Parameters table to be consistent with PCIe Vswing parameter.<br>4. Add note about epad to Power Connections table. | 1-3,5 |
| E | RDW | 2/16/2017 | 1. Updated pins 21 and 20 from VDDA1.5/GNDA to VDDO1.5/GND to clearly indicate that this part has no PLL. | 2, 3 |
| F | RDW | 3/9/2017 | 1. Removed "Bypass Mode" reference in "Output Duty Cycle..." and "Phase Jitter Parameters" tables; update note 3 under Output Duty Cycle table.<br>2. Corrected spelling errors/typos.<br>3. Change VDDA to VDDO1.5 in Current Consumption table.<br>4. Update Additive Phase Jitter conditions for PCIe Gen3. | 7, 8 |

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