1:2, Differential-to-LVCMOS/LVTTL Zero Delay Clock Generator

87002-02

DATA SHEET

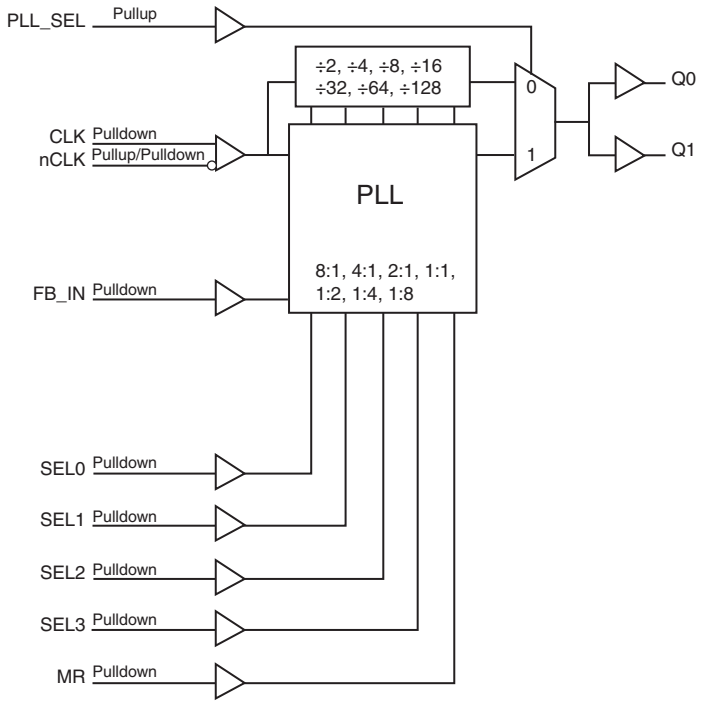
General Description

The 87002-02 is a highly versatile 1:2 Differential-to-LVCMOS/LVTTL Clock Generator. The 87002-02 has a differential clock input. The CLK, nCLK pair can accept most standard differential input levels. Internal bias on the nCLK input allows the CLK input to accept LVCMOS/LVTTL. The 87002-02 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider and has an input and output frequency range of 15.625MHz to 250MHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve “zero delay” between the input clock and the output clocks. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

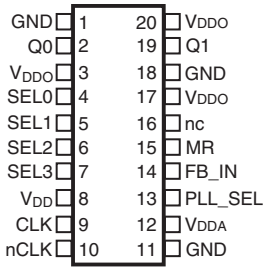
Features

- Two LVCMOS/LVTTL outputs, 7Ω typical output impedance
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, HSTL, HCSL, SSTL
- Internal bias on nCLK to support LVCMOS/LVTTL levels on CLK input
- Output frequency range: 15.625MHz to 250MHz
- Input frequency range: 15.625MHz to 250MHz
- VCO range: 250MHz to 500MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Fully integrated PLL
- Cycle-to-cycle jitter: 45ps (maximum)
- Output skew: 35ps (maximum)
- Static phase offset: -10ps ± 150ps (3.3V ± 5%)
- Full 3.3V or 2.5V operating supply
- 5V tolerant inputs
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- Industrial temperature information available upon request

Block Diagram



Pin Assignment



87002-02

20-Lead TSSOP
6.50mm x 4.40mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 11, 18	GND	Power		Power supply ground.
2, 19	Q0, Q1	Output		Single-ended clock outputs. 7Ω typical output impedance. LVCMOS/LVTTL interface levels.
3, 17, 20	V_{DDO}	Power		Output supply pins.
4, 5, 6, 7	SEL0, SEL1, SEL2, SEL3	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
8	V_{DD}	Power		Core supply pin.
9	CLK	Input	Pulldown	Non-inverting differential clock input.
10	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
12	V_{DDA}	Power		Analog supply pin.
13	PLL_SEL	Input	Pullup	PLL select. Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock (PLL Bypass). When HIGH, selects PLL (PLL enabled). LVCMOS/LVTTL interface levels.
14	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with “Zero Delay.” Connect to one of the outputs. LVCMOS/LVTTL interface levels.
15	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
16	nc	Unused		No connect.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDA}, V_{DDO} = 3.465V			23	pF
		V_{DD}, V_{DDA}, V_{DDO} = 2.625V			17	pF
R_{OUT}	Output Impedance		5	7	12	Ω

Function Tables

Table 3A. PLL Enable Function Table

Inputs					Outputs PLL_SEL = 1 PLL Enable Mode
SEL3	SEL2	SEL1	SEL0	Reference Frequency Range (MHz)	Q0, Q1
0	0	0	0	125 - 250	÷1
0	0	0	1	62.5 - 125	÷1
0	0	1	0	31.25 - 62.5	÷1
0	0	1	1	15.625 - 31.25	÷1
0	1	0	0	125 - 250	÷2
0	1	0	1	62.5 - 125	÷2
0	1	1	0	31.25 - 62.5	÷2
0	1	1	1	125 - 250	÷4
1	0	0	0	62.5 - 125	÷4
1	0	0	1	125 - 250	÷8
1	0	1	0	62.5 - 125	x2
1	0	1	1	31.25 - 62.5	x2
1	1	0	0	15.625 - 31.25	x2
1	1	0	1	31.25 - 62.5	x4
1	1	1	0	15.625 - 31.25	x4
1	1	1	1	15.625 - 31.25	x8

Table 3B. PLL Bypass Function Table

Inputs				Outputs PLL_SEL = 0 PLL Bypass Mode
SEL3	**SEL2**	**SEL1**	**SEL0**	**Q0, Q1**
0	0	0	0	÷8
0	0	0	1	÷8
0	0	1	0	÷8
0	0	1	1	÷16
0	1	0	0	÷16
0	1	0	1	÷16
0	1	1	0	÷32
0	1	1	1	÷32
1	0	0	0	÷64
1	0	0	1	÷128
1	0	1	0	÷4
1	0	1	1	÷4
1	1	0	0	÷8
1	1	0	1	÷2
1	1	1	0	÷4
1	1	1	1	÷2

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				100	mA
I_{DDA}	Analog Supply Current				16	mA
I_{DDO}	Output Supply Current				6	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				96	mA
I_{DDA}	Analog Supply Current				15	mA
I_{DDO}	Output Supply Current				6	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
			$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{DD} = 3.3V$	-0.3		0.8	V
			$V_{DD} = 2.5V$	-0.3		0.7	V
I_{IH}	Input High Current	FB_IN, SEL[0:3], MR	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	µA
		PLL_SEL	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	µA
I_{IL}	Input Low Current	FB_IN, SEL[0:3], MR	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
		PLL_SEL	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO} = 3.465V$	2.6			V
			$V_{DDO} = 2.625V$	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDO} = 3.465V$ or $2.625V$			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. In the Parameter Measurement Information Section, see *Output Load Test Circuit Diagrams.*

Table 4D. Differential DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	µA
		nCLK	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	µA
I_{IL}	Input Low Current	CLK	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
		nCLK	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		$V_{DD} – 0.85$	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		15.625		250	MHz
t_{PD}	Propagation Delay; NOTE 1	PLL_SEL = 0V, f ≤ 250MHz, Qx ÷ 2	4.8		5.8	ns
t(Ø)	Static Phase Offset; NOTE 2, 4	PLL_SEL = 3.3V, f_{REF} ≤ 167MHz, Qx ÷ 1	-160	-10	140	ps
*t*sk(o)	Output Skew; NOTE 3, 4	PLL_SEL = 0V			40	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4	f_{OUT} > 40MHz			45	ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	400		800	ps
odc	Output Duty Cycle		40		60	%

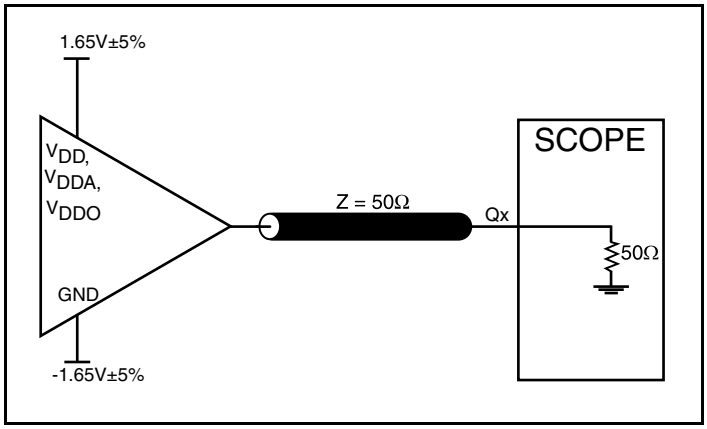
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

Table 5B. AC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

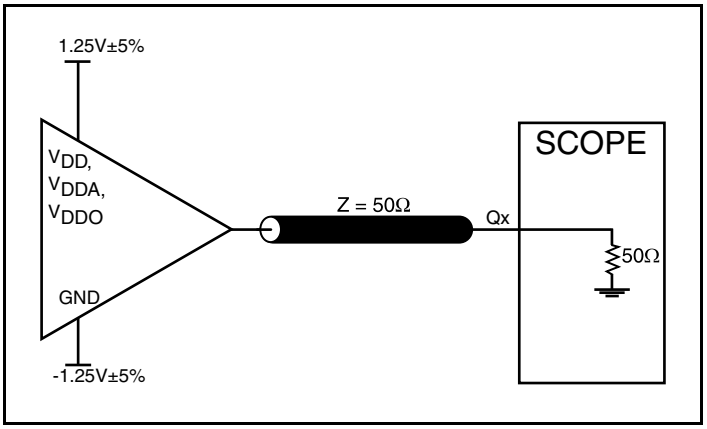
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		15.625		250	MHz
t_{PD}	Propagation Delay; NOTE 1	PLL_SEL = 0V, f ≤ 250MHz, Qx ÷ 2	4.9		6.7	ns
t(Ø)	Static Phase Offset; NOTE 2, 4	PLL_SEL = 2.5V, f_{REF} ≤ 167MHz, Qx ÷ 1	-240	-65	110	ps
*t*sk(o)	Output Skew; NOTE 3, 4	PLL_SEL = 0V			35	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4	f_{OUT} > 40MHz			45	ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	400		700	ps
odc	Output Duty Cycle		44		56	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

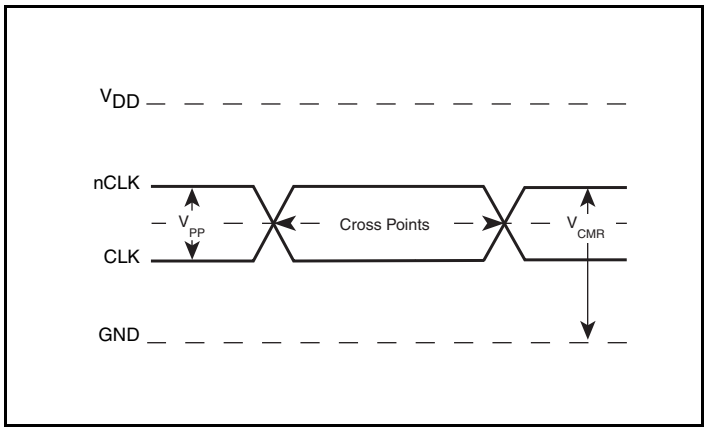
Parameter Measurement Information



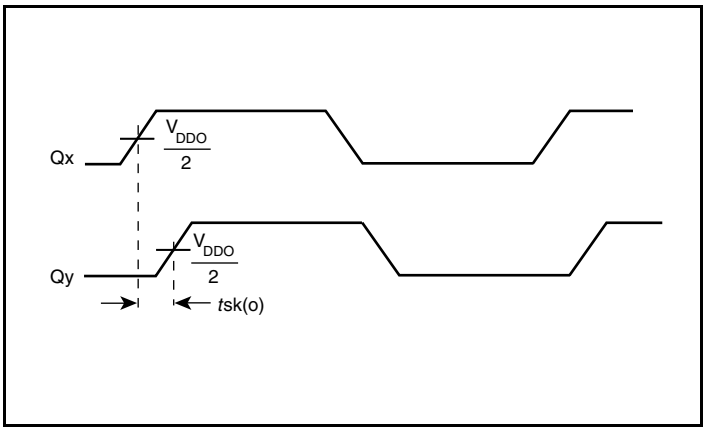
3.3V Output Load AC Test Circuit



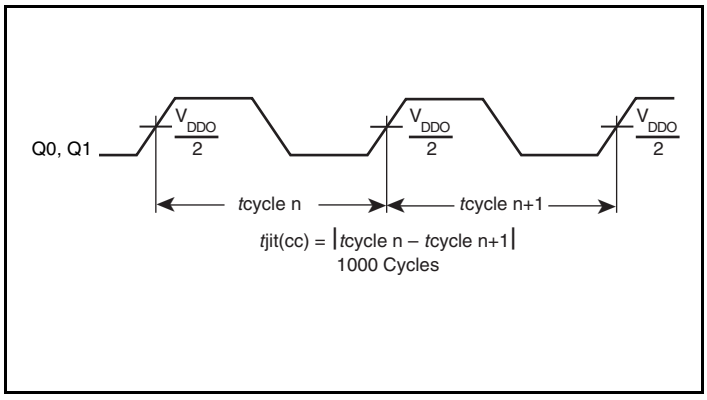
2.5V Output Load AC Test Circuit



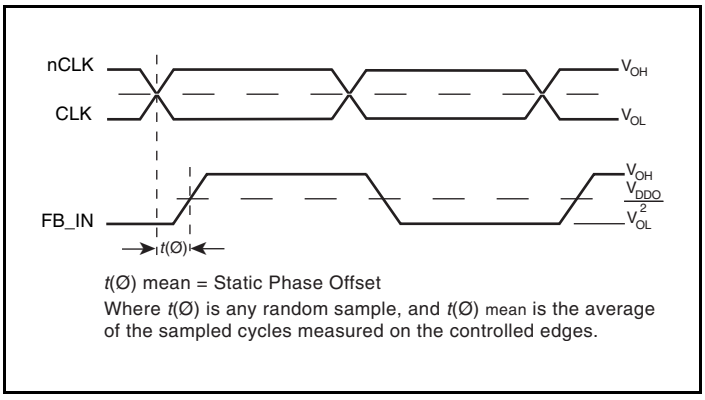
Differential Input Level



Output Skew

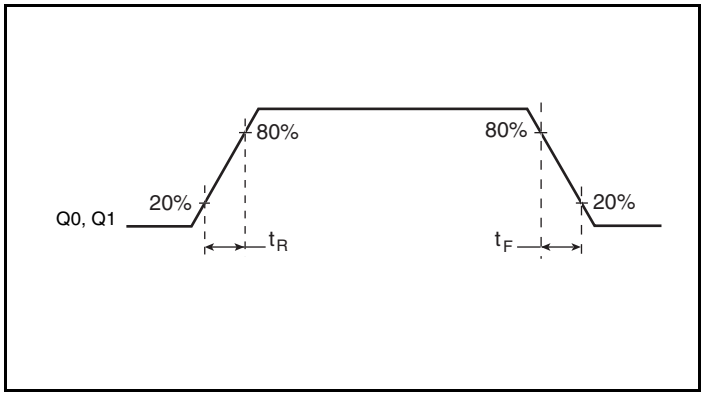


Cycle-to-Cycle Jitter

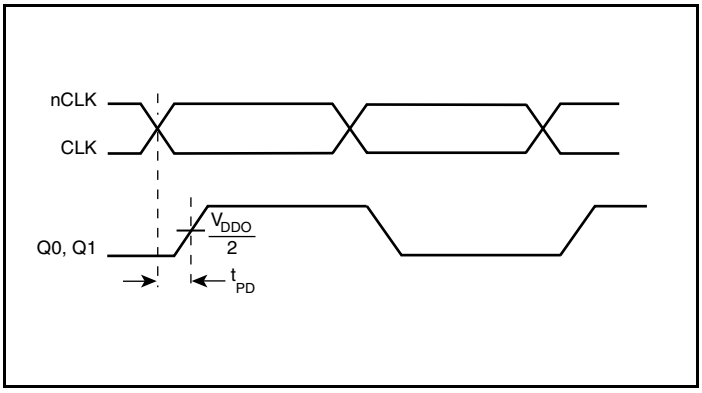


Static Phase Offset

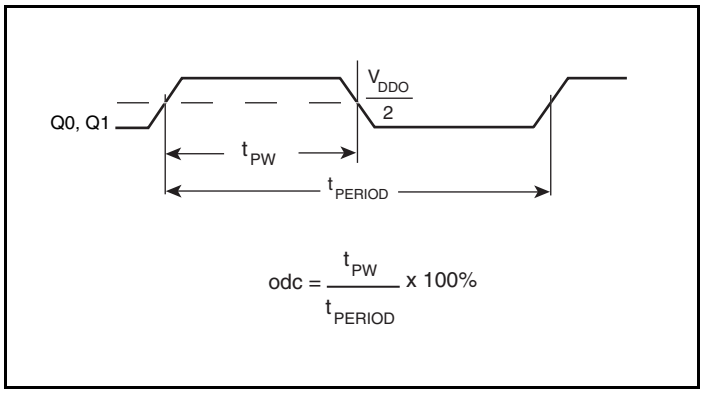
Parameter Measurement Information, continued



Output Rise/Fall Time



Propagation Delay



Output Duty Cycle/Pulse Width/Period

Applications Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 87002-02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

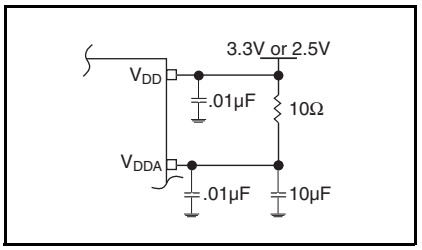


Figure 1. Power Supply Filtering

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

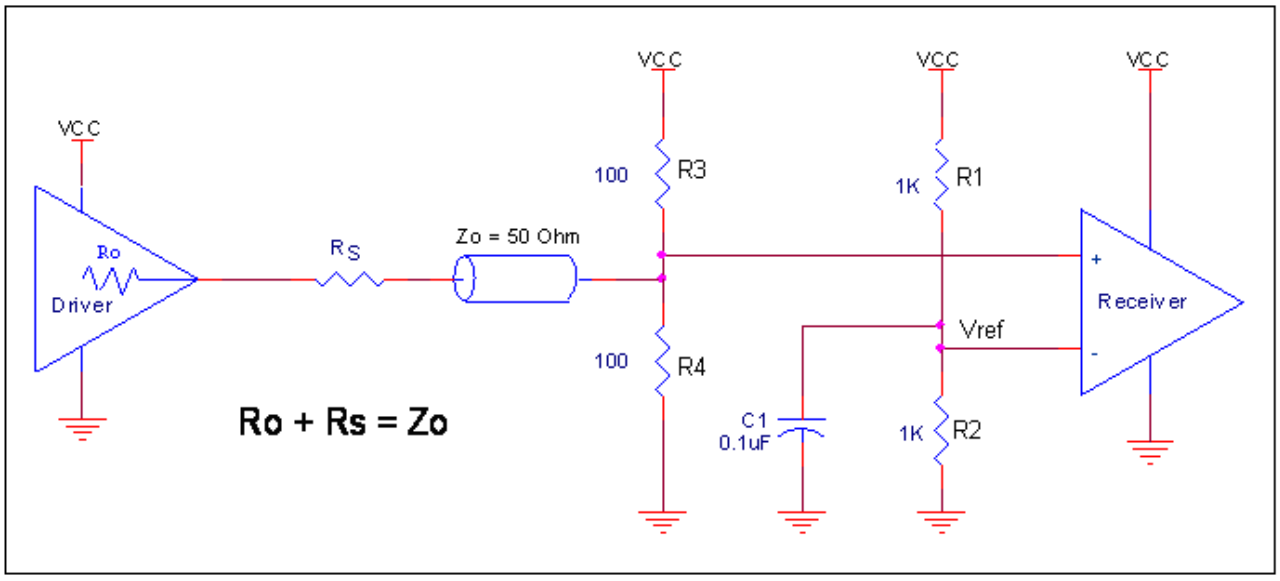


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

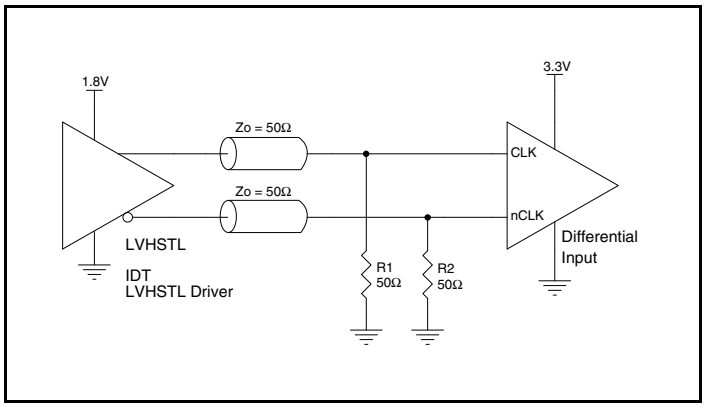


Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

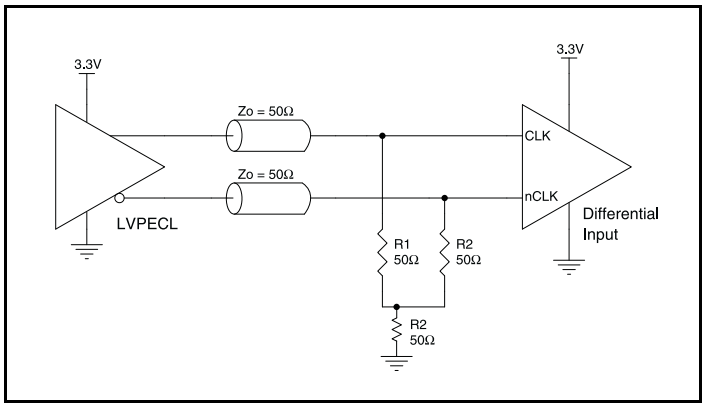


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

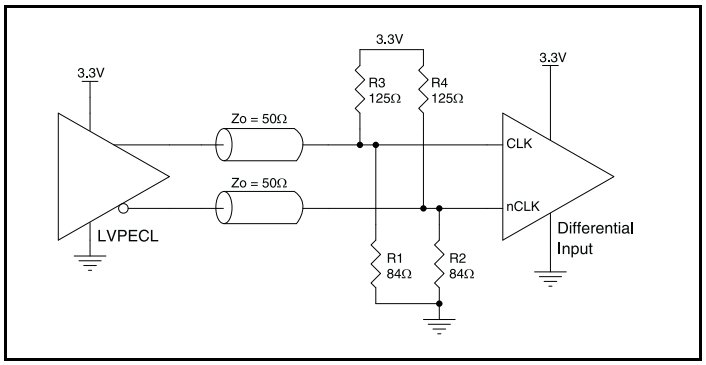


Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

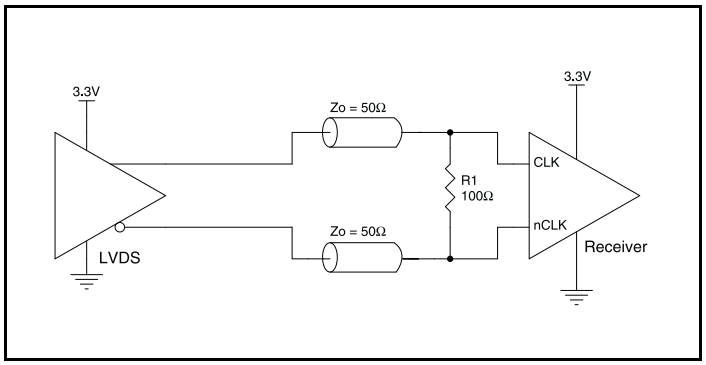


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

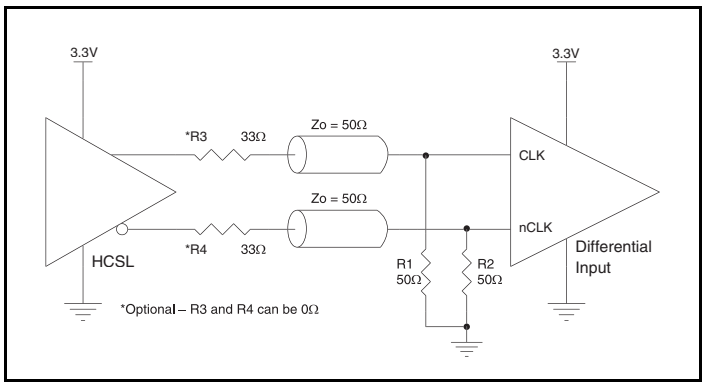


Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

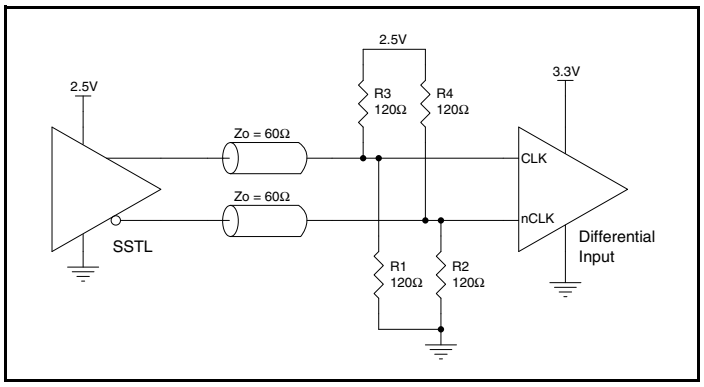


Figure 3F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

Schematic Example

Figure 4 shows an example of 87002-02 application schematic. In this example, the device is operated at V_{DD} = 3.3V. The decoupling capacitors should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver.

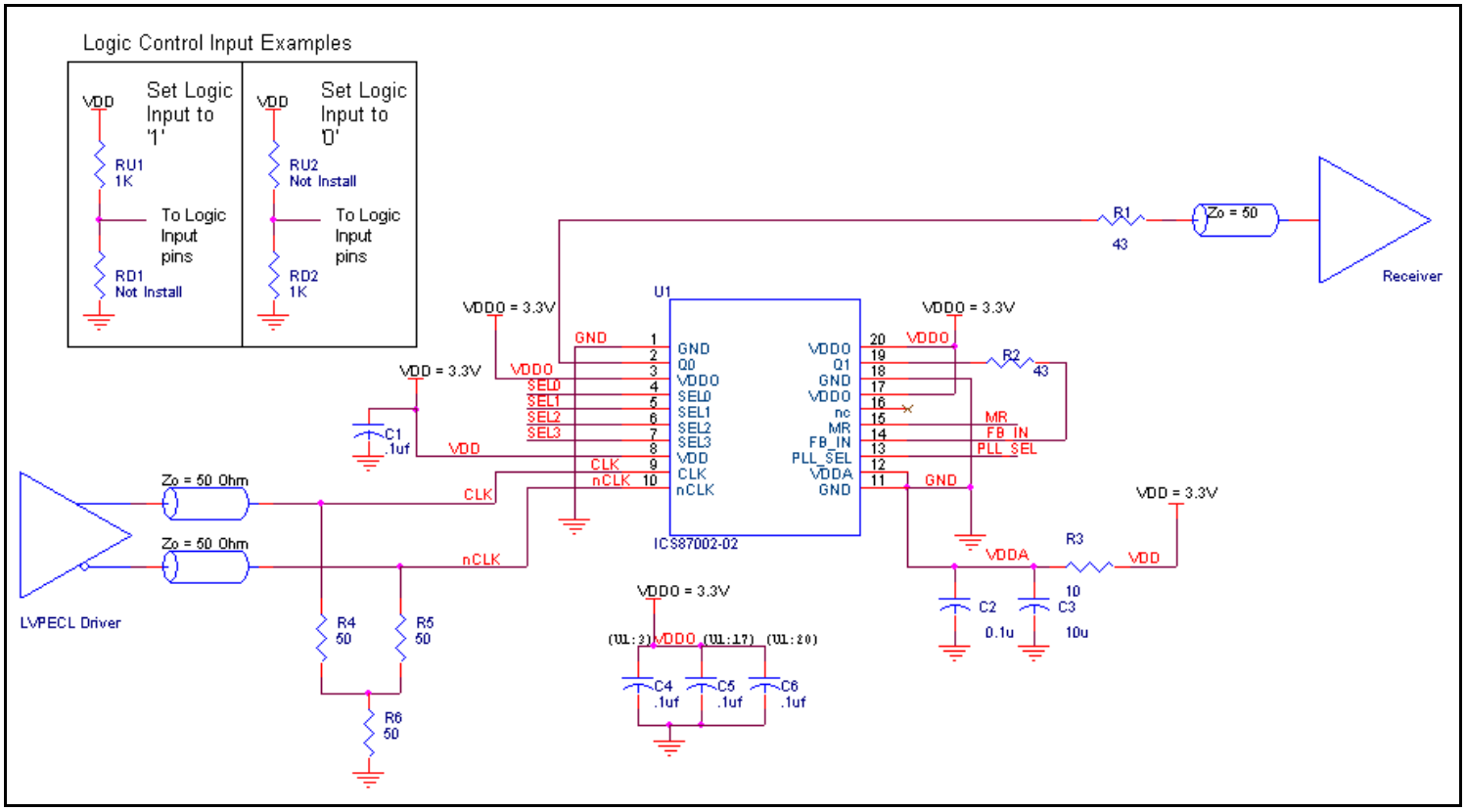


Figure 4. 87002-02 Schematic Example

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

Transistor Count

The transistor count for 87002-02 is: 2578

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

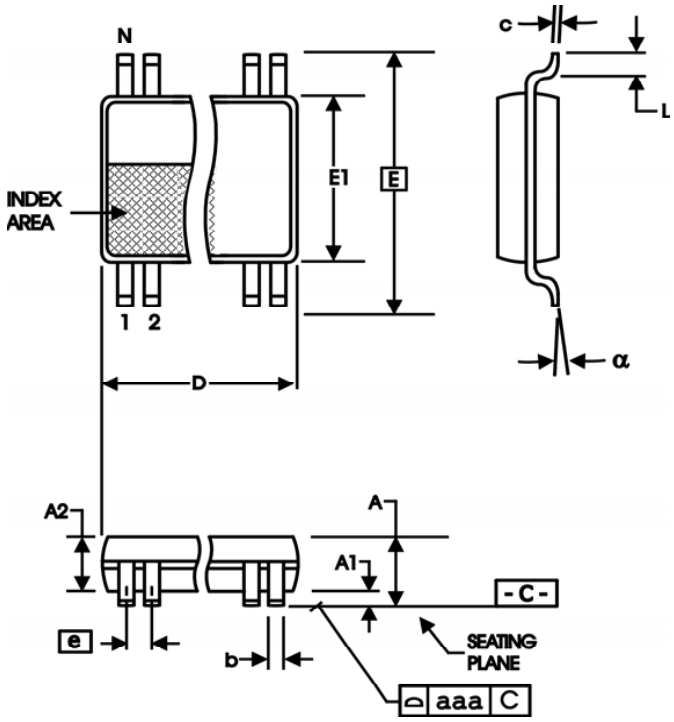


Table 7. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87002AG-02LF	ICS87002A02L	“Lead-Free” 20 Lead TSSOP	Tube	0°C to 70°C
87002AG-02LFT	ICS87002A02L	“Lead-Free” 20 Lead TSSOP	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T2	2	Pin Characteristics Table - added C_{PD} specs.	4/29/08
		10	Added *Recommendations for Unused Input and Output Pins* section.	
		11	Updated *Differential Clock Input Interface* section.	
		12	Added Schematic Layout	
	T8	14	Ordering Information Table - added Lead-Free marking.	
C	T5A, T5B	7	Added thermal note.	8/9/10
	T5B	7	2.5V AC Characteristics Table - due to datasheet conversion on April 29, 2008, corrected typo for static phase offset spec from -650 to -65.	
		10	Updated *Wiring the Differential Levels to Accept Single-ended Levels* section.	
	T8	14	Ordering Information Table - deleted “ICS” prefix from the Part/Order Number column. Updated header/footer of datasheet.	
C	T8	14	Ordering Information - removed leaded devices. Updated data sheet format.	7/13/15

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