

14 MHz to 190 MHz PLL Clock Multiplier

NB3N502

Description

The NB3N502 is a clock multiplier device that generates a low jitter, TTL/CMOS level output clock which is a precise multiple of the external input reference clock signal source. The device is a cost efficient replacement for the crystal oscillators commonly used in electronic systems. It accepts a standard fundamental mode crystal or an external reference clock signal. Phase-Locked-Loop (PLL) design techniques are used to produce an output clock up to 190 MHz with a 50% duty cycle. The NB3N502 can be programmed via two select inputs (S0, S1) to provide an output clock (CLKOUT) at one of six different multiples of the input frequency source, and at the same time output the input aligned reference clock signal (REF).

Features

- Clock Output Frequency up to 190 MHz
- Operating Range: $V_{DD} = 3\text{ V to }5.5\text{ V}$
- Low Jitter Output of 15 ps One Sigma (rms)
- Zero ppm Clock Multiplication Error
- 45% – 55% Duty Cycle
- 25 mA TTL-level Drive Outputs
- Crystal Reference Input Range of 5 – 27 MHz
- Input Clock Frequency Range of 2 – 50 MHz
- Available in 8-pin SOIC Package or in Die Form
- Full Industrial Temperature Range $-40^{\circ}\text{C to }85^{\circ}\text{C}$
- These are Pb-Free Devices

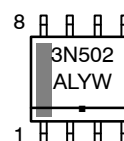


ON Semiconductor®

www.onsemi.com

MARKING DIAGRAM

8
1
SOIC-8
D SUFFIX
CASE 751



3N502 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NB3N502DG	SOIC-8 (Pb-Free)	98 Units / Rail
NB3N502DR2G	SOIC-8 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

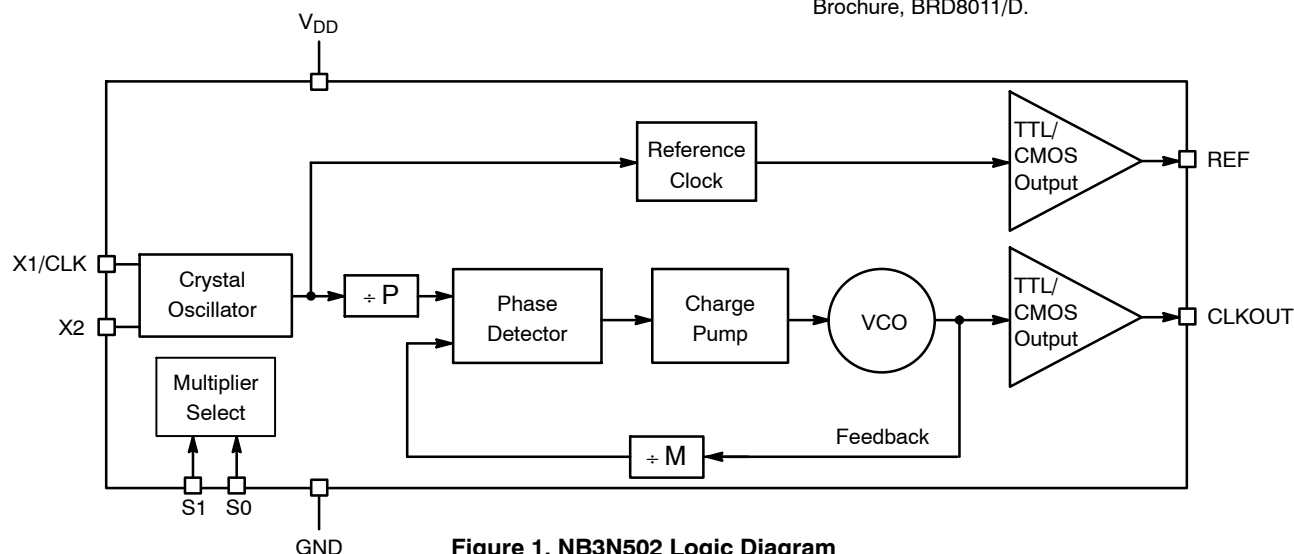


Figure 1. NB3N502 Logic Diagram

NB3N502

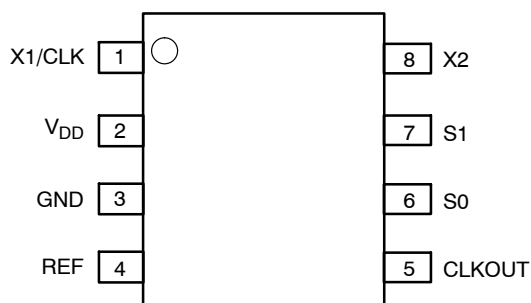


Figure 2. Pin Configuration (Top View)

Table 1. CLOCK MULTIPLIER SELECT TABLE

S1*	S0**	Multiplier
L	L	2X
L	H	5X
M	L	3X
M	H	3.33X
H	L	4X
H	H	2.5X

L = GND

H = V_{DD}

M = OPEN (unconnected)

* Pin S1 defaults to M when left open

** Pin S0 defaults to H when left open

Table 2. OUTPUT FREQUENCY EXAMPLES

Output Frequency (MHz)	20	25	33.3	48	50	54	64	66.66	75	100	108	120	135
Input Frequency (MHz)	10	10	10	16	20	13.5	16	20	15	20	27	24	27
S1, S0	0, 0	1, 1	M, 1	M, 0	1, 1	1, 0	1, 0	M, 1	0, 1	0, 1	1, 0	0, 1	0, 1

Table 3. PIN DESCRIPTION

Pin #	Name	I/O	Description
1	X1/CLK	Input	Crystal or External Reference Clock Input
2	V _{DD}	Power Supply	Positive Supply Voltage (3 V to 5.5 V)
3	GND	Power Supply	0 V Ground.
4	REF	CMOS/TTL Output	Buffered Crystal Oscillator Clock Output
5	CLKOUT	CMOS/TTL Output	Clock Output
6	S0	CMOS/TTL Input	Multiplier Select Pin – Connect to V _{DD} or GND. Internal Pull-up Resistor.
7	S1	Three-level Input	Multiplier Select Pin – Connect to V _{DD} , GND or Float to M.
8	X2	Crystal Input	Crystal Input – Do Not Connect when Providing an External Clock Reference

Table 4. ATTRIBUTES

Characteristic	Value
ESD Protection Human Body Model Machine Model	> 8 kV > 600 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	6700 Devices
Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test	

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{DD}	Positive Power Supply	GND = 0 V		7	V
V _I	Input Voltage			GND – 0.5 = V _I = V _{DD} + 0.5	V
T _A	Operating Temperature Range			–40 to +85	°C
T _{stg}	Storage Temperature Range			–65 to +150	°C
θ _{JA}	Thermal Resistance (Junction–to–Ambient)	0 LFPM 500 LFPM	SOIC–8 SOIC–8	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction–to–Case)	(Note 1)	SOIC–8	41 to 44	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 6. DC CHARACTERISTICS (V_{DD} = 3 V to 5.5 V unless otherwise noted, GND = 0 V, T_A = –40°C to +85°C) (Note 2)

Symbol	Characteristic	Min	Typ	Max	Unit
I _{DD}	Power Supply Current (unloaded CLKOUT operating at 100 MHz with 20 MHz crystal)		20		mA
V _{OH}	Output HIGH Voltage I _{OH} = –25 mA TTL High	2.4			V
V _{OL}	Output LOW Voltage I _{OL} = 25 mA			0.4	V
V _{IH}	Input HIGH Voltage, CLK only (pin 1)	(V _{DD} / 2) + 1	V _{DD} / 2		V
V _{IL}	Input LOW Voltage, CLK only (pin 1)		V _{DD} / 2	(V _{DD} / 2) – 1	V
V _{IH}	Input HIGH Voltage, S0, S1	V _{DD} – 0.5			V
V _{IL}	Input LOW Voltage, S0, S1			0.5	V
V _{IM}	Input level of S1 when open (Input Mid Point)		V _{DD} ÷ 2		V
C _{in}	Input Capacitance, S0, S1		4		pF
I _{SC}	Output Short Circuit Current		± 70		mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

2. Parameters are guaranteed by characterization and design, not tested in production.

Table 7. AC CHARACTERISTICS (V_{DD} = 3 V to 5.5 V unless otherwise noted, GND = 0 V, T_A = –40°C to +85°C) (Note 3)

Symbol	Characteristic	Min	Typ	Max	Unit
f _{Xtal}	Crystal Input Frequency	5		27	MHz
f _{CLK}	Clock Input Frequency	2		50	MHz
f _{OUT}	Output Frequency Range V _{DD} = 4.5 to 5.5 V (5.0 V ± 10%) V _{DD} = 3.0 to 3.6 V (3.3 V ± 10%)	14 14		190 120	MHz MHz
DC	Clock Output Duty Cycle at 1.5 V up to 190 MHz	45	50	55	%
t _{jitter (rms)}	Period Jitter (RMS, 1 σ)		15		ps
t _{jitter (pk-to-pk)}	Total Period Jitter, (peak–to–peak)		±40		ps
t _r /t _f	Output rise/fall time (0.8 V to 2.0 V / 2.0 V to 0.8 V)		1	2	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

3. Parameters are guaranteed by characterization and design, not tested in production.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

APPLICATIONS INFORMATION

High Frequency CMOS/TTL Oscillators

The NB3N502, along with a low frequency fundamental mode crystal, can build a high frequency CMOS/TTL output oscillator. For example, a 20 MHz crystal connected to the NB3N502 with the 5X output selected (S1 = L, S0 = H) produces a 100 MHz CMOS/TTL output clock.

External Components**Decoupling Instructions**

In order to isolate the NB3N502 from system power supply, noise de-coupling is required. The 0.01 μF decoupling capacitor has to be connected between V_{DD} and GND on pins 2 and 3. It is recommended to place de-coupling capacitors as close as possible to the NB3N502 device to minimize lead inductance. Control input pins can be connected to device pins V_{DD} or GND, or to the V_{DD} and GND planes on the board.

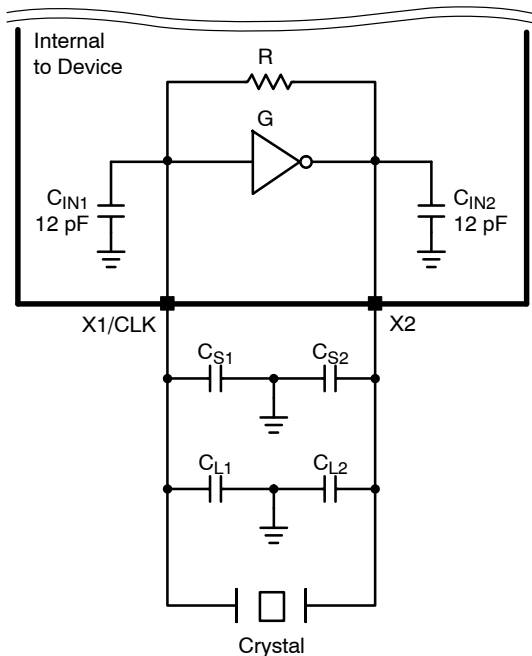
Series Termination Resistor Recommendation

A 33 Ω series terminating resistor can be used on the CLKOUT pin.

Crystal Load Capacitors Selection Guide

The total on-chip capacitance is approximately 12 pF per pin (C_{IN1} and C_{IN2}). A parallel resonant, fundamental mode crystal should be used.

The device crystal connections should include pads for small capacitors from X1/CLK to ground and from X2 to ground. These capacitors, C_{L1} and C_{L2} , are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance (C_{LOAD} (crystal)). Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal load capacitors, if needed, must be connected from each of the pins X1 and X2 to ground. The load capacitance of the crystal (C_{LOAD} (crystal)) must be matched by total load capacitance of the oscillator circuitry network, C_{INX} , C_{SX} and C_{LX} , as seen by the crystal (see Figure 3 and equations below).



$$C_{\text{LOAD1}} = C_{\text{IN1}} + C_{\text{S1}} + C_{\text{L1}} \text{ [Total capacitance on X1/CLK]}$$

$$C_{\text{LOAD2}} = C_{\text{IN2}} + C_{\text{S2}} + C_{\text{L2}} \text{ [Total capacitance on X2]}$$

$$C_{\text{IN1}} \approx C_{\text{IN2}} \approx 12 \text{ pF (Typ) [Internal capacitance]}$$

$$C_{\text{S1}} \approx C_{\text{S2}} \approx 5 \text{ pF (Typ) [External PCB stray capacitance]}$$

$$C_{\text{LOAD1,2}} = 2 \cdot C_{\text{LOAD}} \text{ (Crystal)}$$

$$C_{\text{L2}} = C_{\text{LOAD2}} - C_{\text{IN2}} - C_{\text{S2}} \text{ [External load capacitance on X2]}$$

$$C_{\text{L1}} = C_{\text{LOAD1}} - C_{\text{IN1}} - C_{\text{S1}} \text{ [External load capacitance on X1/CLK]}$$

Example 1: Equal stray capacitance on PCB

$$C_{\text{LOAD}} \text{ (Crystal)} = 18 \text{ pF (Specified by the crystal manufacturer)}$$

$$C_{\text{LOAD1}} = C_{\text{LOAD2}} = 36 \text{ pF}$$

$$C_{\text{IN1}} = C_{\text{IN2}} = 12 \text{ pF}$$

$$C_{\text{S1}} = C_{\text{S2}} = 6 \text{ pF}$$

$$C_{\text{L1}} = 36 - 12 - 6 = 18 \text{ pF}$$

$$C_{\text{L2}} = 36 - 12 - 6 = 18 \text{ pF}$$

Example 2: Different stray capacitance on PCB trace X1/CLK vs. X2

$$C_{\text{LOAD}} \text{ (Crystal)} = 18 \text{ pF}$$

$$C_{\text{LOAD1}} = C_{\text{LOAD2}} = 36 \text{ pF}$$

$$C_{\text{IN1}} = C_{\text{IN2}} = 12 \text{ pF}$$

$$C_{\text{S1}} = 4 \text{ pF} \text{ \& } C_{\text{S2}} = 8 \text{ pF}$$

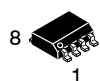
$$C_{\text{L1}} = 36 - 12 - 4 = 20 \text{ pF}$$

$$C_{\text{L2}} = 36 - 12 - 8 = 16 \text{ pF}$$

Figure 3. Using a Crystal as Reference Clock

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

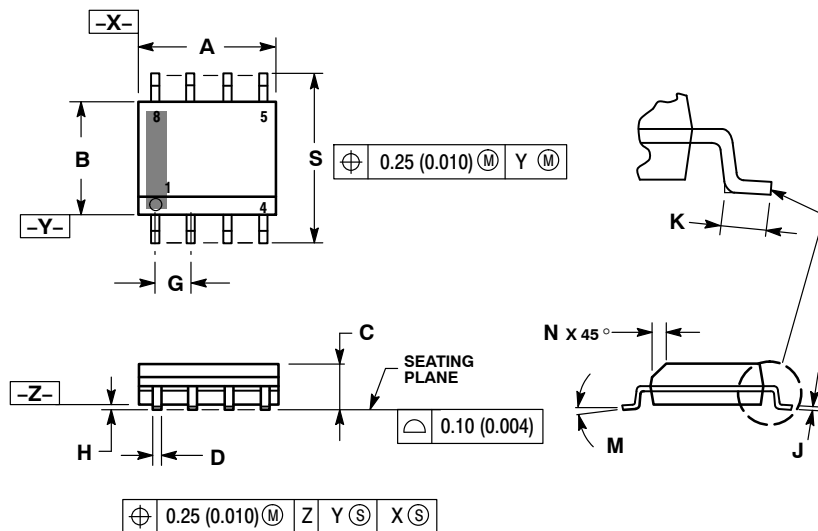
ON Semiconductor®



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

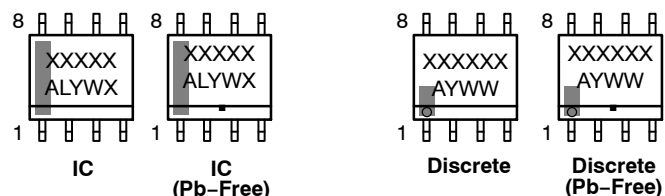
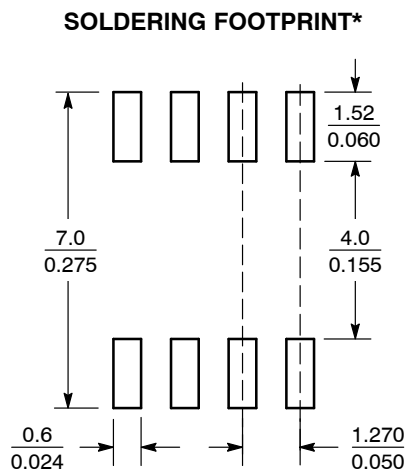


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative