FemtoClock® NG Crystal-to-3.3V, 2.5V LVPECL/LVCMOS Clock Generator with Fanout Buffer

8T49N012

DATA SHEET

General Description

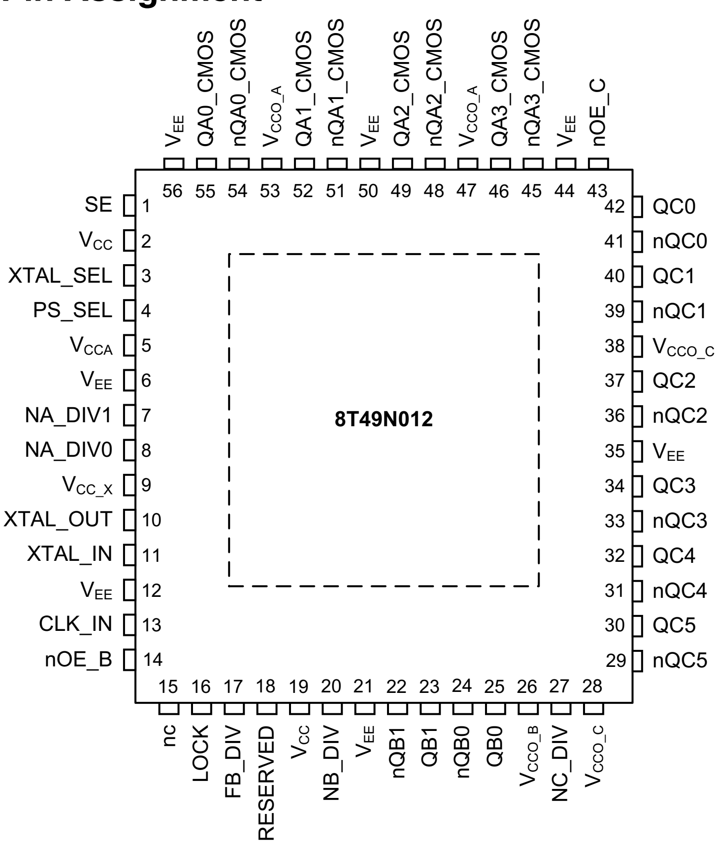
The 8T49N012 is a high performance Clock Generator with selectable LVPECL or Single-ended outputs. The 8T49N012 can generate selectable frequencies from a crystal or a single-ended reference clock. The frequency is selected from the Frequency Selection Table.

Excellent phase noise performance is maintained with IDT's Fourth Generation FemtoClock® NG PLL technology.

Features

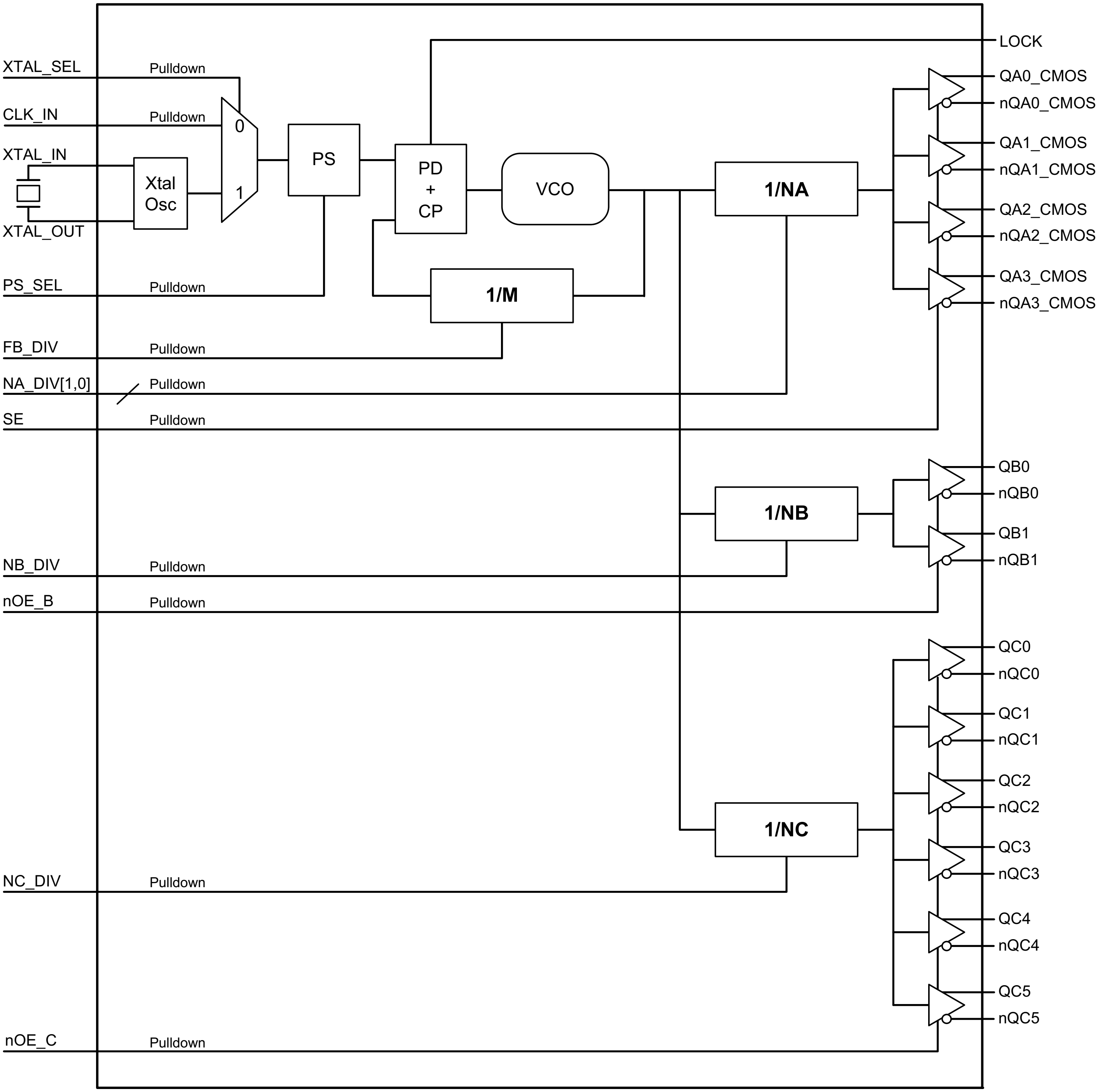
- Fourth Generation FemtoClock NG PLL technology
- Three differential output banks:
  Bank A: selectable between four pairs of LVPECL or four pairs of complementary LVCMOS/LVTTL outputs
  Bank B: two pairs of LVPECL outputs
  Bank C: six pairs of LVPECL outputs
- Selectable clock input or crystal input.
- Supports 25MHz fundamental crystal or 25MHz, 50MHz, 66.67MHz clock input
- Selectable 156.25MHz, 125MHz, 100MHz clock for Bank B and Bank C outputs
- Selectable 156.25MHz, 125MHz, 100MHz, 250MHz, 312.5MHz, 50MHz, 25MHz, 62.5MHz or 78.125MHz for Bank A outputs
- PLL lock indication (LVCMOS output)
- RMS phase jitter at 156.25MHz (12kHz - 20MHz): 0.199ps (typical)
- Power supply modes:
  Core / Output
  3.3V / 3.3V
  3.3V / 2.5V
  2.5V / 2.5V
- -40°C to 85°C ambient operating temperature
- 56-Lead VFQFN
- Lead-free (RoHS 6) packaging

Pin Assignment



56-Lead VFQFN, 8.0mm x 8.0mm x 0.9mm

Block Diagram



Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions[1]

Number	Name	Type		Description
1	SE	Input	Pulldown	Select pin for Bank A outputs. LVCMOS/LVTTL interface levels. See the *Function Configuration Tables* section.
2	V_{CC}	Power		Core power supply pins.
3	XTAL_SEL	Input	Pulldown	Select reference source between the crystal or input clock. LVCMOS/ LVTTL interface levels. See the *Function Configuration Tables* section.
4	PS_SEL	Input	Pulldown	Pre scale divider selection. LVCMOS/LVTTL interface levels. See the *Function Configuration Tables* section.
5	V_{CCA}	Power		Analog supply for VCO.
6	V_{EE}	Power		Negative power supply pin.
7	NA_DIV1	Input	Pulldown	Select output frequency for Bank A outputs. LVCMOS/LVTTL interface levels. See the *Function Configuration Tables* section.
8	NA_DIV0	Input	Pulldown	Select output frequency for Bank A outputs. LVCMOS/LVTTL interface levels. See the *Function Configuration Tables* section.
9	V_{CC_X}	Power		Crystal oscillator power supply pin.
10	XTAL_OUT	O/I		Crystal oscillator interface output.
11	XTAL_IN	O/I		Crystal oscillator interface input.
12	V_{EE}	Power		Negative power supply pin.
13	CLK_IN	Input	Pulldown	Single-ended input clock. LVCMOS/LVTTL interface levels.
14	nOE_B	Input	Pulldown	Output enable for Bank B outputs. LVCMOS/LVTTL interface levels. See the *Function Configuration Tables* section.
15	nc	unused		No connect pin.
16	LOCK	Output		PLL lock indicator. Logic High indicates PLL is locked. LVCMOS/LVTTL interface levels. See the *Function Configuration Tables* section.
17	FB_DIV	Input	Pulldown	Feedback divider selection. LVCMOS/LVTTL interface levels. See the *Function Configuration Tables* section.
18	RESERVED	Reserve		Reserve pin. Do not connect.
19	V_{CC}	Power		Core power supply pin.
20	NB_DIV	Input	Pulldown	Select output frequency for Bank B outputs. LVCMOS/LVTTL interface levels. See the *Function Configuration Tables* section.
21	V_{EE}	Power		Negative power supply pin.
22	nQB1	Output		Differential Bank B outputs. LVPECL interface levels.
23	QB1	Output		
24	nQB0	Output		Differential Bank B outputs. LVPECL interface levels.
25	QB0	Output		
26	V_{CCO_B}	Power		Bank B output power supply pin.
27	NC_DIV	Input	Pulldown	Select output frequency for Bank C outputs. LVCMOS/LVTTL interface levels. See the *Function Configuration Tables* section.
28	V_{CCO_C}	Power		Bank C output power supply pin.
29	nQC5	Output		Differential Bank C outputs. LVPECL interface levels.
30	QC5	Output		

Table 1. Pin Descriptions[1] (Continued)

Number	Name	Type		Description
31	nQC4	Output		Differential Bank C outputs. LVPECL interface levels.
32	QC4	Output		
33	nQC3	Output		Differential Bank C outputs. LVPECL interface levels.
34	QC3	Output		
35	V_{EE}	Power		Negative power supply pin.
36	nQC2	Output		Differential Bank C outputs. LVPECL interface levels.
37	QC2	Output		
38	V_{CCO_C}	Power		Bank C output power supply pin.
39	nQC1	Output		Differential Bank C outputs. LVPECL interface levels.
40	QC1	Output		
41	nQC0	Output		Differential Bank C outputs. LVPECL interface levels.
42	QC0	Output		
43	nOE_C	Input	Pulldown	Output enable for Bank C outputs. LVCMOS/LVTTL interface levels. See the *Function Configuration Tables* section.
44	V_{EE}	Power		Negative power supply pin.
45	nQA3_CMOS	Output		Selectable LVPECL differential or complementary LVCMOS/LVTTL Bank A outputs.
46	QA3_CMOS	Output		
47	V_{CCO_A}	Power		Bank A output power supply pin.
48	nQA2_CMOS	Output		Selectable LVPECL differential or complementary LVCMOS/LVTTL Bank A outputs.
49	QA2_CMOS	Output		
50	V_{EE}	Power		Negative power supply pin.
51	nQA1_CMOS	Output		Selectable LVPECL differential or complementary LVCMOS/LVTTL Bank A outputs.
52	QA1_CMOS	Output		
53	V_{CCO_A}	Power		Bank A output power supply pin.
54	nQA0_CMOS	Output		Selectable LVPECL differential or complementary LVCMOS/LVTTL Bank A outputs.
55	QA0_CMOS	Output		
56	V_{EE}	Power		Negative power supply pin.
E-Pad	V_{EE}	Power		Negative power supply pin.

NOTE 1: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance		Input Control Pins		3.5		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)		V_{CC}, V_{CC_X}, V_{CCO_A} = 3.465V		6.5		pF
			V_{CC}, V_{CC_X} = 3.465V, V_{CCO_A} = 2.625V		6.5		pF
Rout	LVCMOS Output Impedance	QA[0:3]_CMOS, nQA[0:3]_CMOS	V_{CCO_A} = 3.3V ± 5%		26		Ω
			V_{CCO_A} = 2.5V ± 5%		30		Ω

Function Configuration Tables

Table 3A. FB_DIV Function Table

FB_DIV	Feedback Divider
Low (default)	50
Mid	75
High	100

Table 3B. SE Function Table

SE	Bank A Output
Low (default)	Differential output
Mid	High Impedance
High	LVCMOS output

Table 3C. XTAL_SEL Function Table

XTAL_SEL	Bank A Output
Low (default)	CLK_IN
High	XTAL

Table 3D. LOCK indicaiotn Table

LOCK	PLL Status
Low	PLL is Out of Lock
High	PLL is Locked

Table 3E. nQE_B Function Table

nOE_B	Bank B Output
Low (default)	LVPECL
Mid (Reserved)	Reserved
High	High Impedance

Table 3F. nOE_C Function Table

nOE_C	Bank C Output
Low (default)	LVPECL
Mid (Reserved)	Reserved
High	High Impedance

Table 3G. Bank B and C Output Divider Table

Input Frequency (MHz)	PS_SEL	FB_DIV	NB_DIV	Bank B Frequency (MHz)	NC_DIV	Bank C Frequency (MHz)
25	Low (default)	Low (default)	Low (default)	125	Low (default)	125
			Mid	100	Mid	100
			High	156.25	High	156.25
66.66667	Mid	Mid	Low (default)	125	Low (default)	125
			Mid	100	Mid	100
			High	156.25	High	156.25
50	High	Low	Low (default)	125	Low (default)	125
			Mid	100	Mid	100
			High	156.25	High	156.25

Table 3H. Bank A Output Divider table

Input Frequency (MHz)	PS_SEL	FB_DIV	NA_DIV [1:0]	Bank A Frequency (MHz)
25	Low (default)	Low (default)	Low, Low (default)	125
			Low, High	156.25
			High, Low	312.5
			High, High	100
			Low, Mid	25
			High, Mid	50
			Mid, Low	250
			Mid, High	62.5
			Mid, Mid	78.125
66.66667	Mid	Mid	Low, Low (default)	125
			Low, High	156.25
			High, Low	312.5
			High, High	100
			Low, Mid	25
			High, Mid	50
			Mid, Low	250
			Mid, High	62.5
			Mid, Mid	78.125
50	High	Low	Low, Low (default)	125
			Low, High	156.25
			High, Low	312.5
			High, High	100
			Low, Mid	25
			High, Mid	50
			Mid, Low	250
			Mid, High	62.5
			Mid, Mid	78.125

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.6V
Inputs, V_I XTAL_IN Other Input	 0V to 2V -0.5V to V_{CC} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{CCO_A} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Thermal Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CC\_X} = V_{CCO\_X}$[1] = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CC_X}	XTAL Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO_X}	Output Supply Voltage		3.135	3.3	3.465	V
I_{CCA}	Analog Supply Current			42	50	mA
I_{EE}	Power Supply Current	Unterminated Outputs		332	381	mA

NOTE 1: V_{CCO_X} denotes V_{CCO_A}, V_{CCO_B} and V_{CCO_C},

Table 4B. Power Supply DC Characteristics, $V_{CC} = V_{CC\_X} = V_{CCO\_X}$[1] = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CC_X}	XTAL Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{CCO_X}	Output Supply Voltage		2.375	2.5	2.625	V
I_{CCA}	Analog Supply Current			32	41	mA
I_{EE}	Power Supply Current	Unterminated Outputs		306	354	mA

NOTE 1: V_{CCO_X} denotes V_{CCO_A}, V_{CCO_B} and V_{CCO_C},

Table 4C. Power Supply DC Characteristics, $V_{CC} = V_{CC\_X} = 3.3V \pm 5\%$, V_{CCO_X}[1] $= 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CC_X}	XTAL Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO_X}	Output Supply Voltage		2.375	2.5	2.625	V
I_{CCA}	Analog Supply Current			42	50	mA
I_{EE}	Power Supply Current	Unterminated Outputs		323	373	mA

NOTE 1: V_{CCO_X} denotes V_{CCO_A}, V_{CCO_B} and V_{CCO_C},

Table 4D. 2-Level LVCMOS/LVTTL DC Characteristics, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$V_{CC} = 3.3V$	2		$V_{CC} + 0.3$	V
			$V_{CC} = 2.5V$	1.7		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{CC} = 3.3V$	-0.3		0.8	V
			$V_{CC} = 2.5V$	-0.3		0.7	V
I_{IH}	Input High Current	CLK_IN, XTAL_SEL	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	µA
I_{IL}	Input Low Current	CLK_IN, XTAL_SEL	$V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage	QA[0:3]_CMOS, nQA[0:3]_CMOS, LOCK	$V_{CCO\_A} = 3.465V$; $I_{OH} = -8mA$	2.6			V
V_{OL}	Output Low Voltage	QA[0:3]_CMOS, nQA[0:3]_CMOS, LOCK	$V_{CCO\_A} = 3.465V$; $I_{OL} = 8mA$			0.6	V

Table 4E. 3-Level LVCMOS/LVTTL DC Characteristics, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			0.85 * V_{CC}			V
V_{IL}	Input Low Voltage					0.15 * V_{CC}	V
V_{IM}	Input middle Voltage			0.45 * V_{CC}		0.55 * V_{CC}	V
I_{IH}	Input High Current	nOE_B, nOE_C, NA_DIVx, NB_DIV, NC_DIV, PS_SEL, SE	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	µA
I_{IL}	Input Low Current	nOE_B, nOE_C, NA_DIVx, NB_DIV, NC_DIV, PS_SEL, SE	$V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
I_{IM}	Input Middle Current	nOE_B, nOE_C, NA_DIVx, NB_DIV, NC_DIV, PS_SEL, SE	$V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0.5*V_{CC}$			150	µA

Table 4F. LVPECL DC Characteristics, $V_{CCO\_X}{}^{1}$ = 3.3V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[2]		V_{CCO_X} – 1.1		V_{CCO_X} – 0.7	V
V_{OL}	Output Low Voltage[2]		V_{CCO_X} – 2.0		V_{CCO_X} – 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: V_{CCO_X} denotes V_{CCO_A}, V_{CCO_B} and V_{CCO_C},

NOTE 2: Outputs termination with 50Ω to V_{CCO_X} – 2V.

Table 4G. LVPECL DC Characteristics, $V_{CCO\_X}{}^{1}$ = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[2]		V_{CCO_X} – 1.1		V_{CCO_X} – 0.7	V
V_{OL}	Output Low Voltage[2]		V_{CCO_X} – 2.0		V_{CCO_X} – 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: V_{CCO_X} denotes V_{CCO_A}, V_{CCO_B} and V_{CCO_C},

NOTE 2: Outputs termination with 50Ω to V_{CCO_X} – 2V.

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Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Load Capacitance (C_L)			12	18	pF

AC Electrical Characteristics

Table 6. AC Characteristics, $V_{CC} = V_{CC\_X} = V_{CCO\_X}$[1] = 3.3V ± 5% or 2.5V ± 5%, or $V_{CC} = V_{CC\_X}$ = 3.3V ± 5%, V_{CCO_X}[1] = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency		CLK_IN or XTAL		25		MHz
			CLK_IN		50		MHz
			CLK_IN		66.67		MHz
f_{VCO}	VCO Frequency				2500		MHz
tjit(Ø)	LVPECL RMS Phase Jitter, Random[2]		100MHz, Integration Range: 12kHz – 20MHz		320	415	fs
			125MHz, Integration Range: 12kHz – 20MHz		210	270	fs
			125MHz, Integration Range: 10kHz – 1MHz		163	220	fs
			156.25MHz, Integration Range: 12kHz – 20MHz		199	260	fs
			156.25MHz, Integration Range: 10KHz – 1MHz		165	225	fs
			25MHz, Integration Range: 12kHz – 5MHz		245	415	fs
tjit(Ø)	LVCMOS RMS Phase Jitter, Random[2]		125MHz, Integration Range: 12kHz – 20MHz		210	280	fs
			156.25MHz, Integration Range: 12kHz – 20MHz		204	265	fs
			100MHz, Integration Range: 12kHz – 20MHz		312	385	fs
tsk(o)	Output Skew; NOTE[3, 4]	LVPECL Outputs	Same Bank Outputs			51	ps
t_R / t_F	Output Rise/Fall Time	LVPECL Outputs	20% - 80%			500	ps
		LVCMOS Outputs	20% - 80%			700	ps
odc	Output Duty Cycle	LVPECL Outputs		45	50	55	%
		LVCMOS Outputs		45	50	55	%

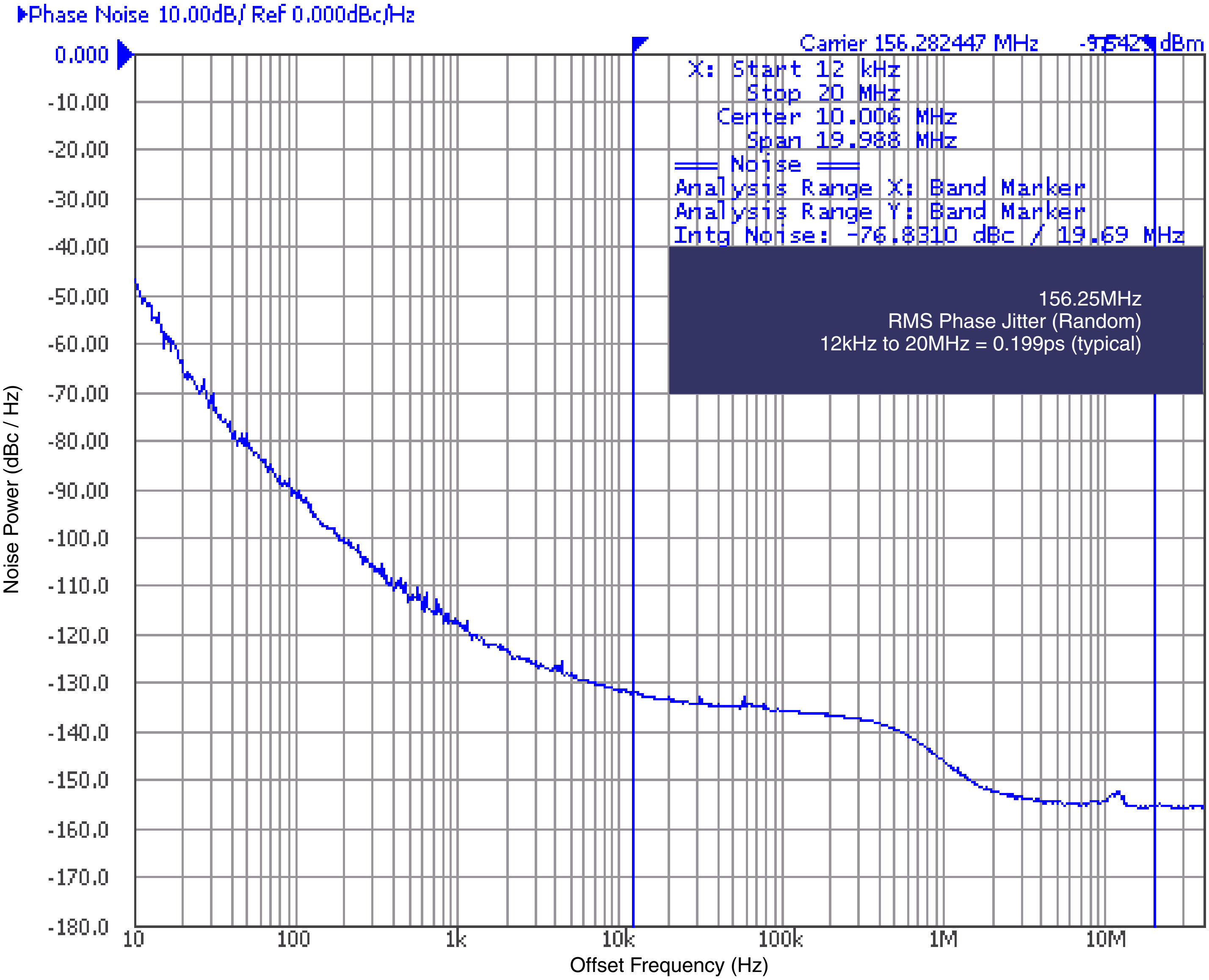
NOTE 1: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2: Characterized using XTAL input.

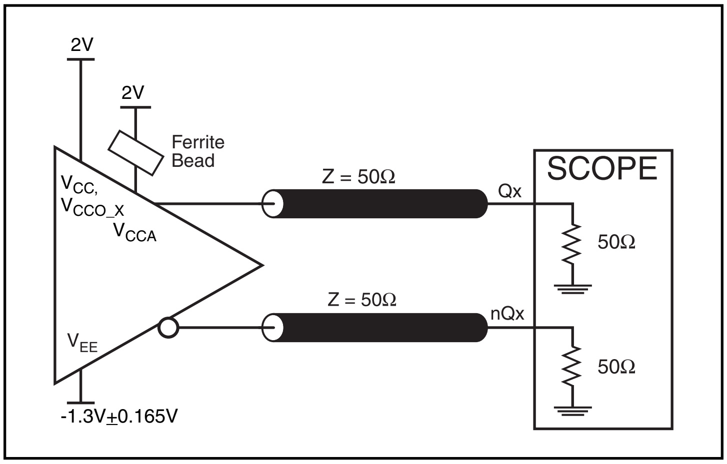
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.

NOTE 4: These parameters are guaranteed by characterization.

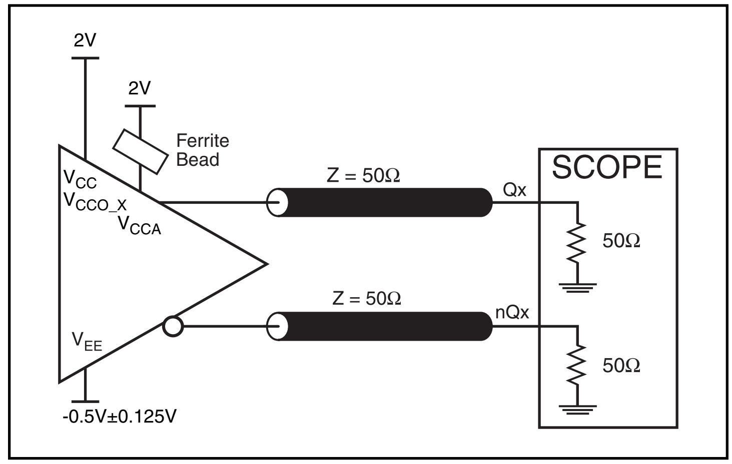
Typical Phase Noise at 156.25MHz



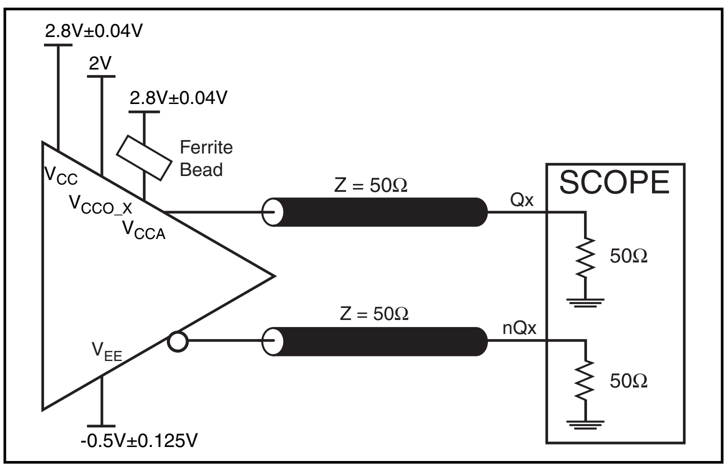
Parameter Measurement Information



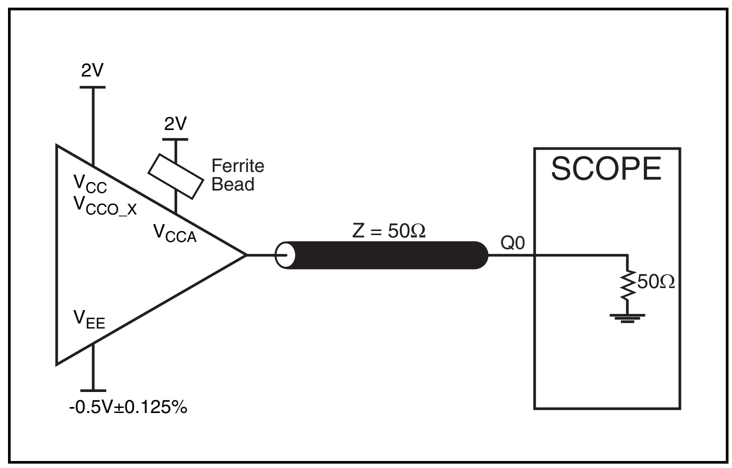
3.3V Core/3.3V QAx_CMOS LVPECL Output Load Test Circuit



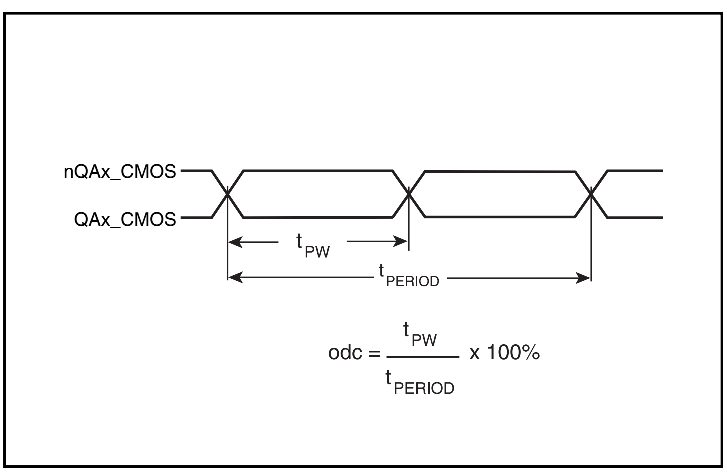
2.5V Core/2.5V QAx_CMOS LVPECL Output Load Test Circuit



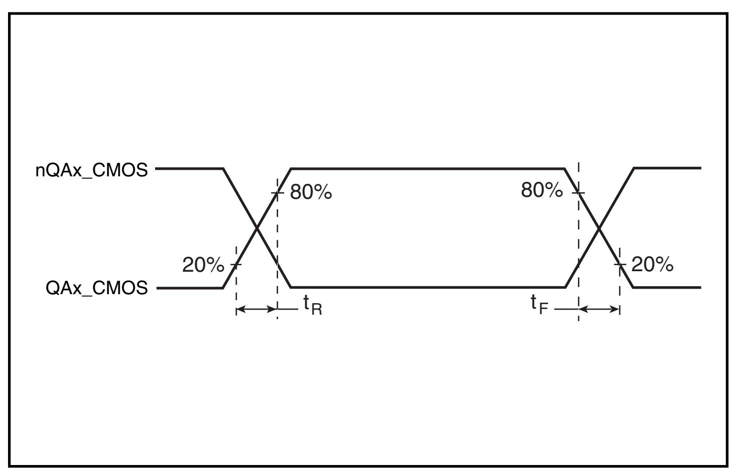
3.3V Core/2.5V QAx_CMOS LVPECL Output Load Test Circuit



2.5V/2.5V QAx_CMOS Output Load Test Circuit

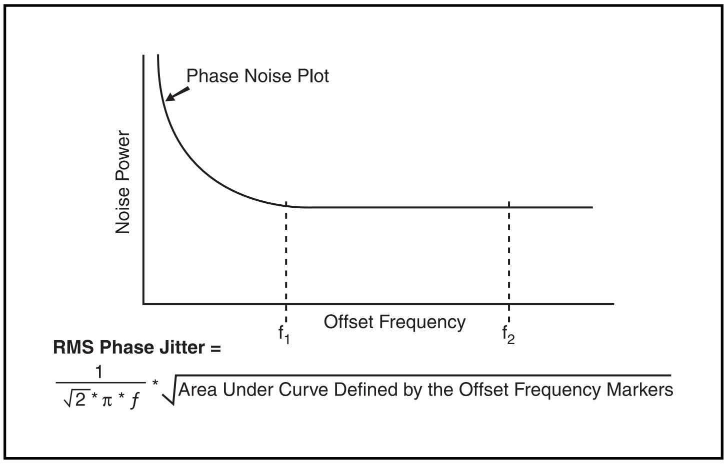


LVCMOS Output Duty Cycle/Pulse Width/Period

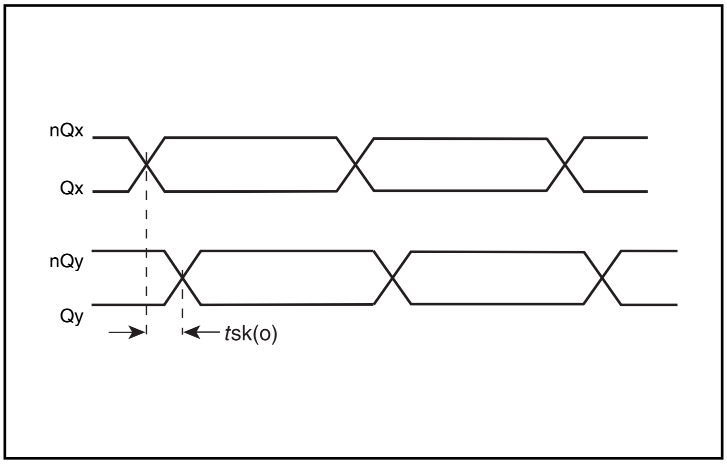


Output Rise/Fall Time

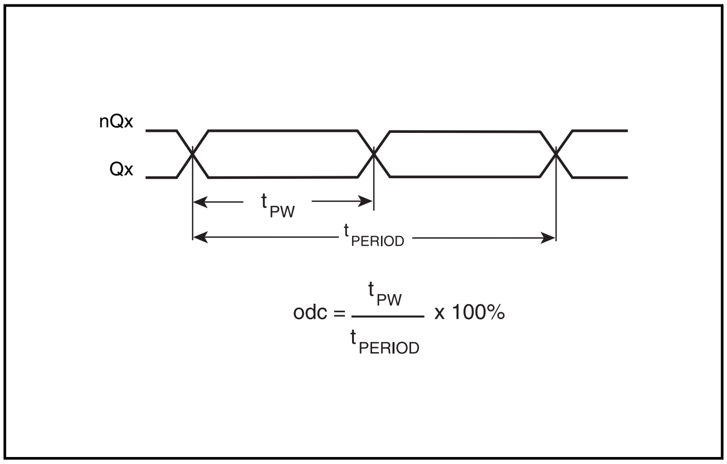
Parameter Measurement Information, continued



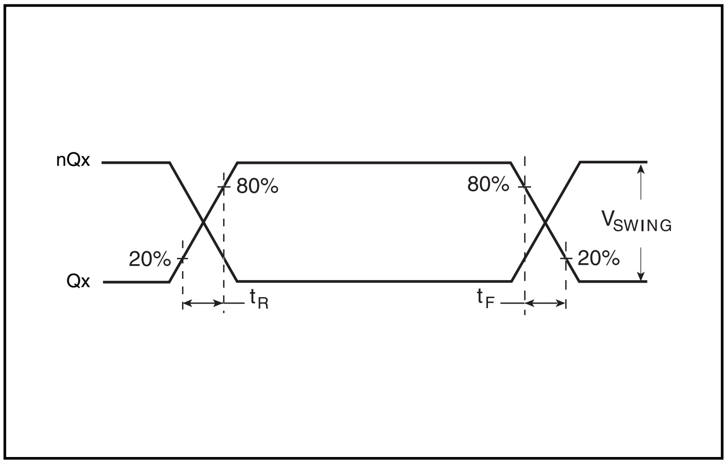
RMS Phase Jitter



Output Skew



Differential Output Duty Cycle



LVPECL Output Rise/Fall Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pullup or pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVCMOS Outputs

All unused LVCMOS outputs can be left floating. There should be no trace attached.

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 1*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

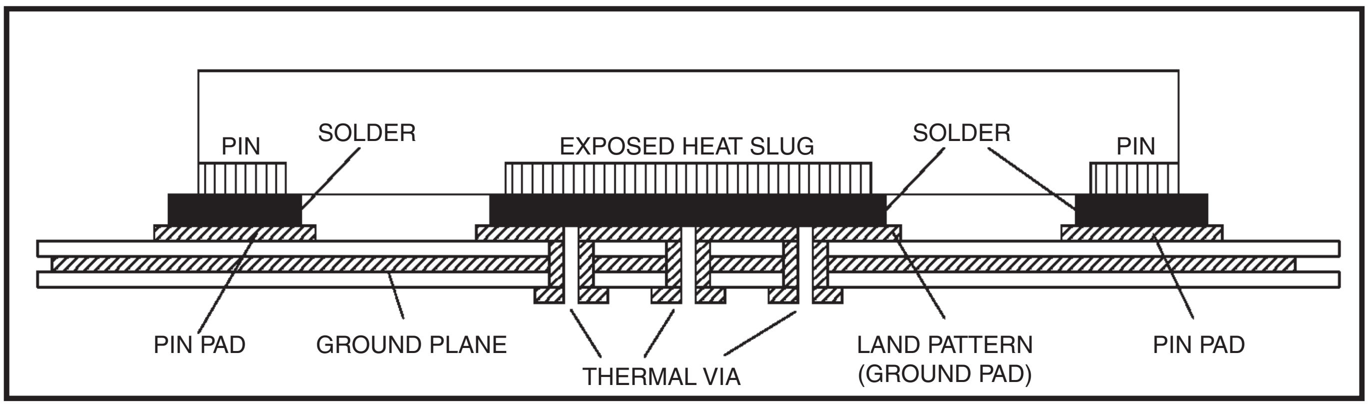


Figure 1. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 2A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 2B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

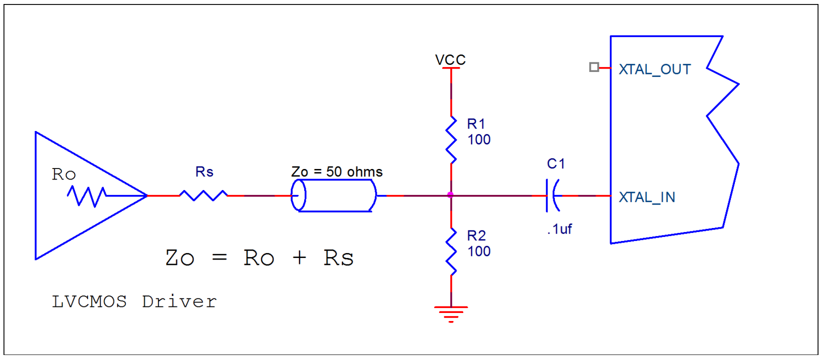


Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

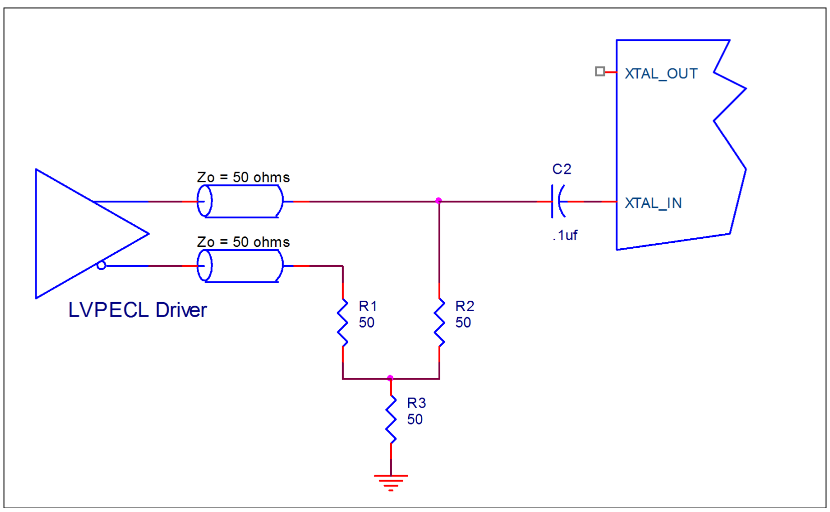


Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figure 3A* shows a layout that is recommended only as a guideline. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

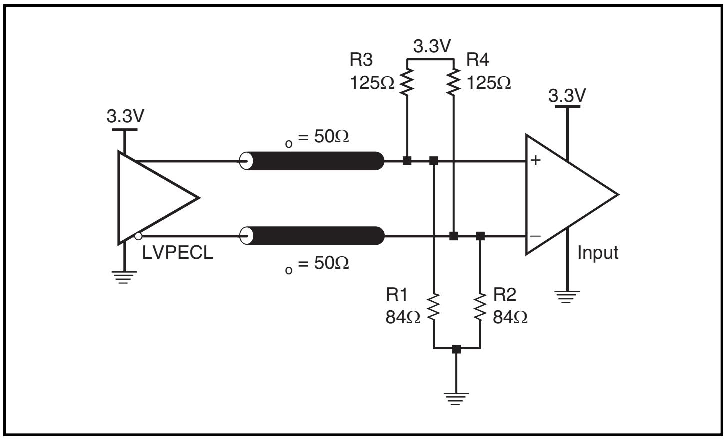


Figure 3A. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in *Figure 4B* can be eliminated and the termination is shown in *Figure 4C.*

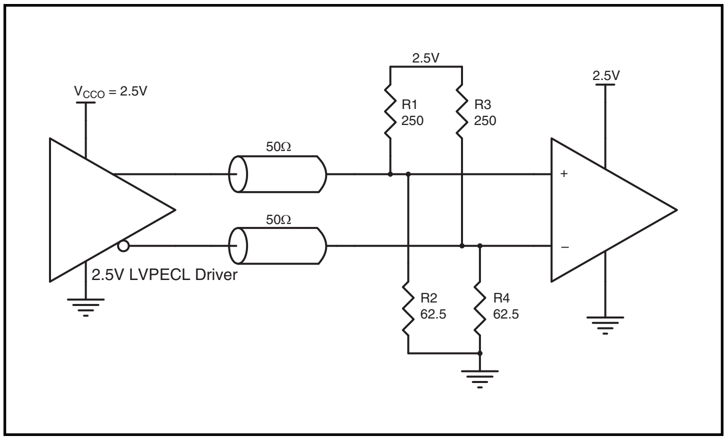


Figure 4A. 2.5V LVPECL Driver Termination Example

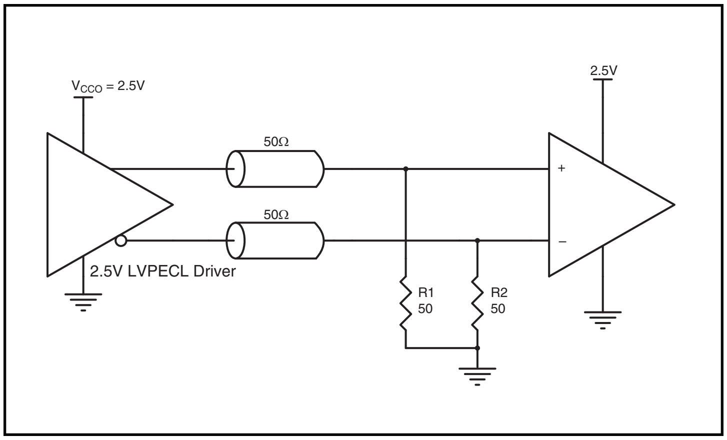


Figure 4C. 2.5V LVPECL Driver Termination Example

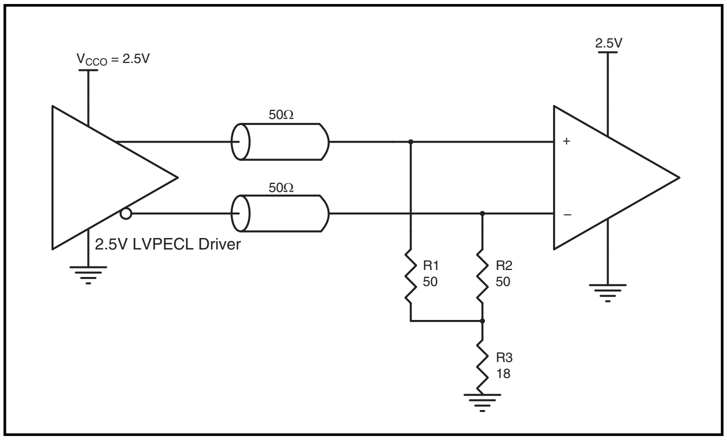


Figure 4B. 2.5V LVPECL Driver Termination Example

Schematic Example

Figure 5 (next page) is an 8T49N012 application example schematic. The schematic focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

In this example the device is operated at all V_{CC} power pins = 3.3V. The Bank A outputs are configured for LVCMOS by pulling SE high. Three different examples of LVPECL terminations are shown for the outputs to demonstrate less common termination options.

Crystal layout is very important to minimize capacitive coupling between the crystal pads and leads and other metal in the circuit board. Capacitive coupling to other conductors has two adverse effects. The first is that it reduces the oscillator frequency, leaving less tuning margin. Second, noise on power planes and logic transitions on signal traces can pull the phase of voltages on the XTAL_IN and XTAL_OUT pins of the oscillator.

Using a crystal on the top layer as an example, void all signal and power layers under the crystal, XTAL_IN, XTAL_OUT and the input pins of the 8T49N012 between the top layer and the ground plane for the 8T49N012. If the ground plane for the 8T49N012 is the first layer under the crystal and the parasitic capacity of the traces and pads is excessive, then void enough power and signal planes to minimize the coupling capacity to the first ground plane. Ensure that the ground under the crystal is the same ground as used for the tuning caps and the oscillator.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8T49N012 provides separate power supply pins to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. The 0.1µF capacitors in each power pin filter must be placed on the device side. If space is limited, the other components can be on the opposite side of the PCB. Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices.

The V_{CC} and V_{CCO} LC filters start to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

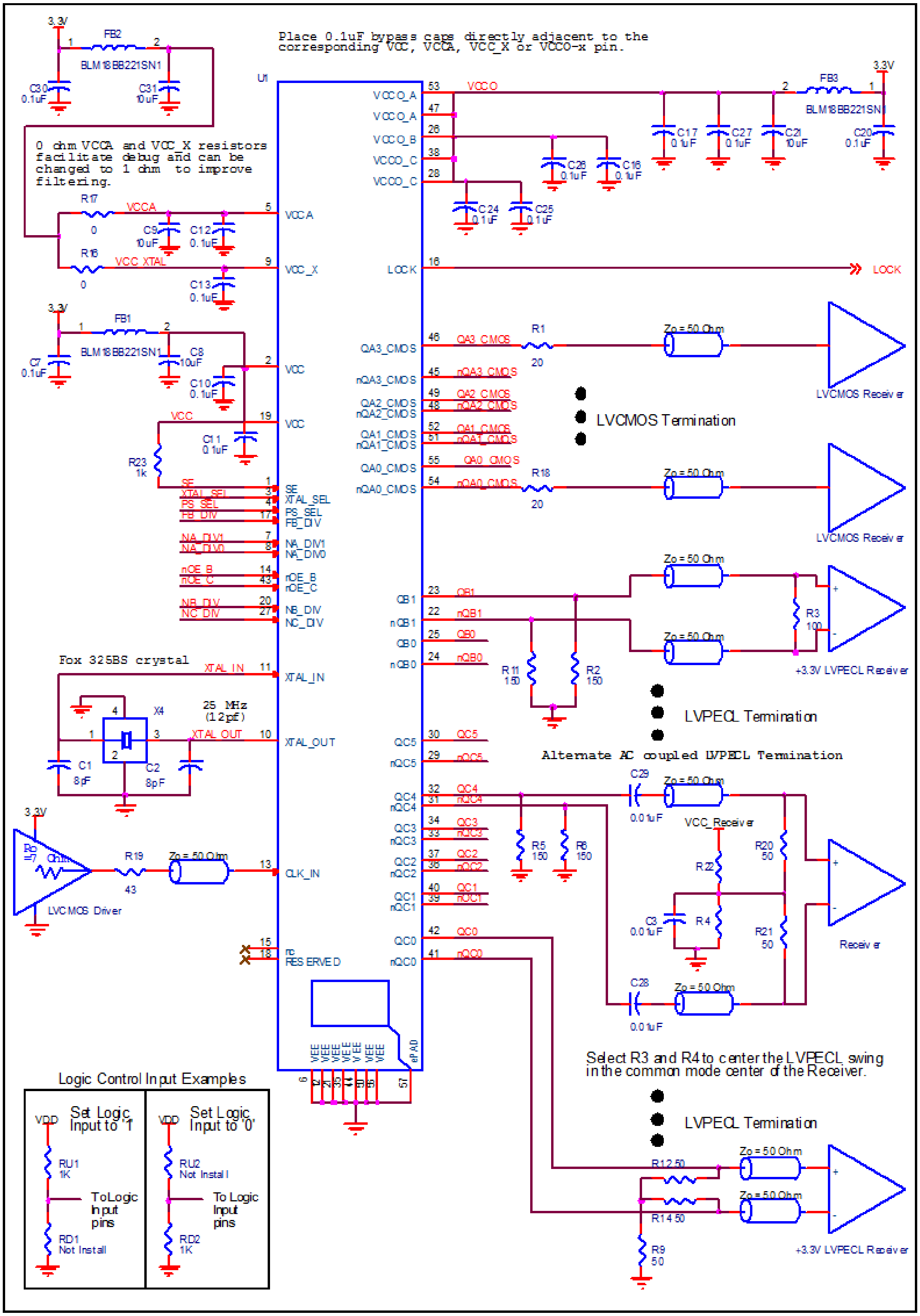


Figure 5. 8T49N012 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8T49N012I. Equations and example calculations are also provided.

1. Power Dissipation

The total power dissipation for the8T49N012 is the sum of the core power plus the output power dissipated due to the loading.
The following is the power dissipation for V_{CC}= 3.3V + 5% = 3.465V, which gives worst case results.

I_{EE} = 344mA with QA Bank in LVCMOS mode is the worst case scenario.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE} = 3.465V * 0.345A = **1.195W**
- Power (LVPECL)$_{MAX}$ = **31mW** per output
- Total Power (LVPECL)$_{MAX}$ = 31mW * 8 = **0.248W**

LVCMOS Dynamic Power Dissipation

- Dynamic Power at 312.5MHz:
  P = C_{PD} * Freq * $(V_{DDO})^2$ = 6.5pF * 312.5MHz * $(3.465V)^2$
  P = 0.024W per output
  Total Power (CPD) = 0.024W * 8 = 0.195W

Total Power Dissipation

- **Total Power**
  = Power (core) + Total Power (LVPECL) + Total Power (CPD)
  = 1.195W + 0.248W+ 0.195W
  = **1.638W**

2. Junction Temperature

Junction temperature, T_J, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_J, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $T_J = \theta_{JA}$ * Pd_total + T_A

T_J = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 23.1 per *Table 7* below.

°C/W per Table 6 below.

Therefore, T_J for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.638W * 23.1°C/W = 122.8°C. This is below the limit of 125°C.

This calculation is only an example. T_J will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 56-Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	23.1°C/W	20.2°C/W	18.6°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

The LVPECL output driver circuit and termination are shown in *Figure 6*.

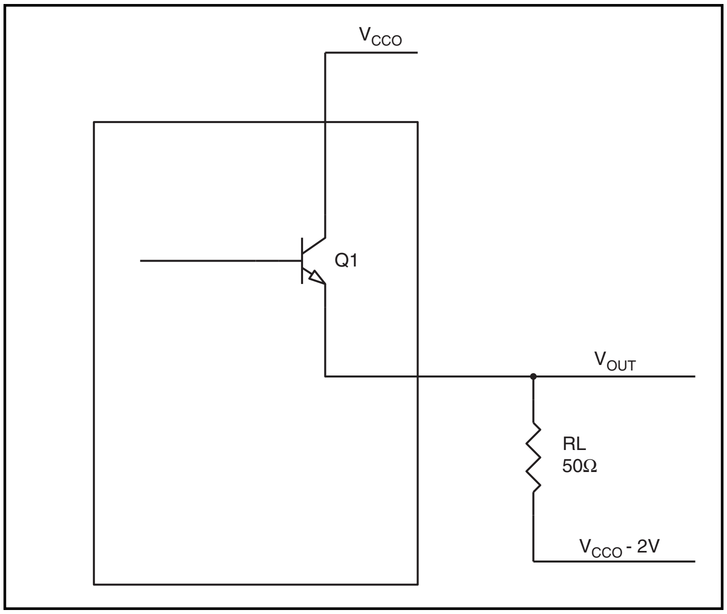


Figure 6. LVPECL Driver Circuit and Termination

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 0.7V}$
  $(V_{CCO\_MAX} – V_{OH\_MAX})$ = **0.7V**
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} – 1.6V}$
  $(V_{CCO\_MAX} – V_{OL\_MAX})$ = **1.6V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.7V)/50\Omega] * 0.7V =$ **18.2mW**

$Pd\_L = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) =$
$[(2V– 1.6V)/50\Omega] * 1.6V =$ **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **31.00mW**

Reliability Information

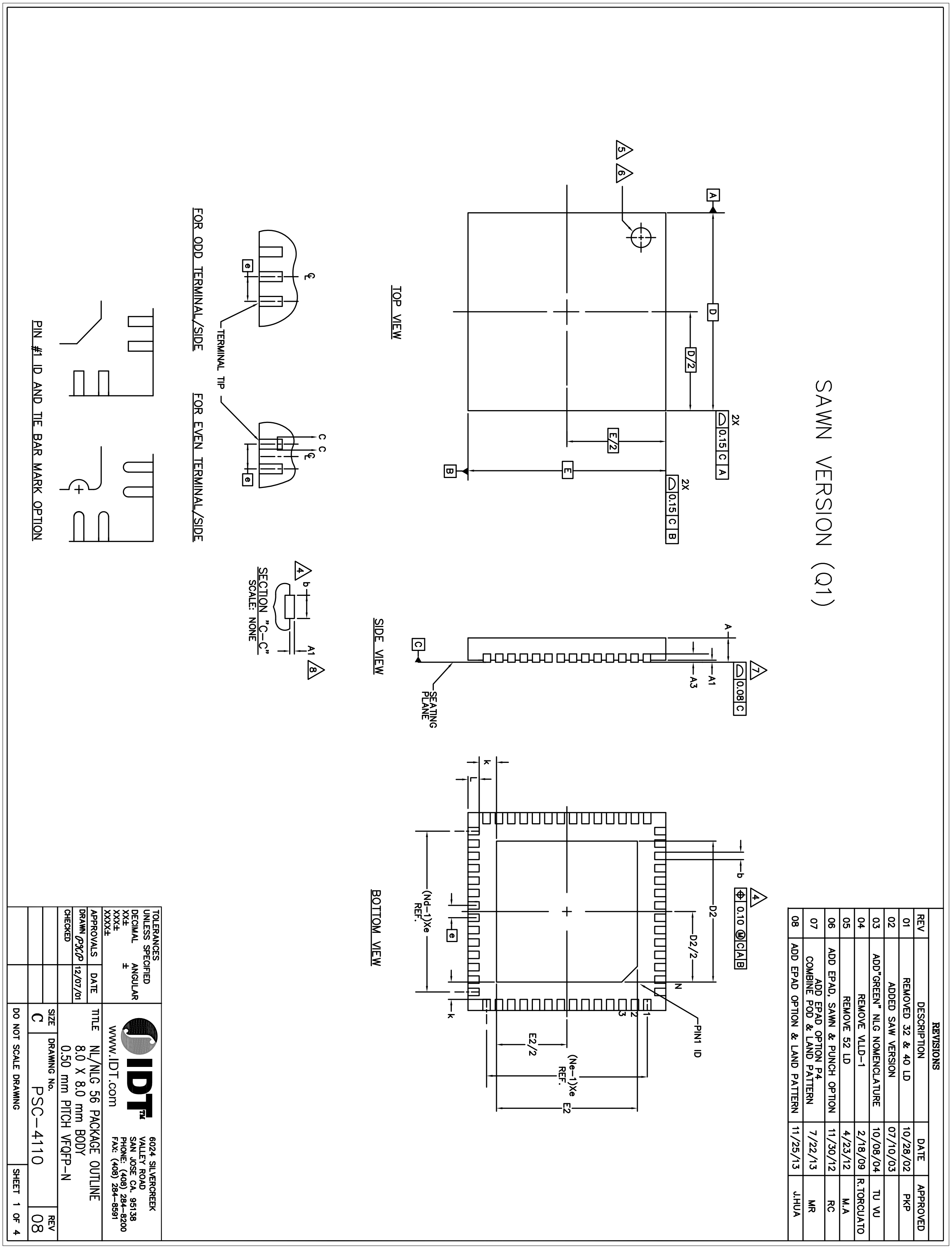
Table 8. θ_{JA} vs. Air Flow Table for a 56-Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	23.1°C/W	20.2°C/W	18.6°C/W

Transistor Count

The transistor count for 8T49N012 is 176,638

56-Lead VFQFN Package Outline and Package Dimension



56-Lead VFQFN Package Outline and Package Dimensions, continued

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
01	REMOVED 32 & 40 LD	10/28/02	PKP
02	ADDED SAW VERSION	07/10/03	
03	ADD "GREEN" NLG NOMENCLATURE	10/08/04	TU VU
04	REMOVE VLLD-1	3/18/09	R.TORQUATO
05	REMOVE 32 LD	4/23/12	M.A
06	ADD EPAD, SAWN & PUNCH OPTION	11/30/12	RC
07	ADD EPAD OPTION P4 COMBINE POD & LAND PATTERN	7/22/13	MR
08	ADD EPAD OPTION & LAND PATTERN	11/25/13	J.HUA

EPAD OPTION

SYMBOL	P2		
	MIN	NOM	MAX
E2	6.45	6.60	6.75
D2	6.45	6.60	6.75

COMMON DIMENSION

SYMBOL	DIMENSION			NOTE
	MIN.	NOM.	MAX.	
e	0.50 BSC			
N	56			2
Nd	14			2
Ne	14			2
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	4
D2	SEE EPAD OPTION			
E2	SEE EPAD OPTION			
A	0.80	0.9	1.00	
A1	0.00	0.02	0.05	
A3	0.20 REF.			
D	8.00 BSC			
E	8.00 BSC			
θ	–	–	12°	
k	0.20	–	–	

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. APPLIED TO EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY FOR TERMINALS.
9. NOT AN ACTUAL IO.

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

APPROVALS	DATE
DRAWN PSCP	12/07/01
CHECKED	

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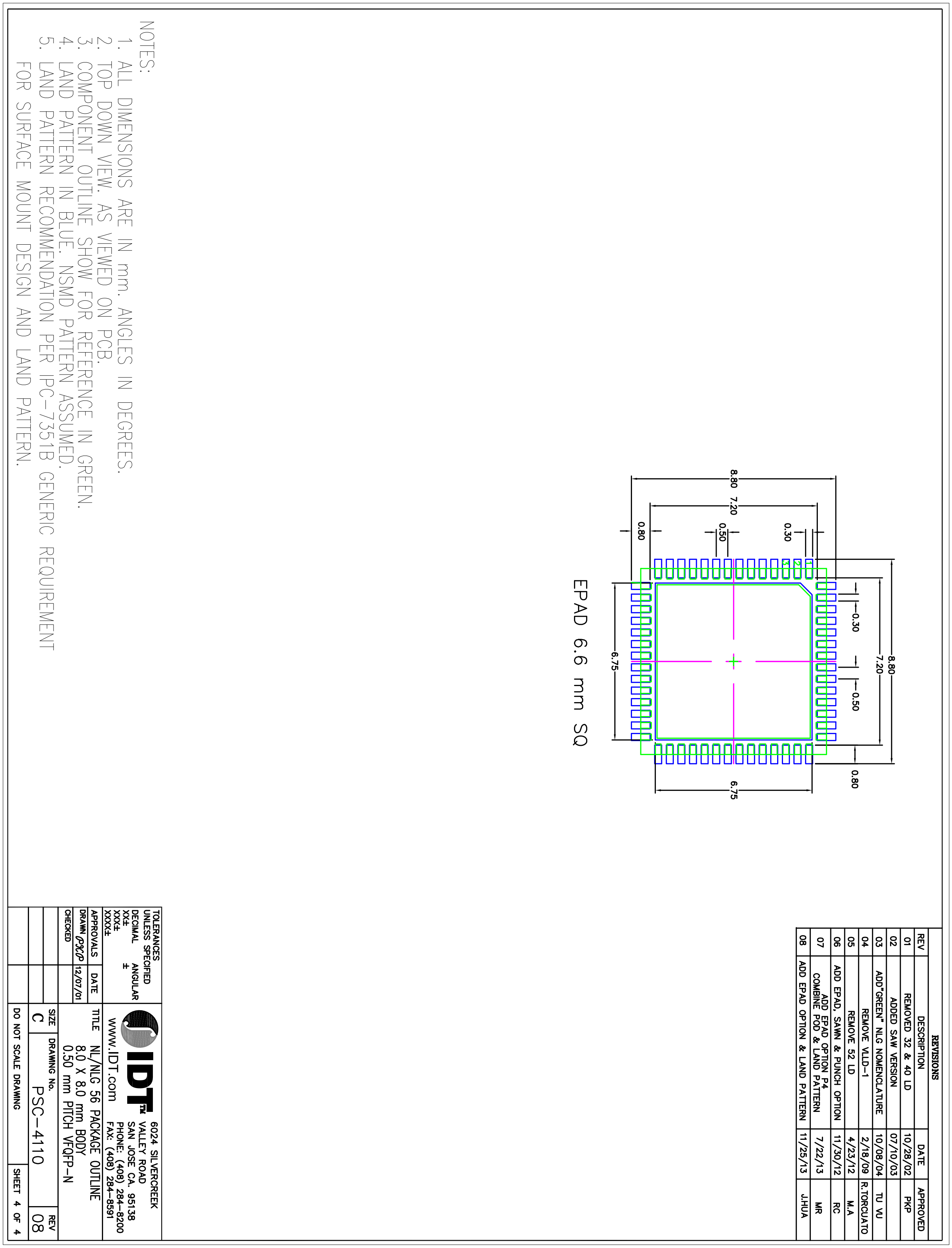
6024 SILVERCREEK VALLEY ROAD
SAN JOSE CA. 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

TITLE NL/NLG 56 PACKAGE OUTLINE
8.0 X 8.0 mm BODY
0.50 mm PITCH VFQFP–N

SIZE C DRAWING No. PSC–4110 REV 08

DO NOT SCALE DRAWING SHEET 3 OF 4

56-Lead VFQFN Package Outline and Package Dimensions, continued



Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49N012NLGI	IDT8T49N012NLGI	“Lead-Free” 56-Lead VFQFN	Tray	-40°C to 85°C
8T49N012NLGI8	IDT8T49N012NLGI	“Lead-Free” 56-Lead VFQFN	Tape & Reel	-40°C to 85°C

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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