National Semiconductor

DS8908B AM/FM Digital Phase-Locked Loop Frequency Synthesizer

General Description

The DS8908B is a PLL synthesizer designed specifically for use in AM/FM radios. It contains the reference oscillator, a phase comparator, a charge pump, an operational amplifier, a 120 MHz ECL/I^2L dual modulus programmable divider, and a 19-bit shift register/latch for serial data entry. The device is designed to operate with a serial data controller generating the necesary division codes for each frequency, and logic state information for radio function inputs/outputs.

A 3.96 MHz pierce oscillator and divider chain generate a 1.98 MHz external controller clock, a 20 kHz, 10 kHz, 9 kHz, and a 1 kHz reference signals, and a 50 Hz time-of-day signal. The oscillator and divider chain are sourced by the V_{CCM} pin thus providing a low power controller clock drive and time-of-day indication when the balance of the PLL is powered down.

The 21-bit serial data steram is transferred between the frequency synthesizer and the controller via a 3-wire bus system comprised of a data line, a clock line, and an enable line.

The first 2 bits in the serial data stream address the synthesizer thus permitting other devices such as display drivers to share the same bus. The next 14 bits are used for the PLL(N + 1) divide code. The 15th bit is used internally to select the AM or FM local oscillator input. A high level on this bit enables the FM input and a low level enables the AM input. The 16th and 17th bits are used to select one of the 4 reference frequencies. The 18th and 19th bits are connected via latches to open collector outputs. These outputs can be used to drive radio functions such as gain, mute, AM, FM, or charge pump current source levels.

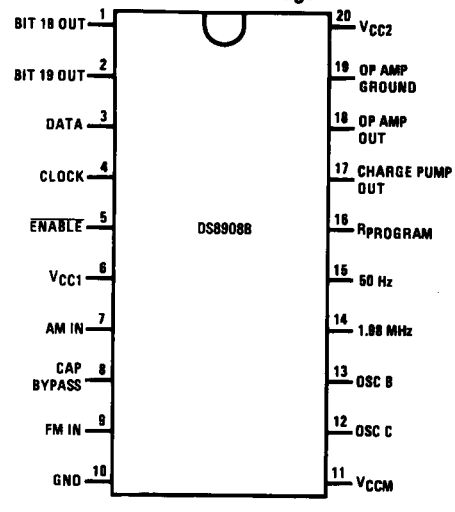
The PLL consists of a 14-bit programmable I^2L divider, an ECL phase comparator, an ECL dual modulus (p/p + 1) prescaler, a high speed charge pump, and an operational amplifier. The programmable divider divides by (N + 1), N being the number loaded into the shift register. The programmable divider is clocked through a $\div 7/8$ prescaler by the AM input or through a $\div 63/64$ prescaler by the FM input. The AM input will work at frequencies up to 15 MHz, while the FM input works up to 120 MHz. The VCO can be tuned with a frequency resolution of either 1 kHz, 9 kHz, 10 kHz, or 20 kHz. The buffered AM and FM inputs are self-biased and can be driven directly by the VCO through a capacitor. The ECL phase comparator produces very accurate resolution of the phase difference between the input signal and the reference oscillator. The high speed charge pump consists of a switchable constant current source and sink. The charge pump can be programmed to deliver from 75 μA to 750 μA of constant current by connection of an external resistor from pin $R_{PROGRAM}$ to ground or the open collector bit outputs. Connection of programming resistors to the bit outputs enables the controller to adjust the loop gain for the particular reference frequency selected. The charge pump will source current if the VCO frequency is high and sink current if the VCO frequency is low. The low noise operational amplifier provided has a high impedance JFET input and a large output voltage range. The op amp's negative input is common with the charge pump output and its positive input is internally biased.

Features

- Uses inexpensive 3.96 MHz reference crystal
- F_{IN} capability greater than 120 MHz allows direct synthesis at FM frequencies
- FM resolution of either 10 kHz or 20 kHz allows usage of 10.7 MHz ceramic filter distribution
- Serial data entry for simplified control
- 50 Hz output for time-of-day reference driven from separate low power V_{CCM}
- 2 open collector buffered outputs for controlling various radio functions or loop gain
- Separate AM and FM inputs; AM input has 15 mV (typical) hysteresis
- Programmable charge pump current sources enable adjustment of system loop gain
- Operational amplifier provides high impedance load to charge pump output and a wide voltage range for the VCO input

Connection Diagram

Dual-In-Line Package



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Top View
Order Number DS8908BN
See NS Package Number N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
(V_{CC1}) (V_{CCM})	7V
(V_{CC2})	17V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
V_{CC1}	4.5	5.5	V
V_{CC2}	V_{CC1} + 1.5	15.0	V
V_{CCM}	3.5	5.5	V
Temperature, T_A	−40	+85	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2.0			V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V			0	10	μA
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IL}	Logical "0" Input Current	Data, Clock, and $\overline{\text{ENABLE}}$ Inputs, V_{IN} = 0V			−5	−25	μA
I_{OH}	Logical "1" Output Current All Bit Outputs, 50 Hz Output	V_{OH} = 5.5V				50	μA
	1.98 MHz Output	V_{OH} = 2.4V, V_{CCM} = 4.5V				−250	μA
V_{OL}	Logical "0" Output Voltage All Bit Outputs	I_{OL} = 5 mA				0.5	V
	50 Hz Output, 1.98 MHz Output	I_{OL} = 250 μA				0.5	V
	1.98 MHz Output	I_{OL} = 20 μA, T_A > 70°C I_{OL} = 20 μA, T_A ≤ 70°C				0.3 0.4	V V
I_{CC1}	Supply Current (V_{CC1})	All Bit Outputs High				160	mA
I_{CCM}	V_{CCM} Supply Current	V_{CCM} = 5.5V, All Other Pins Open			2.5	4.0	mA
I_{OUT}	Charge Pump Ougtput Current	3.33k ≤ R_{PROG} ≤ 33.3k I_{OUT} Measured between Pin 17 and Pin 18 I_{PROG} = V_{CC1}/2 R_{PROG}	Pump Up	−20	I_{PROG}	+20	%
			Pump Down	−20	I_{PROG}	+20	%
			TRI-STATE®		0	11	nA
I_{CC2}	V_{CC2} Supply Current	V_{CCM} = 5V, V_{CC1} = 5.5V, V_{CC2} = 15V All Other Pins Open			6.7	11	mA
OP_{VOH}	Op Amp Minimum High Level	V_{CC1} = 4.5V, I_{OH} = −750 μA		V_{CC2} −0.4			V
OP_{VOL}	Op Amp Maximum Low Level	V_{CC1} = 5.5V, I_{OL} = 750 μA				0.6	V
CPO_{BIAS}	Charge Pump Bias Voltage Delta	CPO Shorted to Op Amp Output CPO = TRI-STATE Op Amp I_{OL}: 750 μA vs −750 μA				100	mV

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, t_r ≤ 10 ns, t_f ≤ 10 ns

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(MIN)(F)}$	F_{IN} Minimum Signal Input	AM and FM Inputs, −40°C ≤ T_A ≤ 85°C			20	100	mV(rms)
$V_{IN(MAX)(F)}$	F_{IN} Maximum Signal Input	AM and FM Inputs, −40°C ≤ T_A ≤ 85°C		1000	1500		mV(rms)
$F_{OPERATE}$	Operating Frequency Range (Sine Wave Input)	V_{IN} = 100 mV rms −40°C ≤ T_A ≤ 85°C	AM	0.5		15	MHz
			FM	80		120	MHz
$R_{IN(FM)}$	AC Input Resistance, FM	120 MHz, V_{IN} = 100 mV rms		600			Ω
$R_{IN(AM)}$	AC Input Resistance, AM	15 MHz, V_{IN} = 100 mV rms		1000			Ω
C_{IN}	Input Capacitance, FM and AM	V_{IN} = 120 MHz (FM), 15 MHz (AM)		3	6	10	pF
t_{EN1}	Minimum ENABLE High Pulse Width				625	1250	ns

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, $t_r \leq 10$ ns, $t_f \leq 10$ ns (Continued)

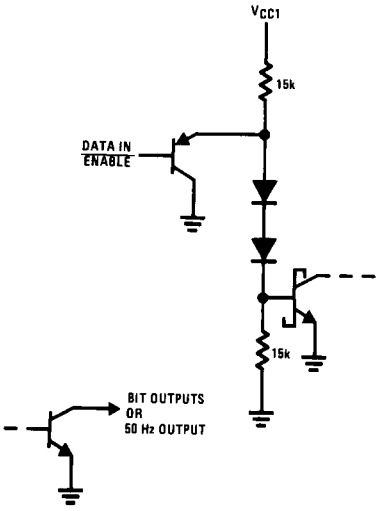
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{\overline{EN}0}$	Minimum $\overline{\text{ENABLE}}$ Low Pulse Width			375	750	ns
$t_{CLK\overline{EN}0}$	Minimum Time before $\overline{\text{ENABLE}}$ Goes Low That CLOCK Must Be Low			−50	0	ns
$t_{\overline{EN}0CLK}$	Minimum Time after $\overline{\text{ENABLE}}$ Goes Low That CLOCK Must Remain Low			275	550	ns
$t_{CLK\overline{EN}1}$	Minimum Time before $\overline{\text{ENABLE}}$ Goes High That Last Positive CLOCK Edge May Occur			300	600	ns
$t_{\overline{EN}1CLK}$	Minimum Time after $\overline{\text{ENABLE}}$ Goes High before an Unused Positive CLOCK Edge May Occur			175	350	ns
t_{CLKH}	Minimum CLOCK High Pulse Width			275	550	ns
t_{CLKL}	Minimum CLOCK Low Pulse Width			400	800	ns
t_{DS}	Minimum DATA Set-Up Time, Minimum Time before CLOCK That DATA Must Be Valid			150	300	ns
t_{DH}	Minimum DATA Hold Time, Minimum Time after CLOCK That DATA Must Remain Valid			400	800	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −40°C to +85°C temperature range for the DS8908B.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Schematic Diagrams (DS8908B AM/FM PLL Typical Input/Output Schematics)



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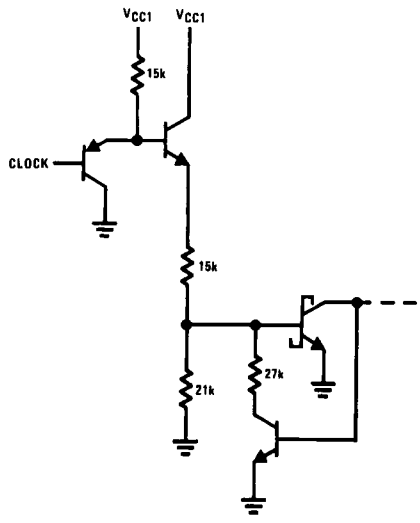

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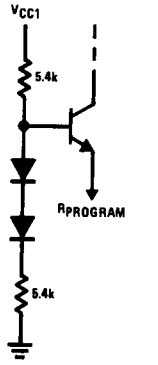

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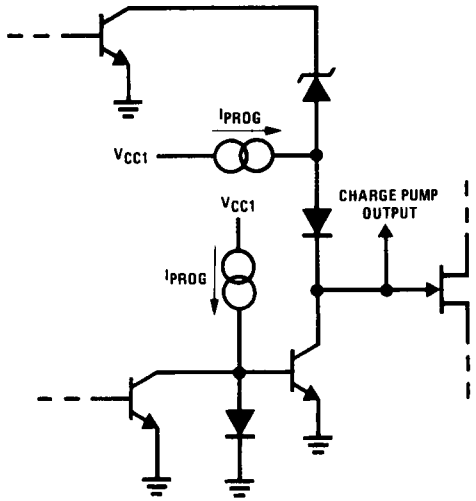
Schematic Diagrams (Continued)



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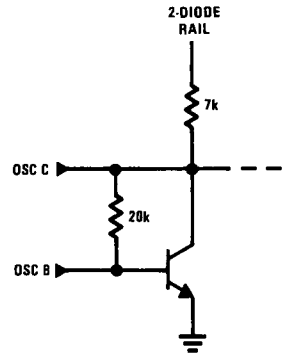

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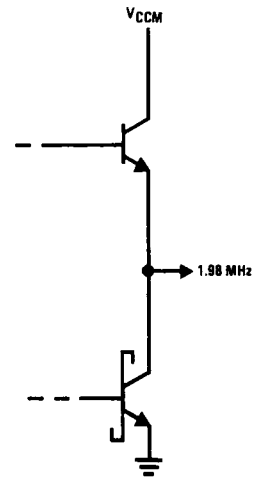

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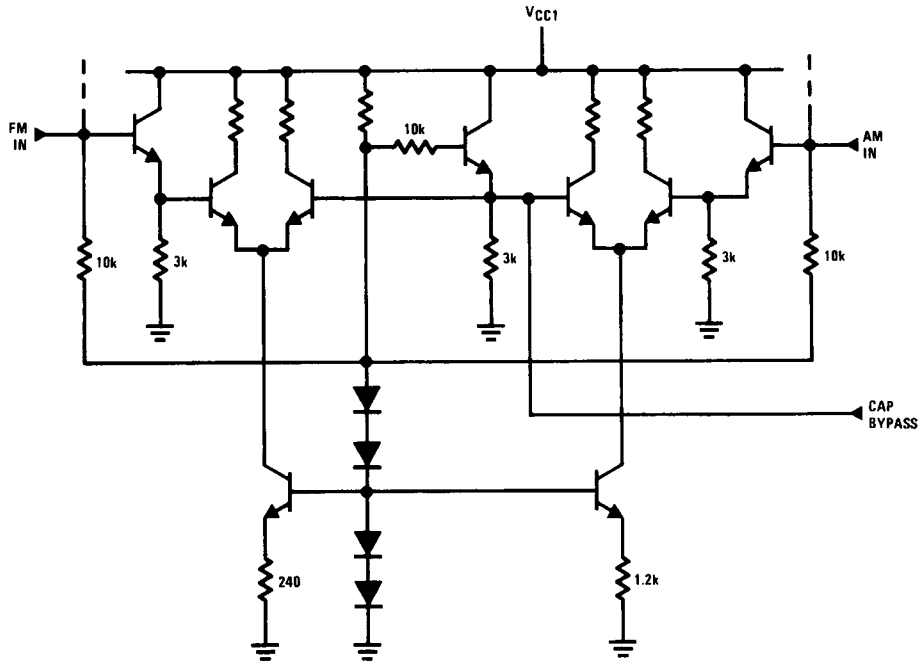

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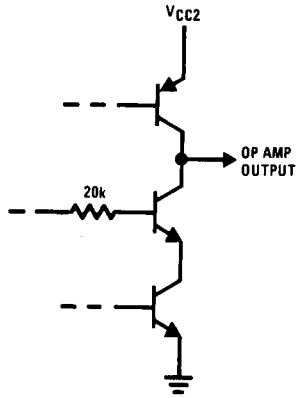
Schematic Diagrams (Continued)



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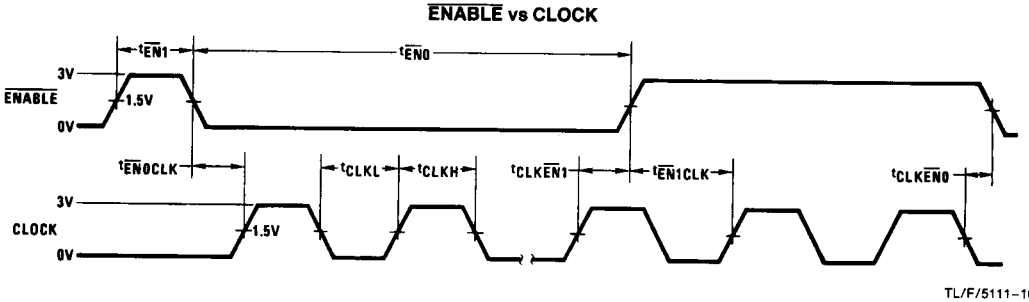
Timing Diagrams*



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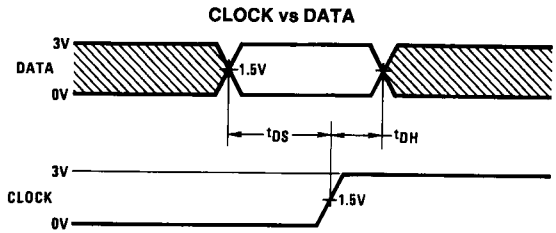

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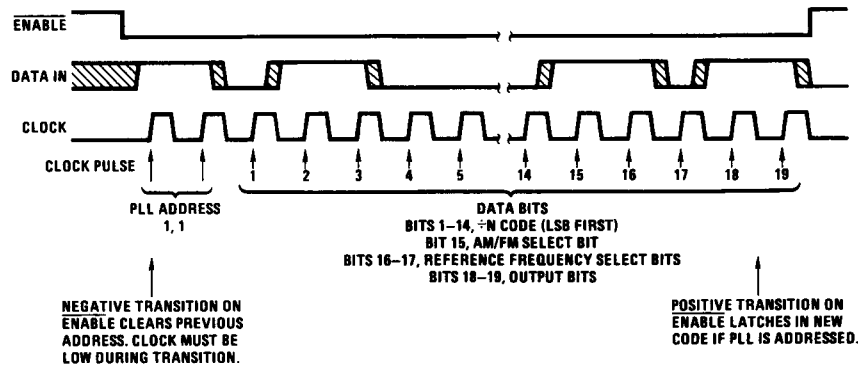
Timing Diagrams* (Continued)

AM/FM Frequency Synthesizer (Scan Mode)



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*Timing diagrams are not drawn to scale. Scale within any one drawing may not be consistent, and intervals are defined positive as drawn.

SERIAL DATA ENTRY INTO THE DS8908B

Serial information entry into the DS8908B is enabled by a low level on the $\overline{\text{ENABLE}}$ input. One binary bit is then accepted from the DATA input with each positive transition of the CLOCK input. The CLOCK input must be low for the specified time preceding and following the negative transition of the $\overline{\text{ENABLE}}$ input.

The first two bits accepted following the negative transition of the $\overline{\text{ENABLE}}$ input are interpreted as address. If these address bits are *not* 1,1 *no* further information will be accepted fromt he DATA inputs, and the internal data latches *will not* be changed when $\overline{\text{ENABLE}}$ returns high.

If these first two bits *are* 1,1, then all succeeding bits are *accepted* as data, and are shifted successively into the internal shift register as long as $\overline{\text{ENABLE}}$ remains low.

Any data bits preceding the 19th to last bit will be shifted out, and thus are irrelevant. Data bits are counted as any bits *following* two valid address bits (1,1) with the $\overline{\text{ENABLE}}$ low. When the $\overline{\text{ENABLE}}$ input returns high, any further serial data entry is inhibited. Upon this positive transition, the data in the internal shift register is transferred into the internal data latches. Note that until this time, the states of the internal data latches have remained unchanged.

These data bits are interpreted as follows:

Data Bit Position	Data Interpretation
Last	Bit 19 Output (Pin 2)
2nd to Last	Bit 18 Output (Pin 1)
3rd to Last	Ref. Freq. Select Bit(1)17
4th to Last	Ref. Freq. Select Bit(1)16
5th to Last	AM/FM Select Bit 15
6th to Last	(2^{13})
7th to Last	(2^{12})
8th to Last	(2^{11})
9th to Last	(2^{10})
10th to Last	(2^{9})
11th to Last	(2^{8})
12th to Last	(2^{7})
13th to Last	(2^{6})
14th to Last	(2^{5})
15th to Last	(2^{4})
16th to Last	(2^{3})
17th to Last	(2^{2})
18th to Last	(2^{1})
19th to Last	LSB of $\div N(2^{0})$

$\div N(2)$

Note 1: See Reference Frequency Select Truth Table.

Note 2: The actual divide code is N + 1, ie., the number loaded plus 1.

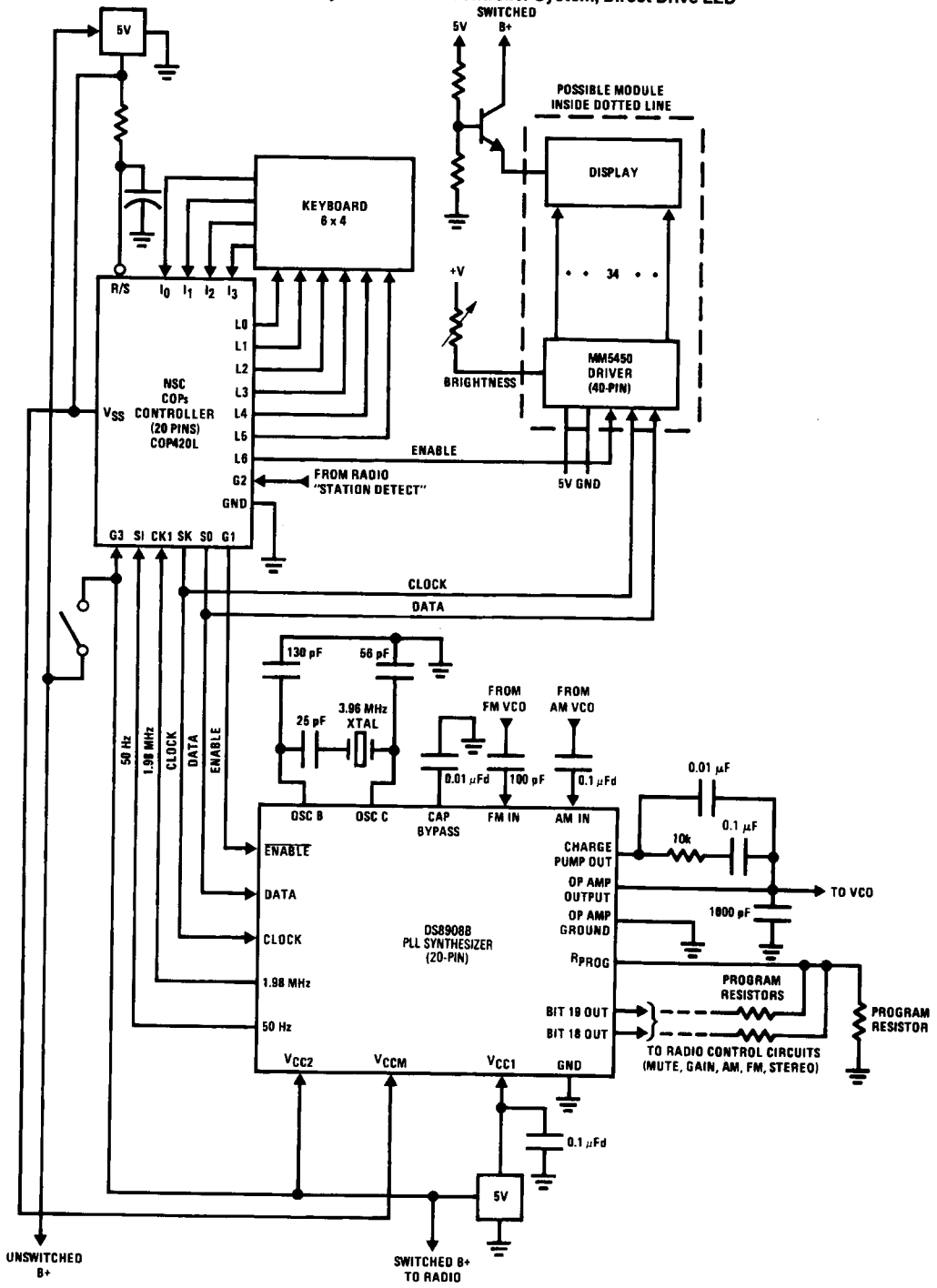
Truth Table

Reference Frequency Selection Truth Table

Serial Data		Reference Frequency
Bit 16	Bit 17	(kHz)
1	1	20
1	0	10
0	1	9
0	0	1

Typical Application Additional application notes are located at the back of section 11.

Electronically Tuned Radio Controller System; Direct Drive LED



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Logic Diagram

AM/FM PLL/Synthesizer (Serial Data 20-Pin Package)