



THIS SPEC IS OBSOLETE

Spec No: 38-07522

Spec Title: CY25023 SPREAD SPECTRUM CLOCK GENERATOR
7FOR EMI REDUCTION

Sunset Owner: Christopher Martin (CXQ)

Replaced by: None

Spread Spectrum Clock Generator for EMI Reduction

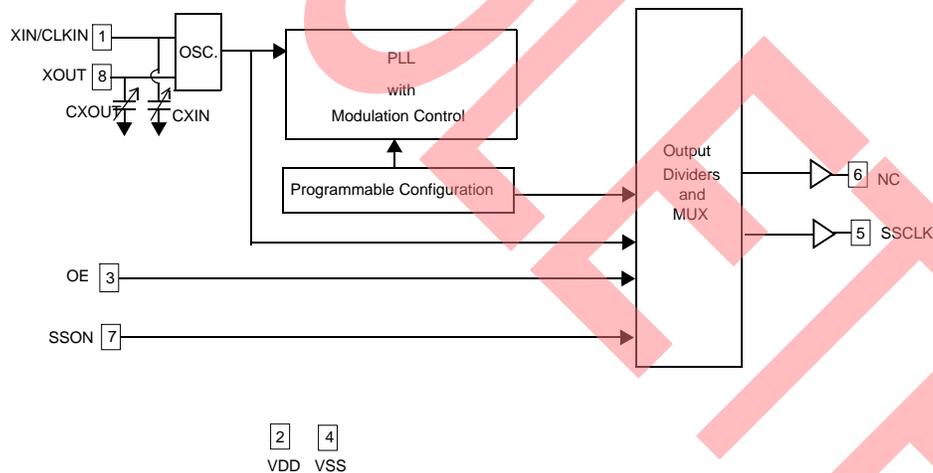
Features

- SSCLK frequency: 52.0 MHz
- Spread spectrum output with nominal 31.5 kHz modulation frequency
 - Center spread: $\pm 1.0\%$
- Input frequency
 - External clock or crystal: 16.384 MHz
- Integrated phase-locked loop (PLL)
- Low cycle to cycle jitter
- 3.3V operation
- Spread spectrum on and off function
- Output enable function

Benefits

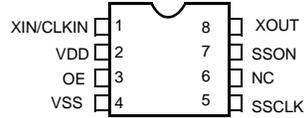
- Services most PC peripherals, networking, and consumer applications.
- Provides electromagnetic interference (EMI) reduction, to meet regulatory agency electromagnetic compliance (EMC) requirements.
- Eliminates the need for expensive and difficult to use overtone crystals.
- Internal PLL to generate up to 200 MHz output. Able to generate custom frequencies from an external crystal or a driven source.
- Suitable for most PC, consumer, and networking applications.
- Application compatibility in standard and low power systems.
- Provides ability to enable or disable spread spectrum with an external pin.
- Enables output clocks to High-Z state.

Logic Block Diagram



Pin Configurations

Figure 1. CY25023, 8-Pin SOIC



Pin Description

Pin	Name	Description
1	XIN/CLKIN	Reference Crystal or Clock Input (16.384 MHz)
2	VDD	3.3V Voltage Supply
3	OE	Output Enable Pin: Active High. If OE = 1, SSCLK is enabled.
4	VSS	GND
5	SSCLK	Spread Spectrum Clock Output (52.0 MHz, $\pm 1.0\%$ center spread)
6	NC	No Connect
7	SSON	Spread Spectrum Control. 1 = spread on, 0 = spread off.
8	XOUT	Crystal Output. Leave this pin floating if external clock is used.

Table 1. Spread Spectrum Table

Part Number	Spread Percentage
CY25023SC-1	$\pm 1.0\%$

Absolute Maximum Condition

Supply Voltage (VDD).....	-0.5 to +7.0V	Data Retention at Tj=125°C	>10 years
DC Input Voltage	-0.5V to V _{DD} +0.5	Package Power Dissipation.....	350 mW
Storage Temperature (Non-Condensing)....	-55°C to +125°C	Static Discharge Voltage.....	≥ 2000V
Junction Temperature	-40°C to +125°C	(per MIL-STD-883, Method 3015)	

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V _{DD}	Supply Voltage	3.13	3.30	3.45	V
T _A	Ambient Temperature	0		70	° C
C _{LOAD}	Max. Load Capacitance at Pin 6			15	pF
XIN/CLKIN	External Reference, Crystal or Clock Input		16.384		MHz
F _{SSCLK}	SSCLK Output Frequency, C _{LOAD} = 15 pF		52.0		MHz
SS%	Spread Spectrum, CY25023SC-1		±1.0		%
T _{PU}	Power Up Time—for all VDDs to reach minimum specified voltage (power ramp must be monotonic)	0.05		500	ms

DC Electrical Specifications

Parameter	Description	Condition	Min	Typ	Max	Unit
I _{OH}	Output High Current	V _{OH} = V _{DD} - 0.5, V _{DD} =3.3V (source)	12	24		mA
I _{OL}	Output Low Current	V _{OL} = 0.5, V _{DD} = 3.3V (sink)	12	24		mA
V _{IH}	Input High Voltage	CMOS levels, 70% of V _{DD}	0.7V _{DD}			V
V _{IL}	Input Low Voltage	CMOS levels, 30% of V _{DD}			0.3V _{DD}	V
I _{IH}	Input High Current, OE and SSON pins	V _{in} =V _{DD}			10	μA
I _{IL}	Input Low Current, OE and SSON pins	V _{in} =V _{SS}			10	μA
I _{OZ}	Output Leakage Current	Three-state output, OE = 0	-10		10	μA
C _{XIN} /C _{XOUT} ^[1]	Capacitance at Pin 1 and Pin 8			22		pF
C _{IN} ^[1]	Input Capacitance at Pin 3 and Pin 7.	Input pins excluding XIN and XOUT		5	7	pF
I _{VDD}	Supply Current	V _{DD} = 3.45V, Fin = 16.384 MHz, SSCLK = 52.0 MHz, C _{LOAD} = 15 pF, OE = SSON = V _{DD}		30	40	mA

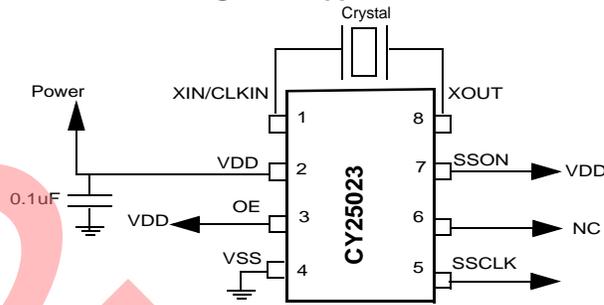
AC Electrical Specifications^[1]

Parameter	Description	Condition	Min	Typ	Max	Unit
DC	Output Duty Cycle	SSCLK, measured at VDD/2	45	50	55	%
SR1	Rising Edge Slew Rate	SSCLK from 20% to 80% of V _{DD}	0.7	1.1	1.5	V/ns
SR2	Falling Edge Slew Rate	SSCLK from 80% to 20% of V _{DD}	0.7	1.1	1.5	V/ns
F _{MOD}	Frequency Modulation	SSON = 1	30.0	31.5	33.0	kHz
tj1	Peak Cycle to Cycle Jitter. SSCLK pin.	SSCLK = 52.0 MHz. Spread on		100	200	ps
T ₁₀	PLL Lock Time	Time from VDD minimum voltage to valid output frequencies		3	5	ms
T _{OE1}	Output Disable time (pin3 = OE)	Time from falling edge on OE to stopped outputs, (Asynchronous)		150	300	ns
T _{OE2}	Output Enable Time (pin3 = OE)	Time from rising edge on OE to outputs at a valid frequency, (Asynchronous)		150	300	ns

Note

1. Guaranteed by Characterization, not 100% tested.

Figure 2. Application Circuit^[2,3]



Switching Waveforms

Figure 3. Duty Cycle Timing ($DC = t_{1A}/t_{1B}$)

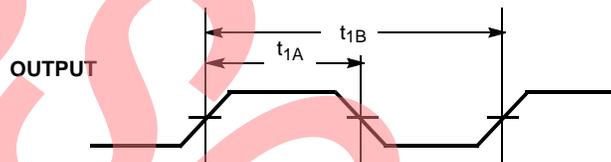


Figure 4. Output Rise/Fall Time (SSCLK and REFCLK)

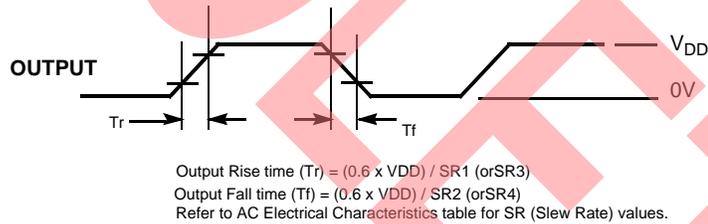
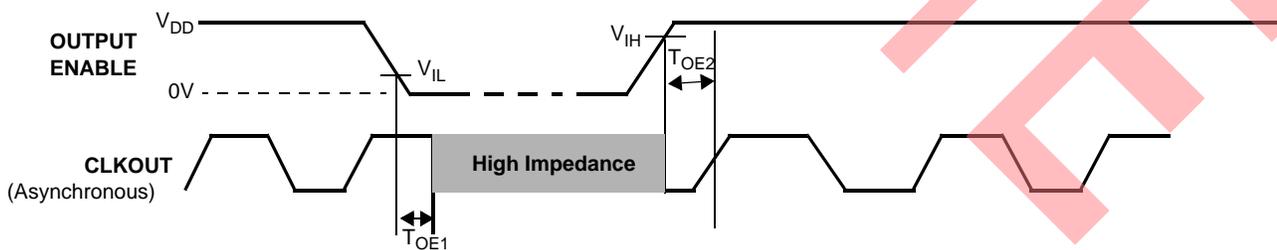


Figure 5. Output Enable/Disable Timing



Notes

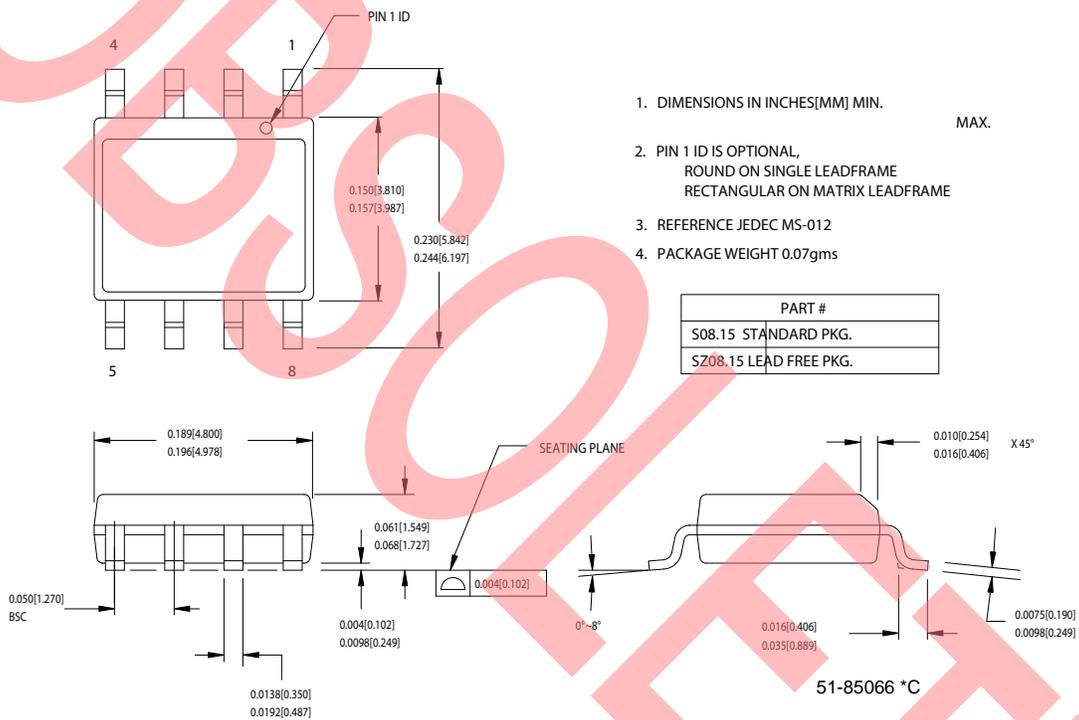
2. IF an external clock is used, apply the clock to CLKIN(pin1) and leave XOUT(pin8) floating (unconnected).
3. If SSON(pin7) is LOW(V_{SS}), the frequency modulation will be stopped on SSCLK pin(pin5)

Ordering Information

Part Number	Package Type	Product Flow
CY25023SXC-1 ^[4]	8-pin Small Outline Integrated Circuit (SOIC)	Commercial, 0 to 70°C
CY25023SXC-1T ^[4]	8-pin Small Outline Integrated Circuit (SOIC) – Tape and Reel	Commercial, 0 to 70°C
CY25023KSXC-1	8-pin Small Outline Integrated Circuit (SOIC)	Commercial, 0 to 70°C
CY25023KSXC-1T	8-pin Small Outline Integrated Circuit (SOIC) – Tape and Reel	Commercial, 0 to 70°C

Package Drawing and Dimensions

Figure 6. 8-lead (150-Mil) SOIC – S8



Note

4. Not recommended for new designs.

Document History Page

Document Title: CY25023 Spread Spectrum Clock Generator for EMI Reduction Document Number: 38-07522				
REV.	ECN NO.	Orig. of Change	Submission Date	Description of Change
**	124268	CKN	See ECN	New Data Sheet
*A	2505007	AESA	See ECN	Updated template and package diagram. In ordering information table, replaced non-Pb-free part numbers CY25023SC-1 and CY25023SC-1T with Pb-free part numbers CY25023SXC-1 and CY25023SXC-1T. Added Note "Not recommended for new designs." Added part number CY25023KSXC-1, and CY25023KSXC-1T.
*B	2908854	CDQ	04/08/10	Inactive parts. Obsolete datasheet.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

PSoC	psoc.cypress.com
Clocks & Buffers	clocks.cypress.com
Wireless	wireless.cypress.com
Memories	memory.cypress.com
Image Sensors	image.cypress.com

PSoC Solutions

General	psoc.cypress.com/solutions
Low Power/Low Voltage	psoc.cypress.com/low-power
Precision Analog	psoc.cypress.com/precision-analog
LCD Drive	psoc.cypress.com/lcd-drive
CAN 2.0b	psoc.cypress.com/can
USB	psoc.cypress.com/usb

© Cypress Semiconductor Corporation, 2003-2008. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.