

NLAS324

Dual SPST Analog Switch, Low Voltage, Single Supply

The NLAS324 is a dual SPST (Single Pole, Single Throw) switch, similar to 1/2 a standard 4066. The device permits the independent selection of 2 analog/digital signals. Available in the Ultra-Small 8 package.

The use of advanced 0.6 μ CMOS process, improves the R_{ON} resistance considerably compared to older higher voltage technologies.

Features

- On Resistance is 20 Ω Typical at 5.0 V
- Matching is < Ω Between Sections
- 2 – 6 V Operating Range
- Ultra Low < 5 pC Charge Injection
- Ultra Low Leakage < 1 nA at 5.0 V, 25°C
- Wide Bandwidth > 200 MHz, -3 dB
- 2000 V ESD (HBM)
- Ron Flatness $\pm 6 \Omega$ at 5.0 V
- Negative Enable
- Switches are Independent
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

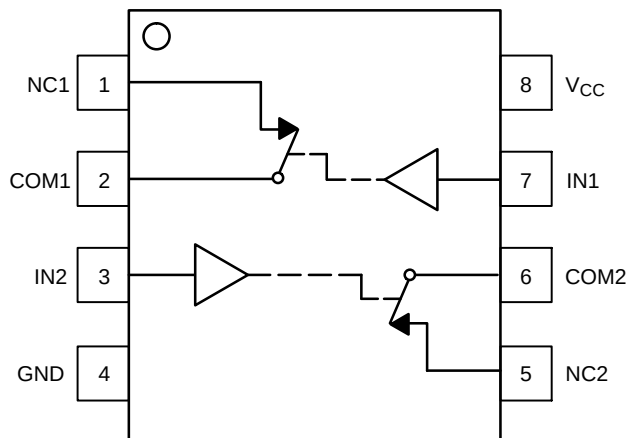
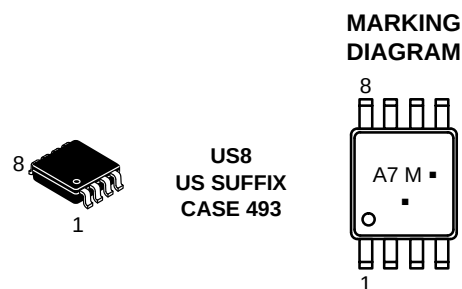


Figure 1. Pinout



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A7 = Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT

1	NC1
2	COM1
3	IN2
4	GND
5	NC2
6	COM2
7	IN1
8	VCC

FUNCTION TABLE

On/Off Enable Input	State of Analog Switch
L	On
H	Off

ORDERING INFORMATION

Device	Package	Shipping†
NLAS324USG	US8 (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	− 0.5 to + 7.0	V
V _I	DC Input Voltage	− 0.5 to + 7.0	V
V _O	DC Output Voltage	− 0.5 to + 7.0	V
I _{IK}	DC Input Diode Current V _I < GND	− 50	mA
I _{OK}	DC Output Diode Current V _O < GND	− 50	mA
I _O	DC Output Sink Current	± 50	mA
I _{CC}	DC Supply Current per Supply Pin	± 100	mA
I _{GND}	DC Ground Current per Ground Pin	± 100	mA
T _{STG}	Storage Temperature Range	− 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature under Bias	+ 150	°C
θ _{JA}	Thermal Resistance (Note 1)	250	°C/W
P _D	Power Dissipation in Still Air at 85°C	250	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 150 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage	2.0	5.5	V
V _{IN}	Digital Input Voltage (Enable)	GND	5.5	V
V _{IO}	Static or Dynamic Voltage Across an Off Switch	GND	V _{CC}	V
V _{IS}	Analog Input Voltage (NO, COM)	GND	V _{CC}	V
T _A	Operating Temperature Range, All Package Types	−55	+125	°C
t _r , t _f	Input Rise or Fall Time, (Enable Input) V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

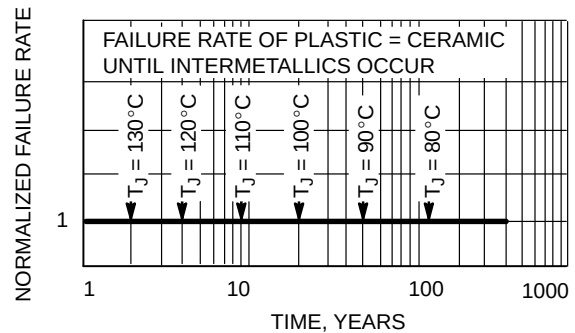


Figure 2. Failure Rate vs. Time Junction Temperature

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC}	Guaranteed Max Limit			Unit
				-55 to 25°C	<85°C	<125°C	
V _{IH}	Minimum High-Level Input Voltage, Enable Inputs		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85	1.5 2.1 3.15 3.85	1.5 2.1 3.15 3.85	V
V _{IL}	Maximum Low-Level Input Voltage, Enable Inputs		2.0 3.0 4.5 5.5	0.5 0.9 1.35 1.65	0.5 0.9 1.35 1.65	0.5 0.9 1.35 1.65	V
I _{IN}	Maximum Input Leakage Current, Enable Inputs	V _{IN} = 5.5 V or GND	0 V to 5.5 V	±0.1	±1.0	±1.0	µA
I _{CC}	Maximum Quiescent Supply Current (per package)	Enable and V _{IS} = V _{CC} or GND	5.5	1.0	1.0	2.0	µA

DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Condition	V _{CC}	Guaranteed Max Limit			Unit
				-55 to 25°C	<85°C	<125°C	
R _{ON}	Maximum ON Resistance (Figures 8 – 12)	V _{IN} = V _{IH} V _{IS} = V _{CC} to GND I _{IS} ≤ 10.0mA	3.0 4.5 5.5	45 30 25	50 35 30	55 40 35	Ω
R _{FLAT(ON)}	ON Resistance Flatness	V _{IN} = V _{IH} I _{IS} ≤ 10.0mA V _{IS} = 1V, 2V, 3.5V	4.5	4	4	5	Ω
I _{NO(OFF)}	Off Leakage Current, Pin 2 (Figure 3)	V _{IN} = V _{IL} V _{NO} = 1.0 V, V _{COM} = 4.5 V or V _{COM} = 1.0 V and V _{NO} 4.5 V	5.5	1	10	100	nA
I _{COM(OFF)}	Off Leakage Current, Pin 1 (Figure 3)	V _{IN} = V _{IL} V _{NO} = 4.5 V or 1.0 V V _{COM} = 1.0 V or 4.5 V	5.5	1	10	100	nA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

Symbol	Parameter	Test Conditions	V _{CC} (V)	Guaranteed Max Limit									Unit
				−55 to 25°C			<85°C			<125°C			
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{ON}	Turn-On Time	R _L = 300 Ω, C _L = 35 pF (Figures 4, 5, and 13)	2.03.04.55.5		7.0 5.0 4.5 4.5	14 10 9 9			16 12 11 11			16 12 11 11	ns
t _{OFF}	Turn-Off Time	R _L = 300 Ω, C _L = 35 pF (Figures 4, 5, and 13)	2.03.04.5 5.5		11.0 7.0 5.0 5.0	22 14 10 10			24 16 12 12			24 16 12 12	ns

			Typical @ 25, V _{CC} = 5.0 V									Unit
C _{IN} C _{NO} or C _{NC} C _{COM(OFF)} C _{COM(ON)}	Maximum Input Capacitance, Select Input Analog I/O (switch off) Common I/O (switch off) Feedthrough (switch on)											
												pF

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Condition	V _{CC} V	Limit	Unit
				25°C	
BW	Maximum On-Channel -3dB Bandwidth or Minimum Frequency Response	V _{IS} = 0 dBm V _{IS} centered between V _{CC} and GND (Figures 6 and 14)	3.0 4.5 5.5	190 200 220	MHz
V _{ONL}	Maximum Feedthrough On Loss	V _{IS} = 0 dBm @ 10 kHz V _{IS} centered between V _{CC} and GND (Figure 6)	3.0 4.5 5.5	-2 -2 -2	dB
V _{ISO}	Off-Channel Isolation	f = 100 kHz; V _{IS} = 1 V RMS V _{IS} centered between V _{CC} and GND (Figures 6 and 15)	3.0 4.5 5.5	-93	dB
Q	Charge Injection Enable Input to Common I/O	V _{IS} = V _{CC} to GND, F _{IS} = 20 kHz t _r = t _f = 3 ns R _{IS} = 0 Ω, C _L = 1000 pF Q = C _L * ΔV _{OUT} (Figures 7 and 16)	3.0 5.5	1.5 3.0	pC
THD	Total Harmonic Distortion THD + Noise	F _{IS} = 20 Hz to 1 MHz, R _L = R _{gen} = 600 Ω, C _L = 50 pF V _{IS} = 3.0 V _{PP} sine wave V _{IS} = 5.0 V _{PP} sine wave (Figure 17)	3.3 5.5	0.3 0.15	%

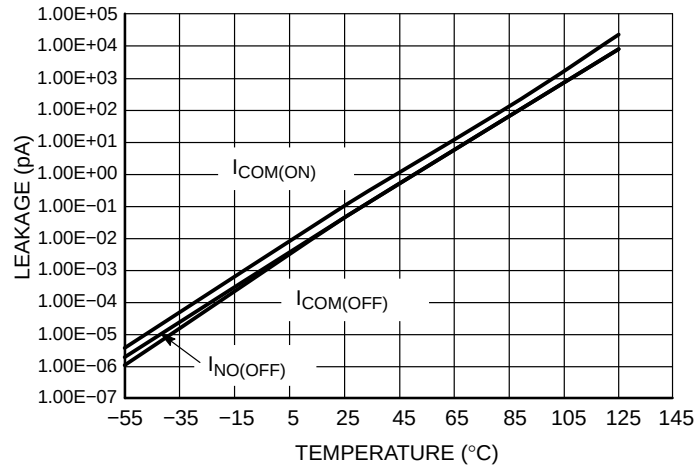


Figure 3. Switch Leakage vs. Temperature

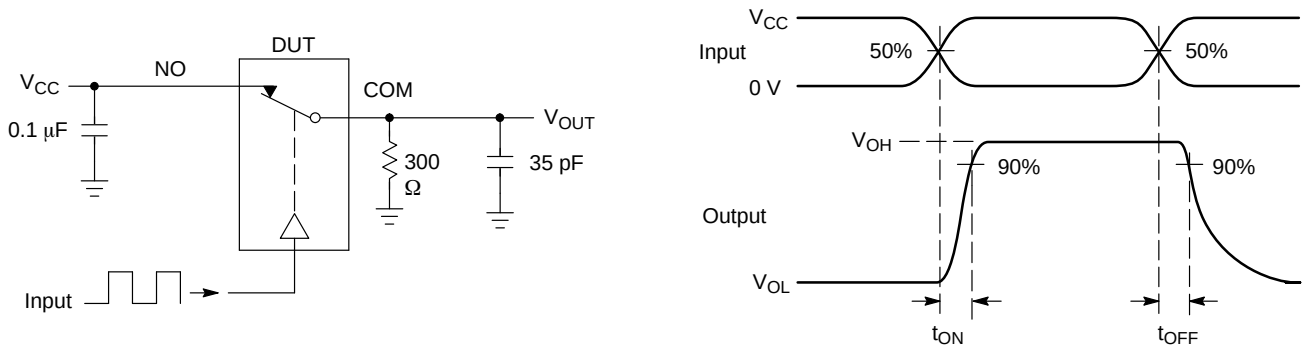


Figure 4. t_{ON}/t_{OFF}

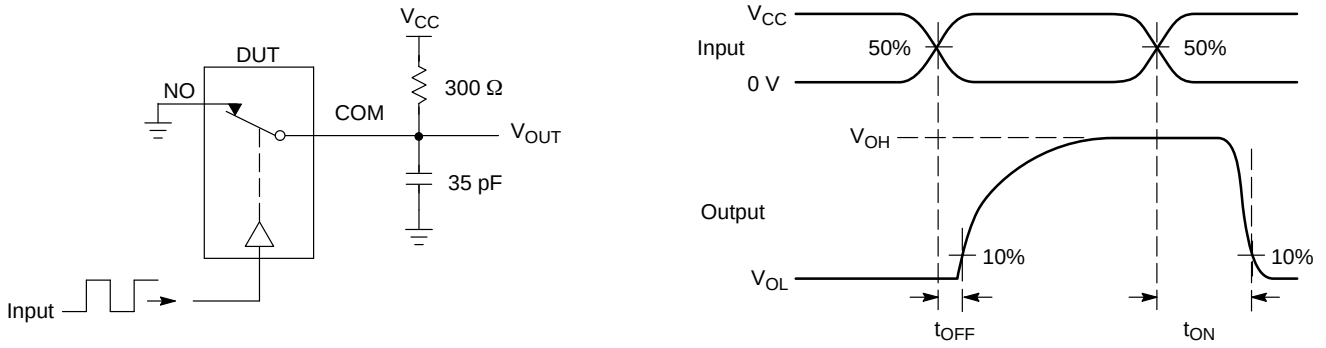
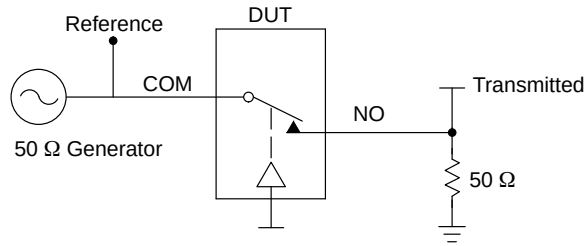


Figure 5. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

Figure 6. Off Channel Isolation/On Channel Loss (BW)/Crosstalk
(On Channel to Off Channel)/ V_{ONL}

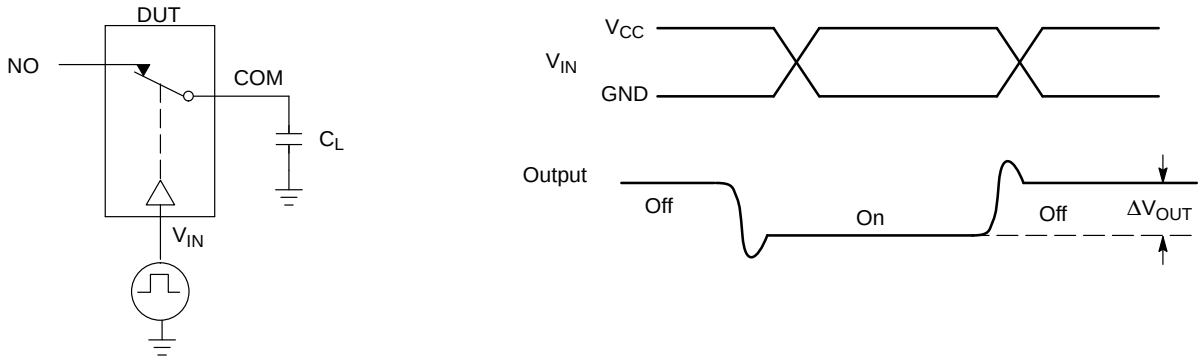


Figure 7. Charge Injection: (Q)

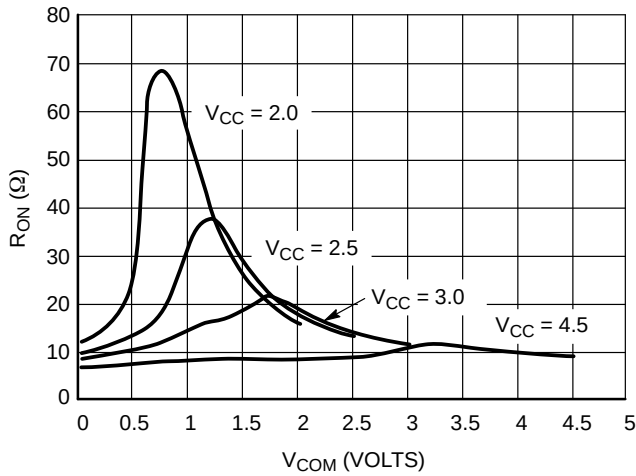


Figure 8. R_{ON} vs. V_{COM} and V_{CC} (@25°C)

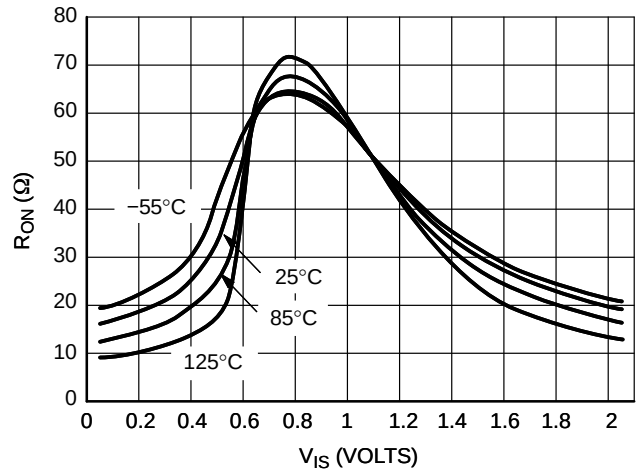


Figure 9. R_{ON} vs. V_{COM} and Temperature, $V_{CC} = 2.0$ V

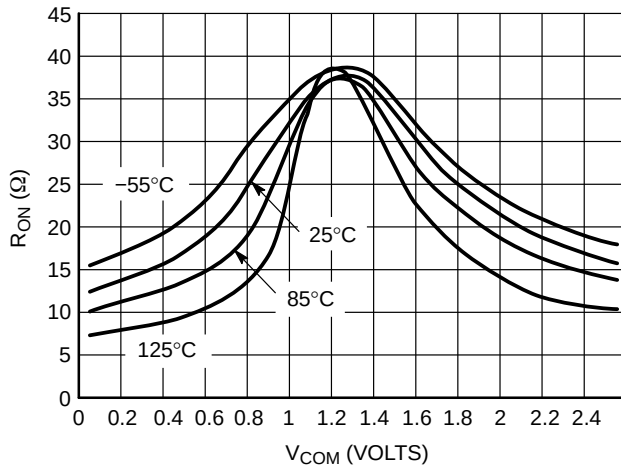


Figure 10. R_{ON} vs. V_{COM} and Temperature, $V_{CC} = 2.5$ V

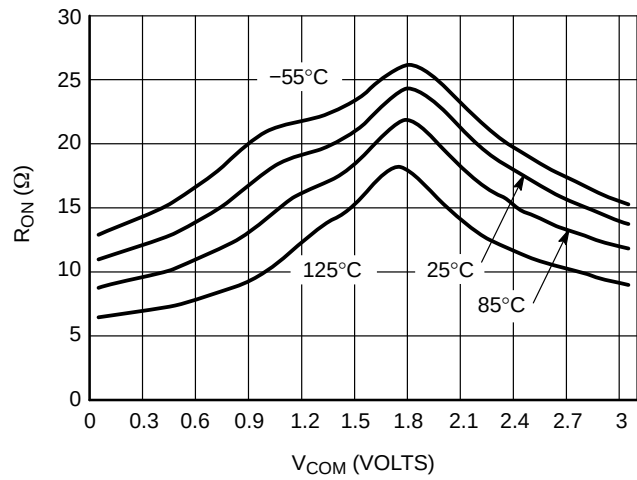


Figure 11. R_{ON} vs. V_{COM} and Temperature, $V_{CC} = 3.0$ V

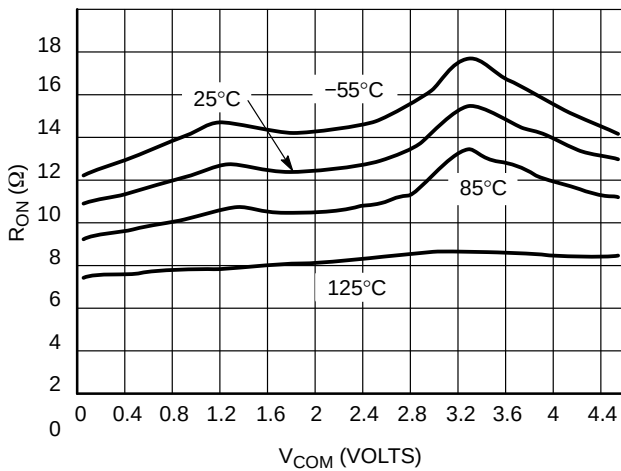


Figure 12. R_{ON} vs. V_{COM} and Temperature, $V_{CC} = 4.5$ V

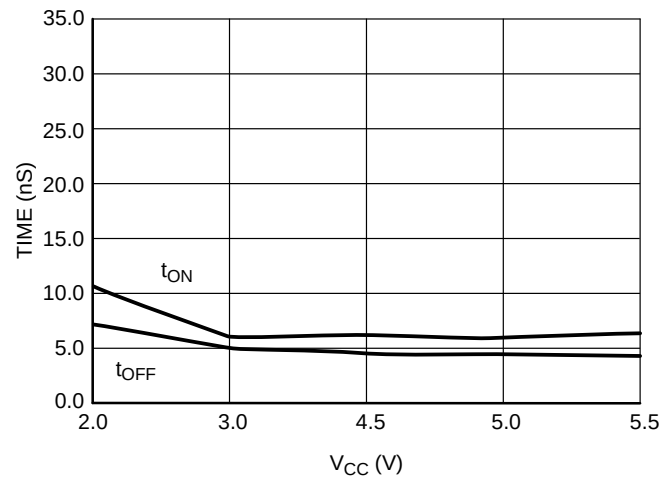


Figure 13. Switching Time vs. Supply Voltage, $T = 25^\circ\text{C}$

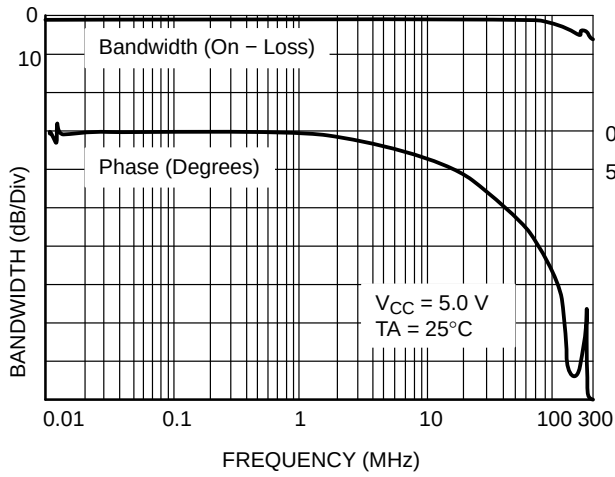


Figure 14. ON Channel Bandwidth and Phase Shift Over Frequency

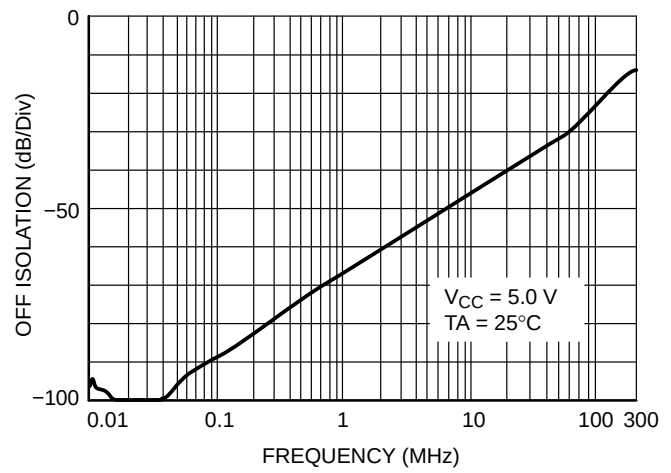


Figure 15. Off Channel Isolation

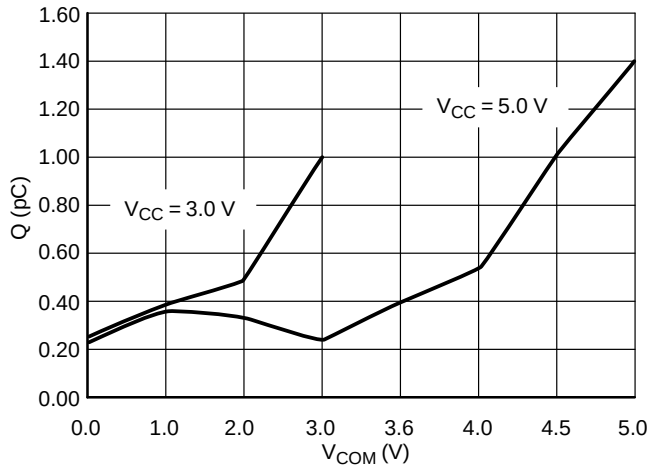


Figure 16. Charge Injection vs. V_{COM}

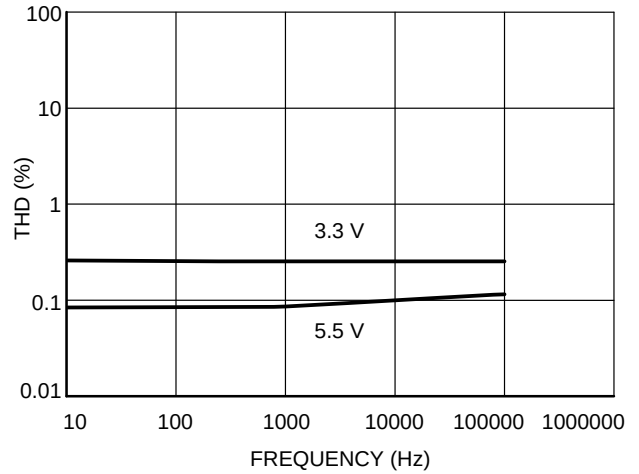
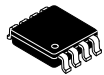


Figure 17. THD vs. Frequency

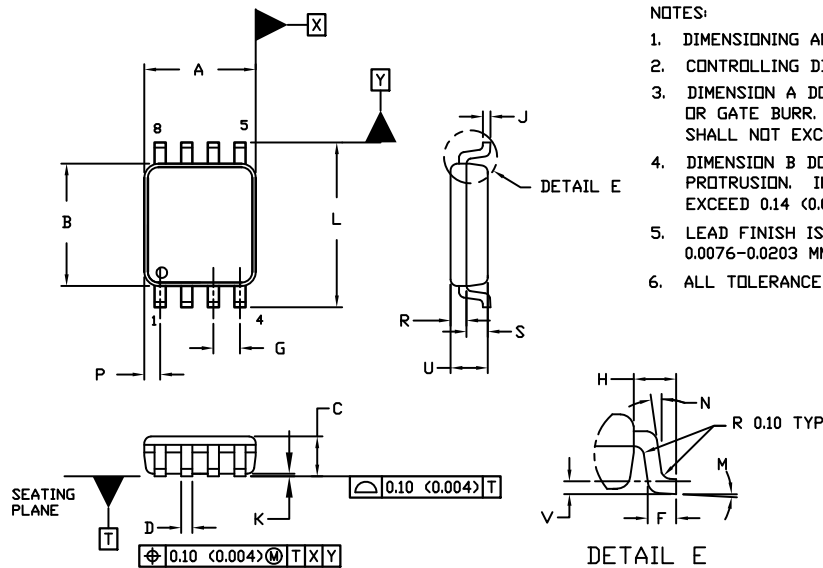
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 4:1

US8
CASE 493
ISSUE F

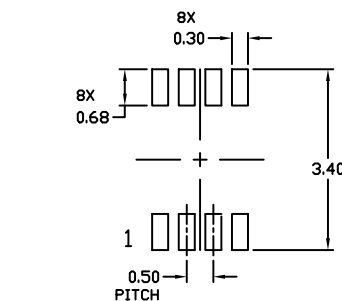
DATE 01 SEP 2021



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR. MOLD FLASH, PROTRUSION, OR GATE BURR SHALL NOT EXCEED 0.14 (0.0055") PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.14 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM (0.003-0.008").
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 MM (0.002").

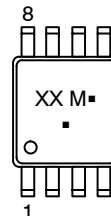
DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50	BSC	0.020	BSC
H	0.40	REF	0.016	REF
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.25	0.118	0.128
M	0°	6°	0°	6°
N	0°	10°	0°	10°
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12	BSC	0.005	BSC



RECOMMENDED * MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the DFN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
■ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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