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# LMH6580/LMH6581

## 8x4 500 MHz Analog Crosspoint Switch, Gain of 1, Gain of 2

### General Description

The LMH® family of products is joined by the LMH6580 and the LMH6581, high speed, non-blocking, analog, crosspoint switches. The LMH6580/LMH6581 are designed for high speed, DC coupled, analog signals such as high resolution video (UXGA and higher). The LMH6580/LMH6581 each has eight inputs and four outputs. The non-blocking architecture allows any output to be connected to any input, including an input that is already selected. With fully buffered inputs the LMH6580/LMH6581 can be impedance matched to nearly any source impedance. The buffered outputs of the LMH6580/LMH6581 can drive up to two back terminated video loads (75Ω load). The outputs and inputs also feature high impedance inactive states allowing high performance input and output expansion for array sizes such as 8 x 8 or 16 x 4 by combining two devices. The LMH6580/LMH6581 are controlled with a 4 pin serial interface that can be configured as a 3 wire interface. Both serial mode and addressed modes are available.

The LMH6580/LMH6581 come in 48-pin TQFP packages. They also have diagonally symmetrical pin assignments to facilitate double sided board layouts and easy pin connections for expansion.

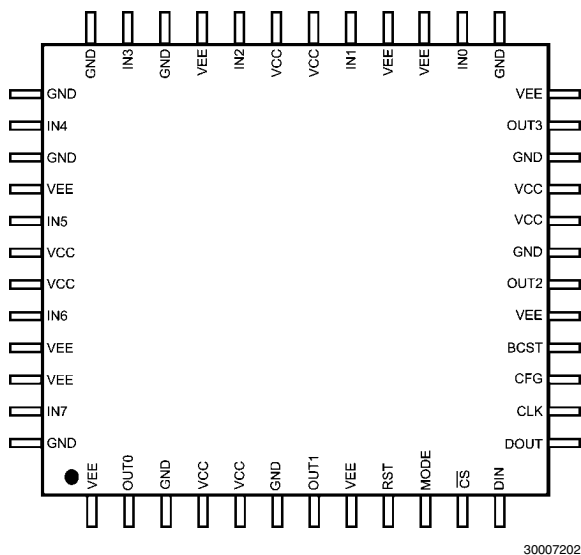
### Features

- 8 inputs and 4 outputs
- 48-pin TQFP package
- -3 dB bandwidth ( $V_{OUT} = 2 V_{PP}$ ,  $R_L = 1 k\Omega$ ) 500 MHz
- -3 dB bandwidth ( $V_{OUT} = 2 V_{PP}$ ,  $R_L = 150\Omega$ ) 450 MHz
- Fast slew rate 2100 V/ $\mu$ s
- Channel to channel crosstalk (10/100 MHz) -70/-52 dBc
- All hostile crosstalk (10/100 MHz) -55/-45 dBc
- Easy to use serial programming 4 wire bus
- Two programming modes Serial & addressed modes
- Symmetrical pinout facilitates expansion.
- Output current  $\pm 70$  mA
- Two gain options  $A_V = 1$  or  $A_V = 2$

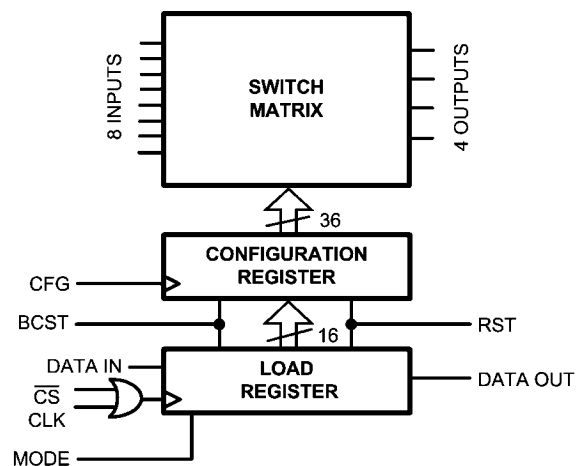
### Applications

- Studio monitoring/production video systems
- Conference room multimedia video systems
- KVM (keyboard video mouse) systems
- Security/surveillance systems
- Multi-antenna diversity radio
- Video test equipment
- Medical imaging
- Wide-band routers & switches

### Connection Diagram



### Block Diagram



30007211

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2000V
Machine Model	200V
$V_S$	$\pm 6V$
$I_{IN}$ (Input Pins)	$\pm 20$ mA
$I_{OUT}$	(Note 3)
Input Voltage Range	$V^-$ to $V^+$
Maximum Junction Temperature	+150°C

Storage Temperature Range	-65°C to +150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C

**Operating Ratings** (Note 1)

Temperature Range (Note 4)	-40°C to +85°C	
Supply Voltage Range	$\pm 3V$ to $\pm 5.5V$	
Thermal Resistance	$\theta_{JA}$	$\theta_{JC}$
48-Pin TQFP	44°C/W	12°C/W

 **$\pm 3.3V$  Electrical Characteristics** (Note 5)

Unless otherwise specified, typical conditions are:  $T_A = 25^\circ\text{C}$ ,  $A_V = +2$ ,  $V_S = \pm 3.3V$ ,  $R_L = 100\Omega$ ; **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
<b>Frequency Domain Performance</b>						
SSBW	-3 dB Bandwidth	$V_{OUT} = 0.5 V_{PP}$		425		MHz
LSBW		LMH6580 $V_{OUT} = 1 V_{PP}$ , LMH6581 $V_{OUT} = 2 V_{PP}$ , $R_L = 1\text{ k}\Omega$		500		
		LMH6580 $V_{OUT} = 1 V_{PP}$ , LMH6581 $V_{OUT} = 2 V_{PP}$ , $R_L = 150\Omega$		450		
GF	0.1 dB Gain Flatness	LMH6580 $V_{OUT} = 1 V_{PP}$ , LMH6581 $V_{OUT} = 2 V_{PP}$ , $R_L = 150\Omega$		70		MHz
<b>Time Domain Response</b>						
$t_r$	Rise Time	LMH6580 1V Step, LMH6581 2V Step, 10% to 90%		3.1		ns
$t_f$	Fall Time	LMH6580 1V Step, LMH6581 2V Step, 10% to 90%		1.4		ns
OS	Overshoot	2V Step		<1		%
SR	Slew Rate	LMH6580, 2 $V_{PP}$ , 40% to 60% (Note 6)		900		V/ $\mu$ s
		LMH6581, 2 $V_{PP}$ , 40% to 60% (Note 6)		1700		V/ $\mu$ s
$t_s$	Settling Time	2V Step, $V_{OUT}$ within 0.5%		7		ns
<b>Distortion And Noise Response</b>						
HD2	2 <sup>nd</sup> Harmonic Distortion	2 $V_{PP}$ , 10 MHz		-76		dBc
HD3	3 <sup>rd</sup> Harmonic Distortion	2 $V_{PP}$ , 10 MHz		-76		dBc
$e_n$	Input Referred Voltage Noise	>1 MHz		12		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input Referred Noise Current	>1 MHz		2		pA/ $\sqrt{\text{Hz}}$
XTLK	Crosstalk	All Hostile, $f = 100$ MHz		-45		dBc
ISOL	Off Isolation	$f = 100$ MHz		-60		dBc
<b>Static, DC Performance</b>						
$A_V$	Gain	LMH6581	1.986	2.00	2.014	
		LMH6580	0.994	1.00	1.005	
$V_{OS}$	Input Offset Voltage			$\pm 3$	$\pm 17$	mV
$TCV_{OS}$	Input Offset Voltage Average Drift	(Note 10)		38		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current	Non-Inverting (Note 9)		-5		$\mu\text{A}$
$TCI_B$	Input Bias Current Average Drift	Non-Inverting (Note 10)		-12		nA/ $^\circ\text{C}$

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
V <sub>O</sub>	Output Voltage Range	LMH6581, R <sub>L</sub> = 100Ω	±1.8	±2.1		V
		LMH6580, R <sub>L</sub> = 100Ω	±1.24	±1.3		
V <sub>O</sub>	Output Voltage Range	LMH6581, R <sub>L</sub> = ∞Ω, (Note 11)	±2.08	±2.2		V
		LMH6580 R <sub>L</sub> = ∞Ω,	±1.25	±1.3		
PSRR	Power Supply Rejection Ratio			-45		dBc
I <sub>CC</sub>	Positive Supply Current	R <sub>L</sub> = ∞		50	60	mA
I <sub>EE</sub>	Negative Supply Current	R <sub>L</sub> = ∞		50	56	mA
	Tri State Supply Current	RST Pin > 2.0V		10	13	mA

**Miscellaneous Performance**

R <sub>IN</sub>	Input Resistance	Non-Inverting		100		kΩ
C <sub>IN</sub>	Input Capacitance	Non-Inverting		1		pF
R <sub>O</sub>	Output Resistance Enabled	Closed Loop, Enabled		300		mΩ
R <sub>O</sub>	Output Resistance Disabled	LMH6580		50		kΩ
		LMH6581	1100	1350	1500	
CMVR	Input Common Mode Voltage Range			±1.3		V
I <sub>O</sub>	Output Current	Sourcing, V <sub>O</sub> = 0 V		±50		mA

**Digital Control**

V <sub>IH</sub>	Input Voltage High		2.0			V
V <sub>IL</sub>	Input Voltage Low				0.8	V
V <sub>OH</sub>	Output Voltage High			>2.0		V
V <sub>OL</sub>	Output Voltage Low			<0.4		V
	Switching Time			15		ns
T <sub>S</sub>	Setup Time			7		ns
T <sub>H</sub>	Hold Time			7		ns

**±5V Electrical Characteristics** (Note 5)

Unless otherwise specified, typical conditions are: T<sub>A</sub> = 25°C, A<sub>V</sub> = +2, V<sub>S</sub> = ±5V, R<sub>L</sub> = 100Ω; **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
<b>Frequency Domain Performance</b>						
SSBW	-3 dB Bandwidth	V <sub>OUT</sub> = 0.5 V <sub>PP</sub> (Note 11)		450		MHz
		LMH6580 V <sub>OUT</sub> = 1 V <sub>PP</sub> , LMH6581 V <sub>OUT</sub> = 2 V <sub>PP</sub> , R <sub>L</sub> = 1 kΩ		500		
LSBW		LMH6580 V <sub>OUT</sub> = 1 V <sub>PP</sub> , LMH6581 V <sub>OUT</sub> = 2 V <sub>PP</sub> , R <sub>L</sub> = 150Ω		450		
GF	0.1 dB Gain Flatness	LMH6580, V <sub>OUT</sub> = 1 V <sub>PP</sub> , LMH6581, V <sub>OUT</sub> = 2 V <sub>PP</sub> , R <sub>L</sub> = 150Ω		100		MHz
DG	Differential Gain	R <sub>L</sub> = 150Ω, 3.58 MHz/4.43 MHz		.05		%
DP	Differential Phase	R <sub>L</sub> = 150Ω, 3.58 MHz/4.43 MHz		.05		deg

**Time Domain Response**

t <sub>r</sub>	Rise Time	LMH6580 2V, Step, 10% to 90%		2.8		ns
		LMH6581 2V, Step, 10% to 90%		1.2		
t <sub>f</sub>	Fall Time	2V Step, 10% to 90%		1.6		ns
OS	Overshoot	2V Step		<1		%

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
SR	Slew Rate	LMH6580, 2 V <sub>pp</sub> , 40% to 60% (Note 6)		1200		V/μs
SR	Slew Rate	LMH6581, 6 V <sub>pp</sub> , 40% to 60% (Note 6)		2100		V/μs
t <sub>s</sub>	Settling Time	2V Step, V <sub>OUT</sub> Within 0.5%		6		ns
<b>Distortion And Noise Response</b>						
HD2	2 <sup>nd</sup> Harmonic Distortion	2 V <sub>pp</sub> , 5 MHz		-80		dBc
HD3	3 <sup>rd</sup> Harmonic Distortion	2 V <sub>pp</sub> , 5 MHz		-70		dBc
e <sub>n</sub>	Input Referred Voltage Noise	>1 MHz		12		nV/√Hz
i <sub>n</sub>	Input Referred Noise Current	>1 MHz		2		pA/√Hz
XTLK	Cross Talk	All Hostile, f = 100 MHz		-45		dBc
		Channel to Channel, f = 100 MHz		-52		dBc
ISOL	Off Isolation	f = 100 MHz		-65		dBc
<b>Static, DC Performance</b>						
A <sub>v</sub>	Gain	LMH6581	1.986	2.00	2.014	
		LMH6580	0.995	1.00	1.005	
V <sub>os</sub>	Input Offset Voltage			±2	±17	mV
TCV <sub>os</sub>	Input Offset Voltage Average Drift	(Note 10)		38		μV/°C
I <sub>B</sub>	Input Bias Current	Non-Inverting (Note 9)		-5	±12	μA
TCI <sub>B</sub>	Input Bias Current Average Drift	Non-Inverting (Note 10)		-12		nA/°C
V <sub>O</sub>	Output Voltage Range	LMH681, R <sub>L</sub> = 100Ω	±3.4	±3.6		V
		LMH6580, R <sub>L</sub> = 100Ω	±2.9	±3.0		
V <sub>O</sub>	Output Voltage Range	LMH6581, R <sub>L</sub> = ∞Ω	±3.7	±3.9		V
		LMH6580, R <sub>L</sub> = ∞Ω	±2.9	±3.0		
PSRR	Power Supply Rejection Ratio	DC	-42	-45		dBc
XTLK	DC Crosstalk Rejection	DC, Channel to Channel	-62	-90		dBc
OISO	DC Off Isolation	DC	-60	-90		dBc
I <sub>CC</sub>	Positive Supply Current	R <sub>L</sub> = ∞		54	66	mA
I <sub>EE</sub>	Negative Supply Current	R <sub>L</sub> = ∞		50	62	mA
	Tri State Supply Current	RST Pin > 2.0V		14	17	mA
<b>Miscellaneous Performance</b>						
R <sub>IN</sub>	Input Resistance	Non-Inverting		100		kΩ
C <sub>IN</sub>	Input Capacitance	Non-Inverting		1		pF
R <sub>O</sub>	Output Resistance Enabled	Closed Loop, Enabled		300		mΩ
R <sub>O</sub>	Output Resistance Disabled	LMH6580, Resistance to Ground		50		kΩ
		LMH6581, Resistance to Ground	1100	1300	1500	
CMVR	Input Common Mode Voltage Range			±3.0		V
I <sub>O</sub>	Output Current	Sourcing, V <sub>O</sub> = 0 V	±60	±70		mA
<b>Digital Control</b>						
V <sub>IH</sub>	Input Voltage High		2.0			V
V <sub>IL</sub>	Input Voltage Low				0.8	V
V <sub>OH</sub>	Output Voltage High			>2.4		V
V <sub>OL</sub>	Output Voltage Low			<0.4		V
	Switching Time			15		ns
T <sub>S</sub>	Setup Time			5		ns
T <sub>H</sub>	Hold Time			5		ns

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

**Note 2:** Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

**Note 3:** The maximum output current ( $I_{OUT}$ ) is determined by device power dissipation limitations.

**Note 4:** The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$ . All numbers apply for packages soldered directly onto a PC Board.

**Note 5:** Electrical Table values apply only for factory testing conditions at the temperature indicated. No guarantee of parametric performance is indicated in the electrical tables under conditions different than those tested.

**Note 6:** Slew Rate is the average of the rising and falling edges.

**Note 7:** Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

**Note 8:** Room Temperature limits are 100% production tested at 25°C. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

**Note 9:** Negative input current implies current flowing out of the device.

**Note 10:** Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

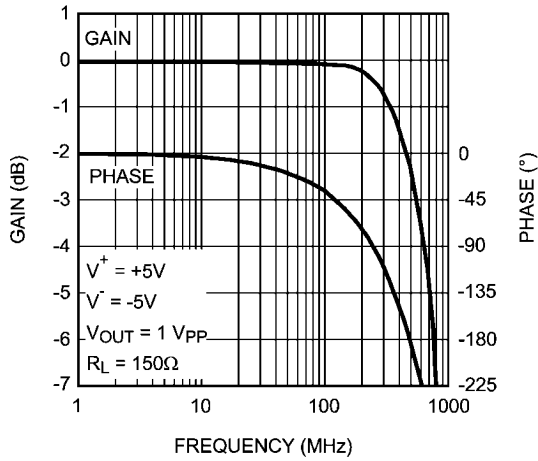
**Note 11:** This parameter is guaranteed by design and/or characterization and is not tested in production.

## Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
48-Pin QFP	LMH6580VS	LMH6580VS	250 Units/Tray	VBC48A
	LMH6581VS	LMH6581VS	250 Units/Tray	

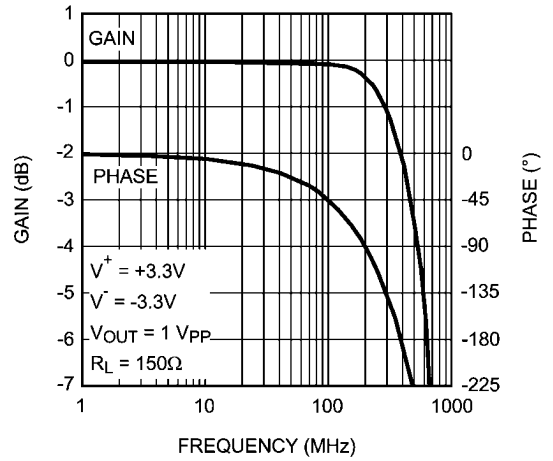
# Typical Performance Characteristics LMH6580

1 V<sub>PP</sub> Frequency Response



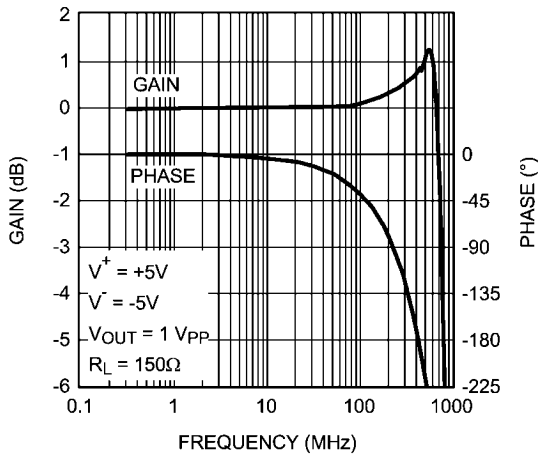
30007253

1 V<sub>PP</sub> Frequency Response



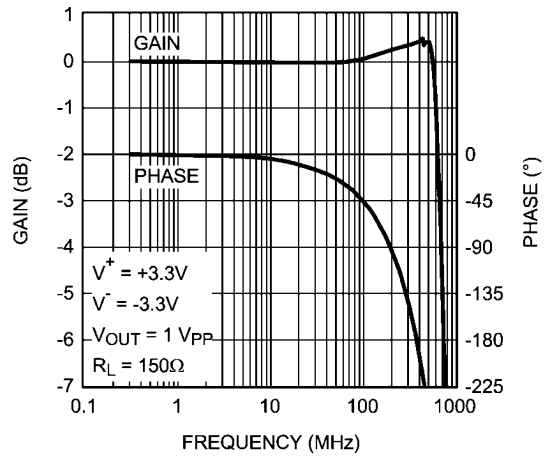
30007254

1 V<sub>PP</sub> Frequency Response Broadcast



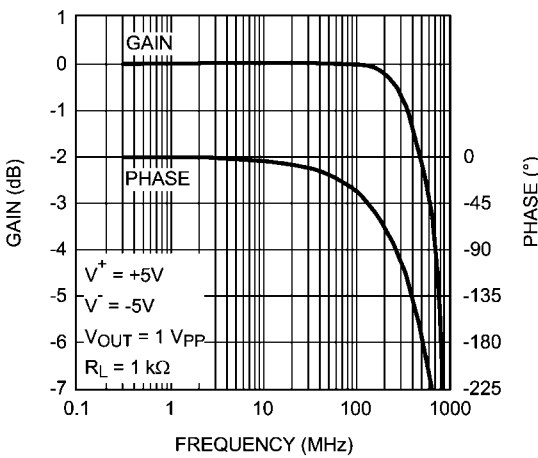
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1 V<sub>PP</sub> Frequency Response Broadcast



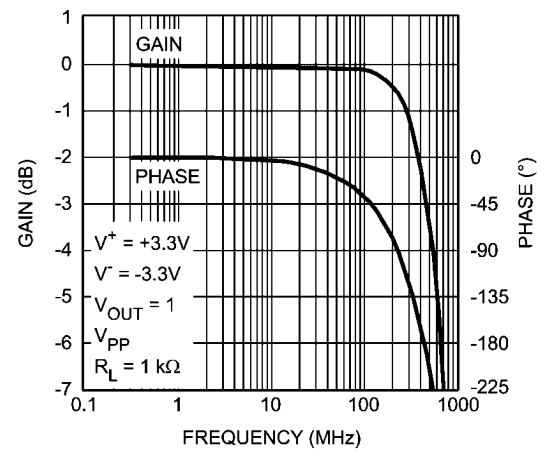
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Frequency Response 1 kΩ Load



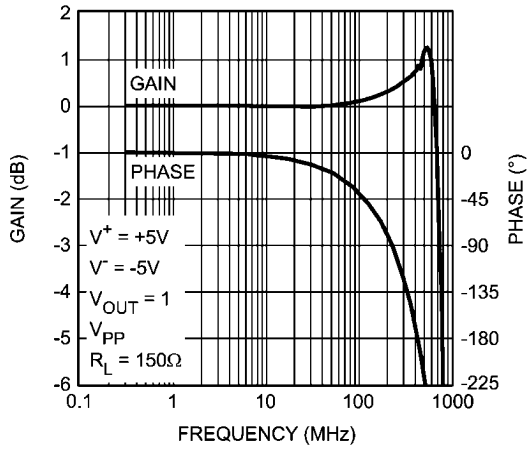
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Frequency Response 1kΩ Load



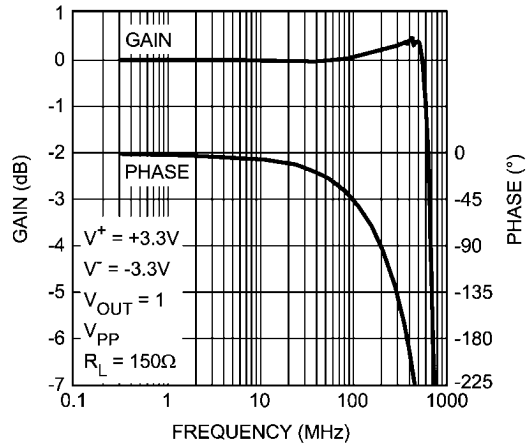
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Frequency Response with Input Expansion



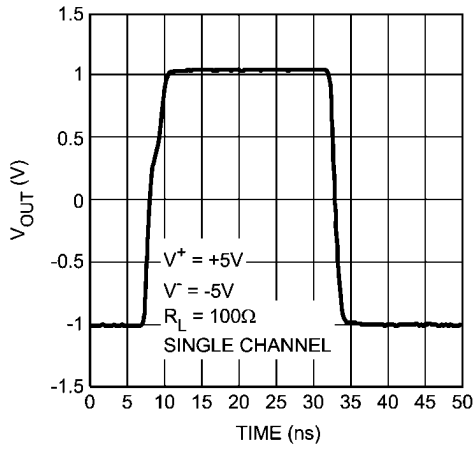
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Frequency Response with Input Expansion



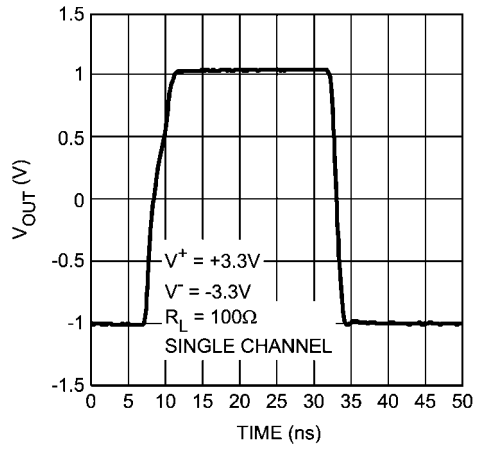
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2 V<sub>pp</sub> Pulse Response



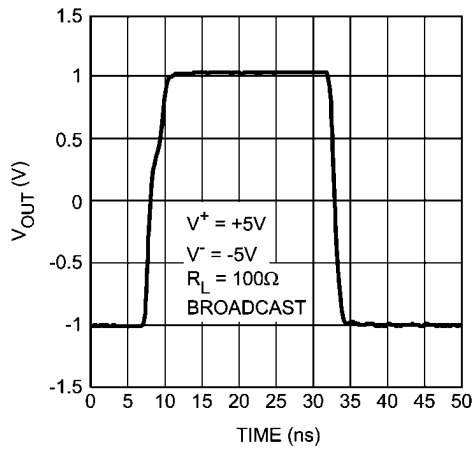
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2 V<sub>pp</sub> Pulse Response



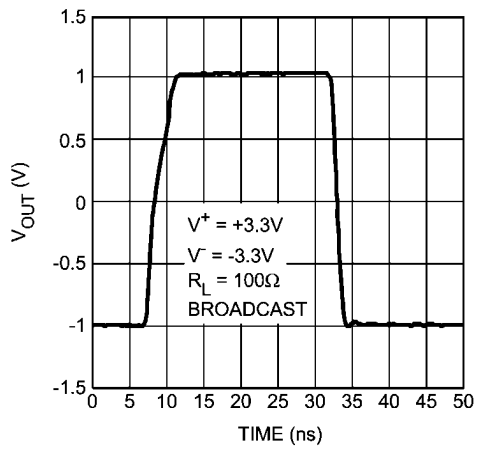
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2 V<sub>pp</sub> Pulse Response, Broadcast Mode



30007258

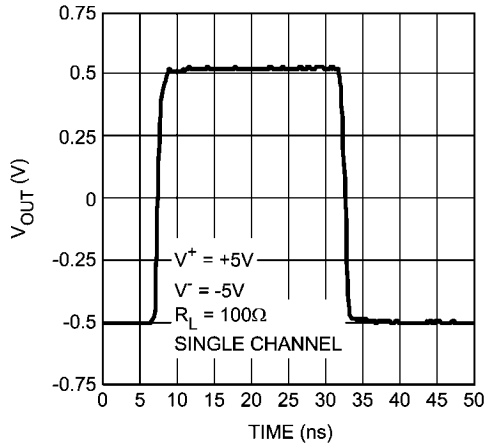
2 V<sub>pp</sub> Pulse Response, Broadcast Mode



30007264

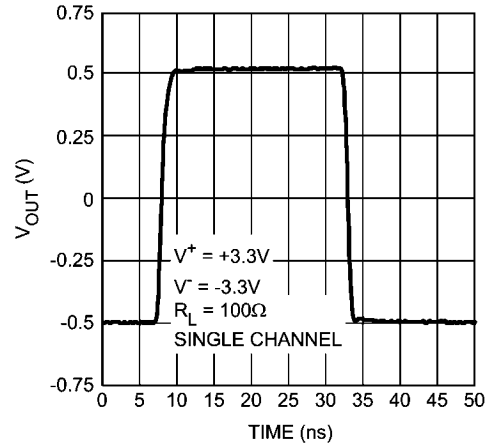


1 V<sub>PP</sub> Pulse Response



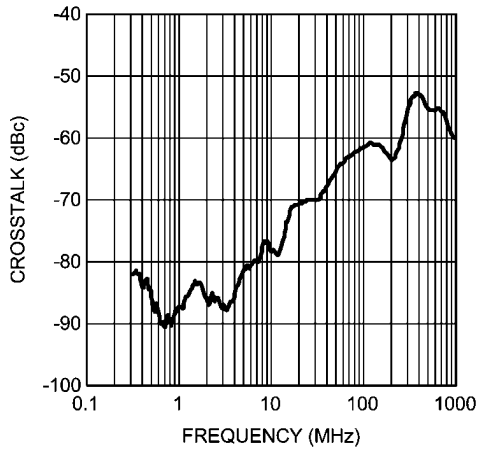
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1 V<sub>PP</sub> Pulse Response



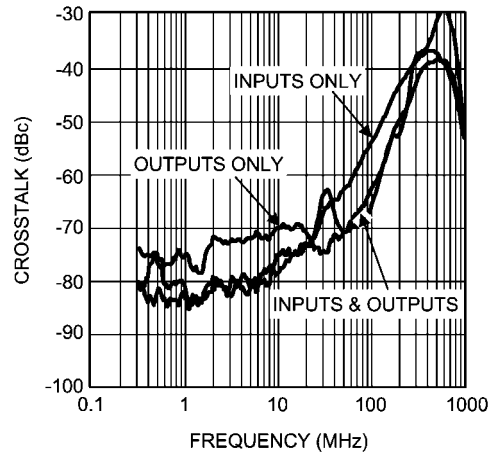
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Channel to Channel Crosstalk



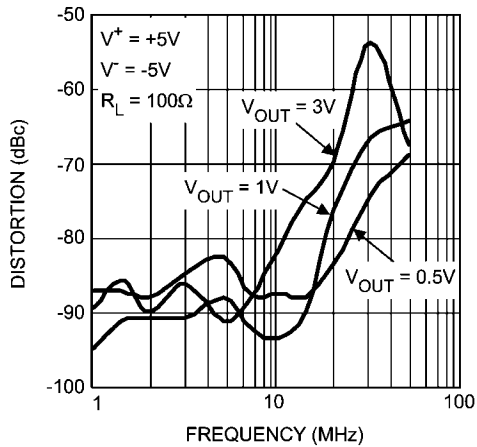
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All Hostile Crosstalk



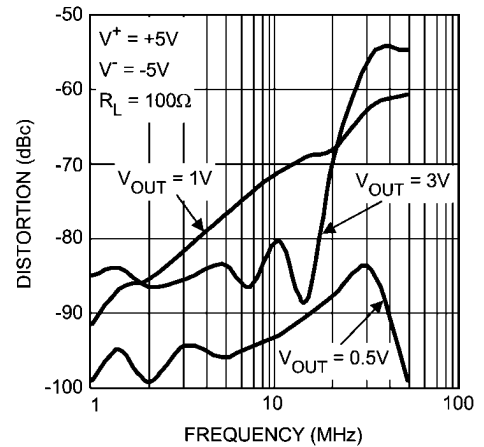
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Second Order Distortion (HD2) vs. Frequency



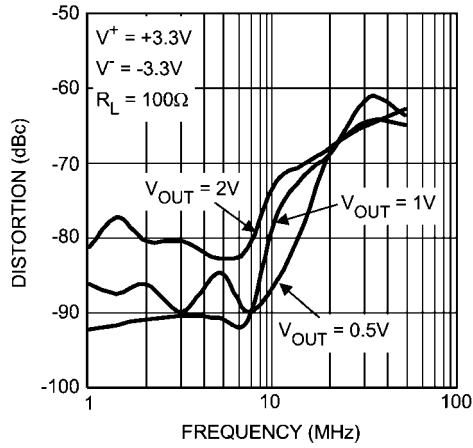
30007272

Third Order Distortion (HD3) vs. Frequency

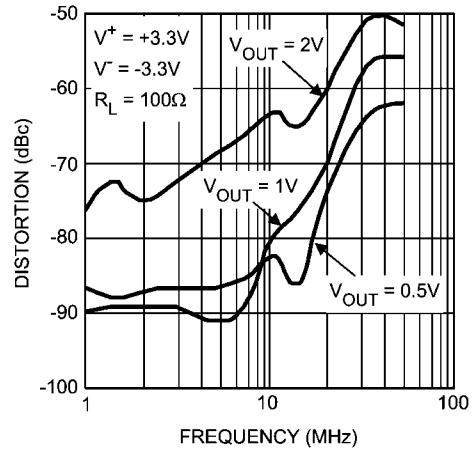


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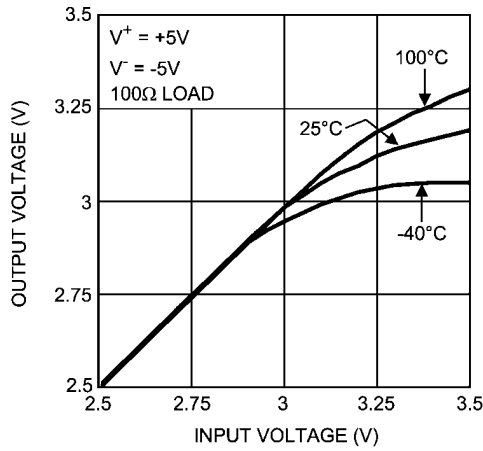
**Second Order Distortion (HD2) vs. Frequency**



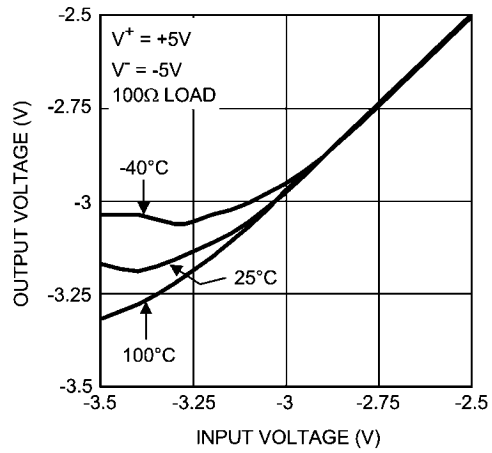
**Third Order Distortion (HD3) vs. Frequency**



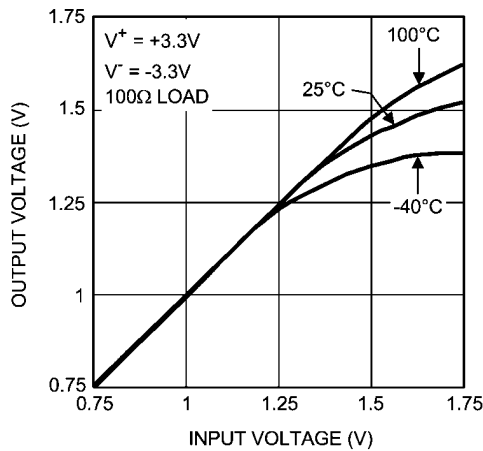
**Positive Voltage Swing over Temperature**



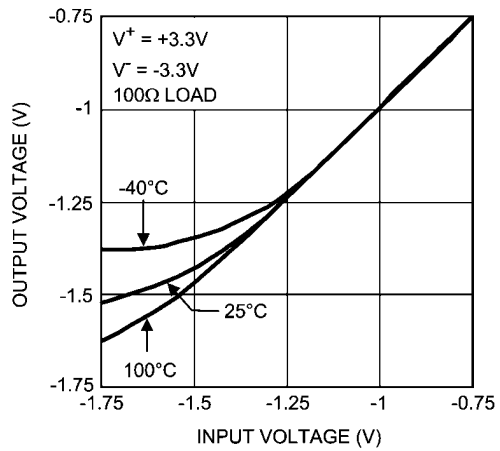
**Negative Voltage Swing over Temperature**



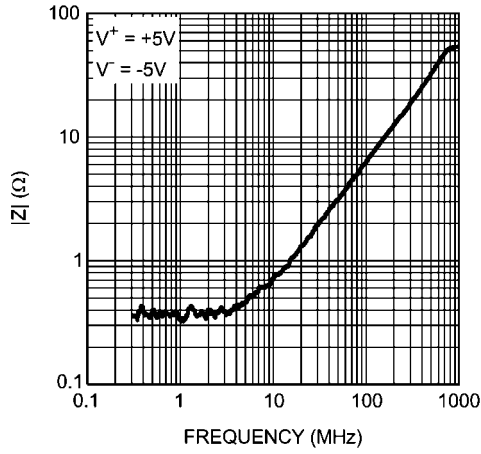
**Positive Voltage Swing over Temperature**



**Negative Voltage Swing over Temperature**

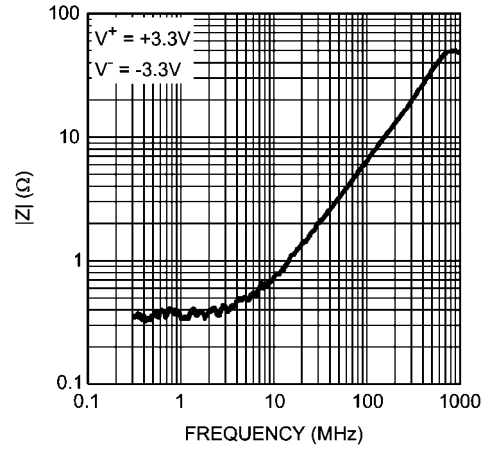


Enabled Output Impedance



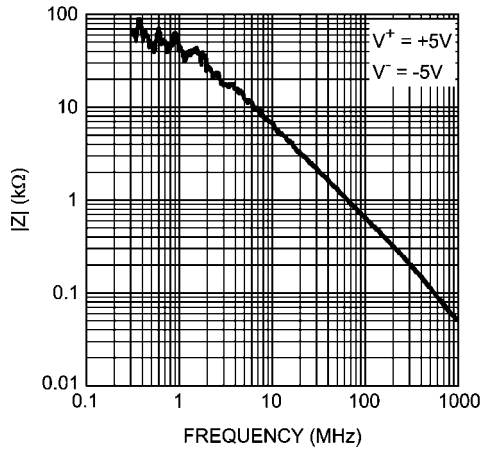
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Enabled Output Impedance



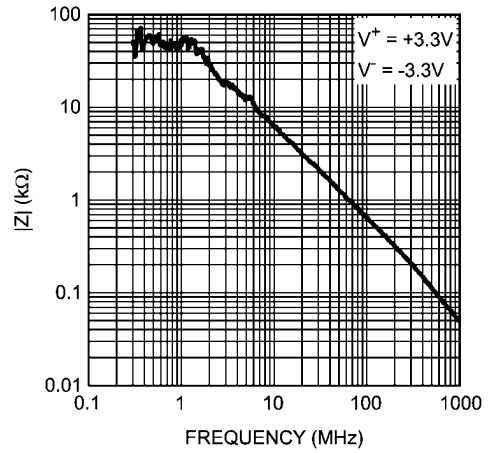
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Disabled Output Impedance



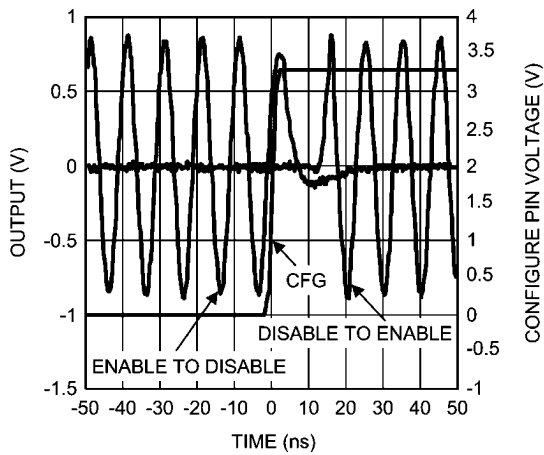
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Disabled Output Impedance



30007280

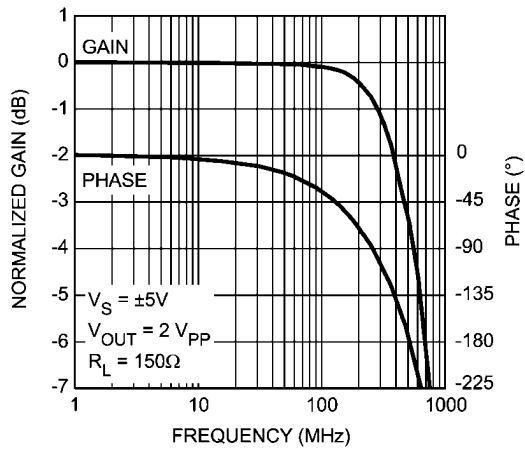
Switching Time



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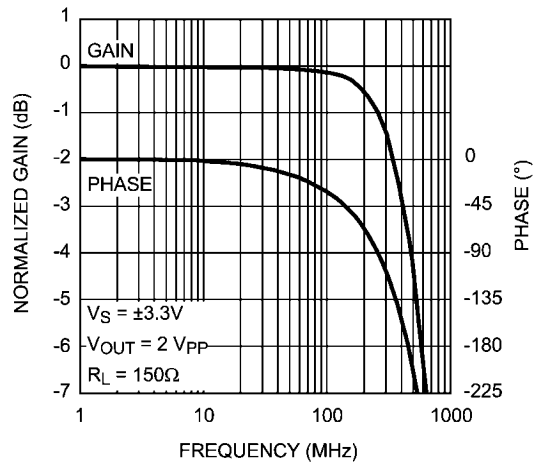
# Typical Performance Characteristics LMH6581

2 V<sub>PP</sub> Frequency Response



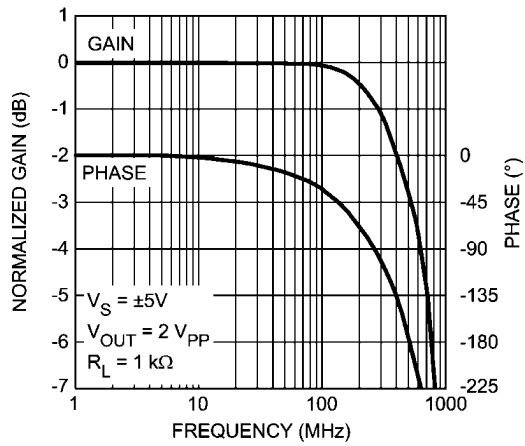
30007248

2 V<sub>PP</sub> Frequency Response



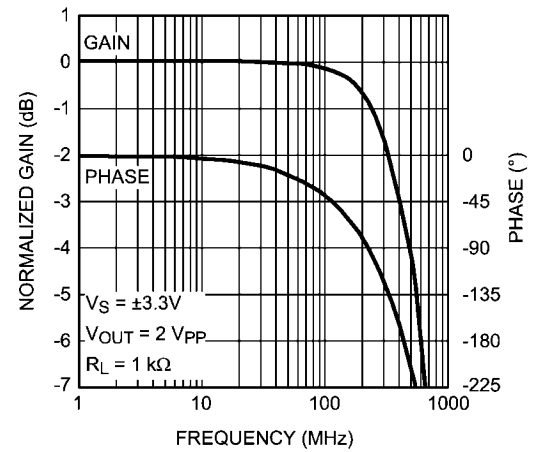
30007249

Large Signal Bandwidth



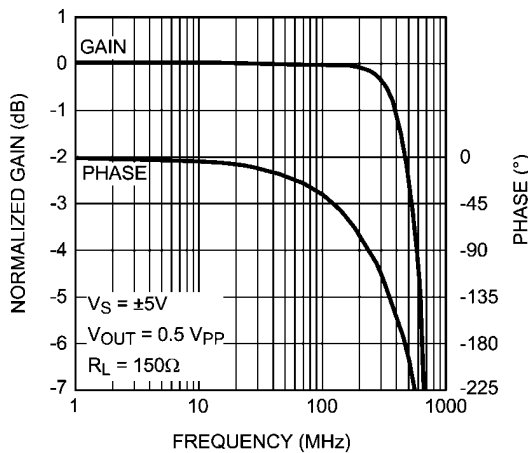
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Large Signal Bandwidth



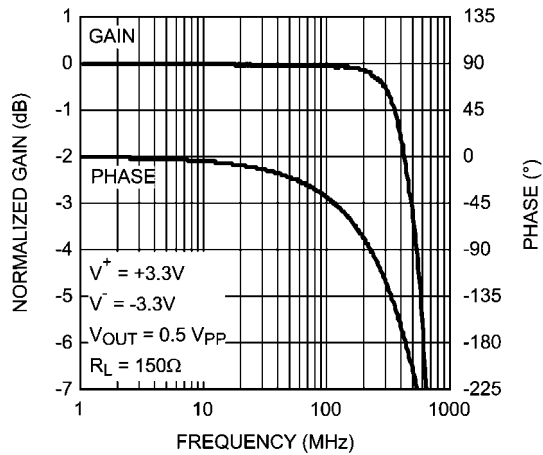
30007223

Small Signal Bandwidth



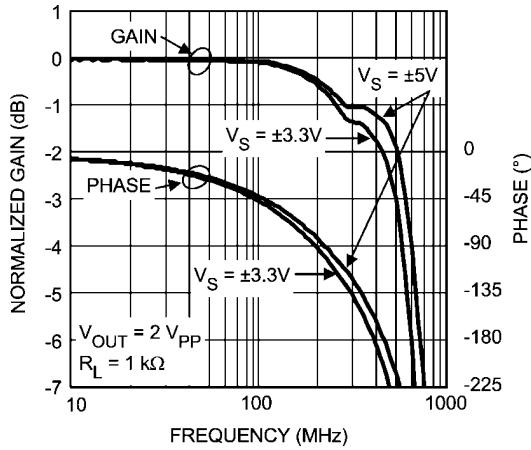
30007224

Small Signal Bandwidth

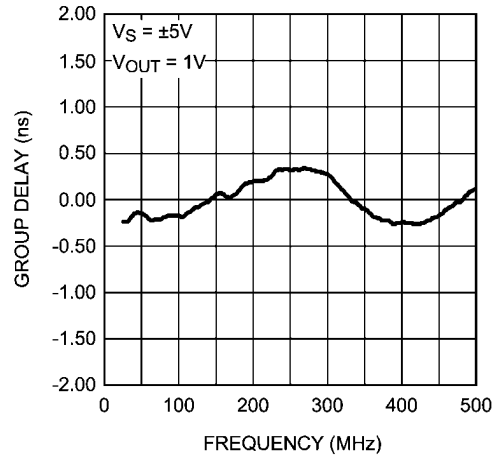


30007225

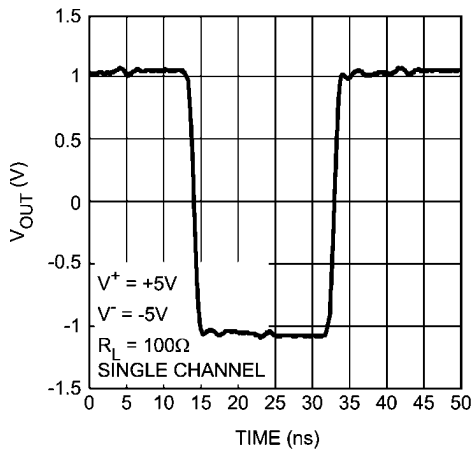
Frequency Response 1 kΩ Load



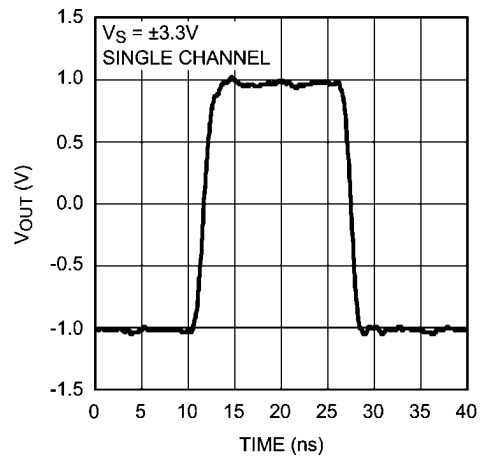
Group Delay



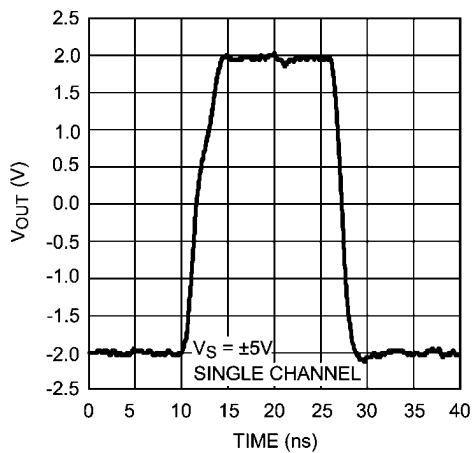
2 V<sub>PP</sub> Pulse Response



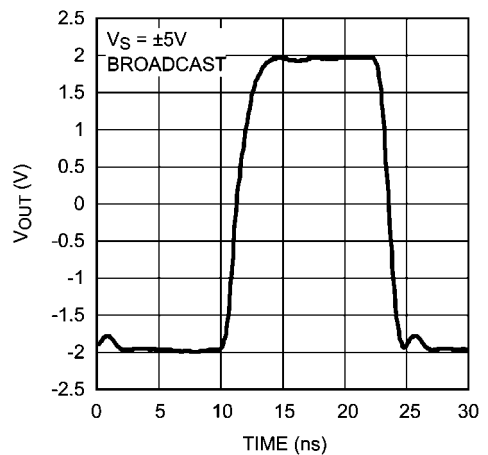
2 V<sub>PP</sub> Pulse Response

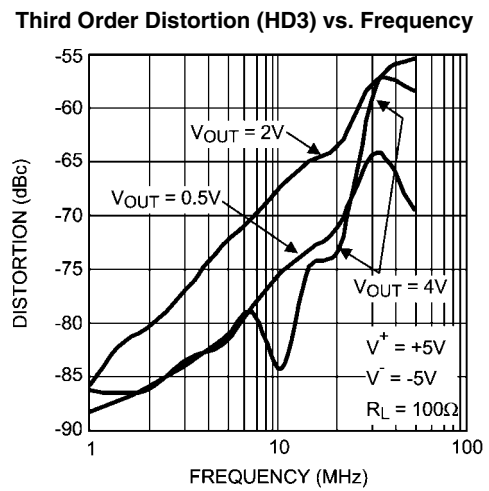
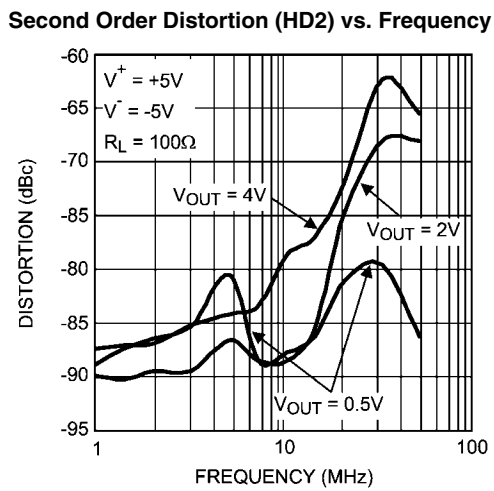
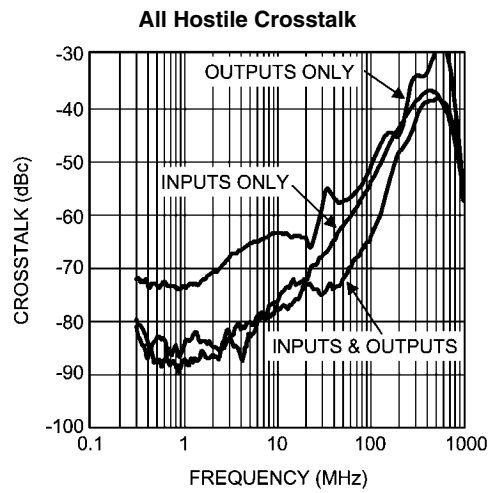
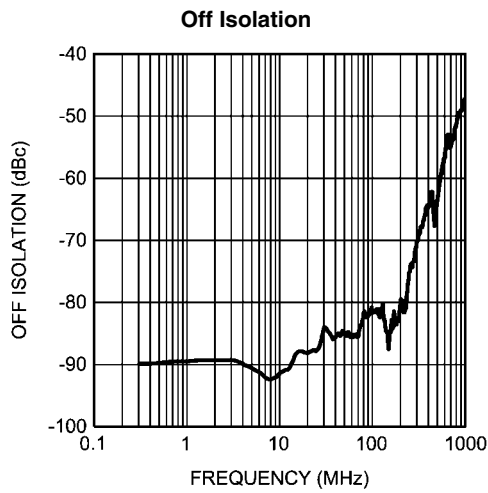
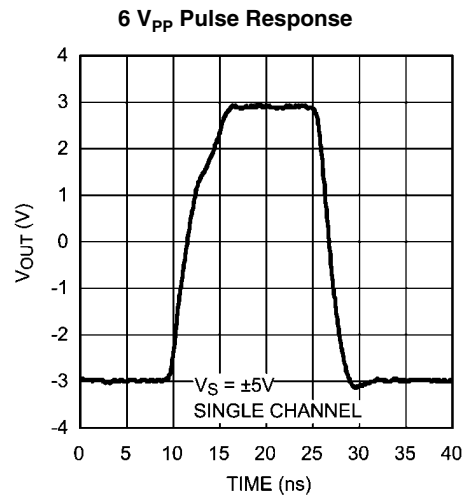
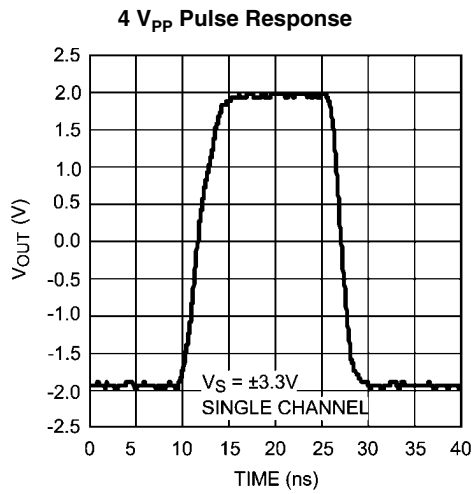


4 V<sub>PP</sub> Pulse Response

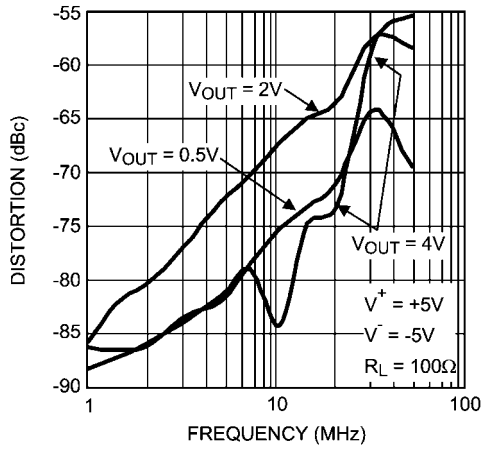


4 V<sub>PP</sub> Pulse Response Broadcast

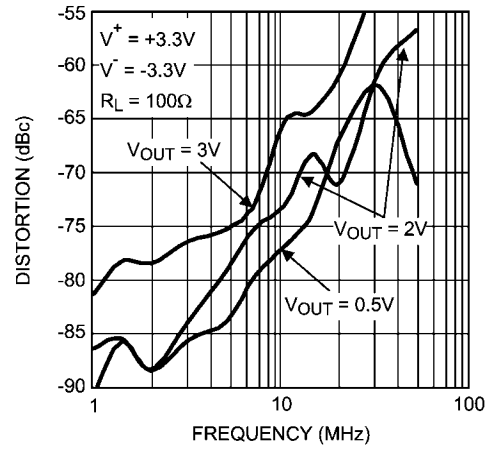




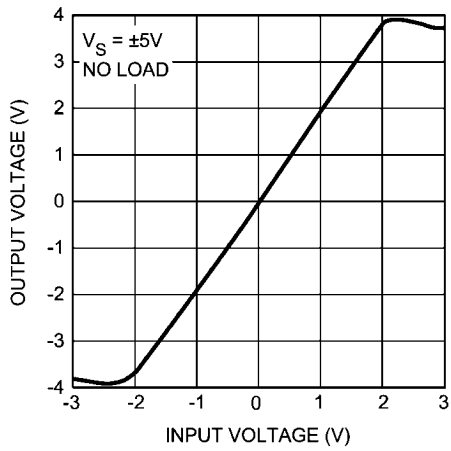
Second Order Distortion vs. Frequency



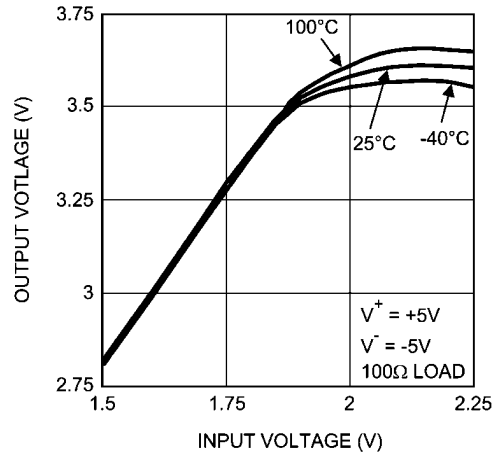
Third Order Distortion vs. Frequency



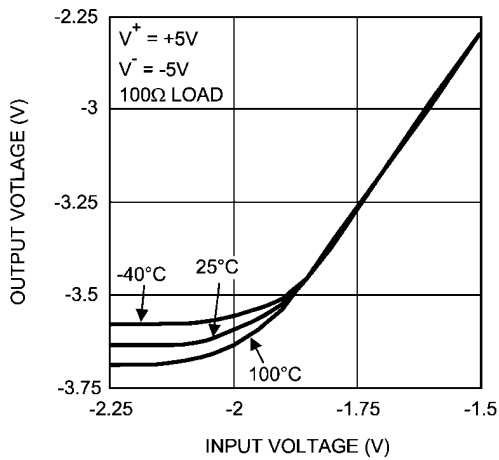
No Load Output Swing



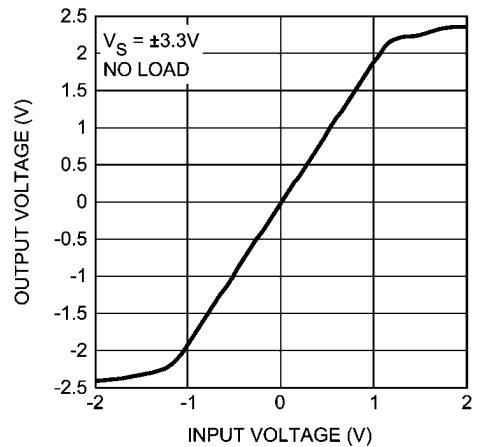
Positive Swing over Temperature



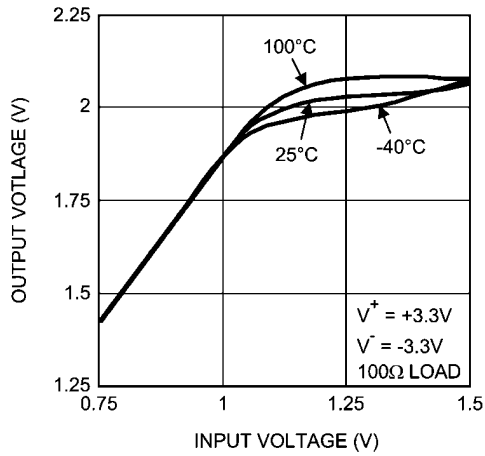
Negative Swing Over Temperature



No Load Output Swing

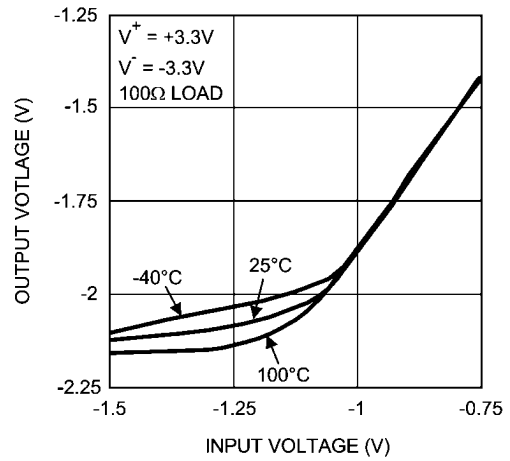


**Positive Swing over Temperature**



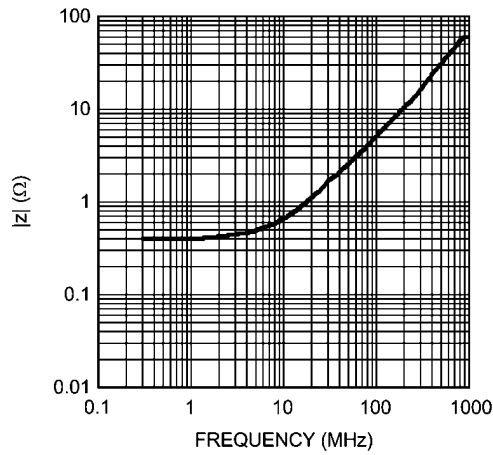
30007236

**Negative Swing over Temperature**



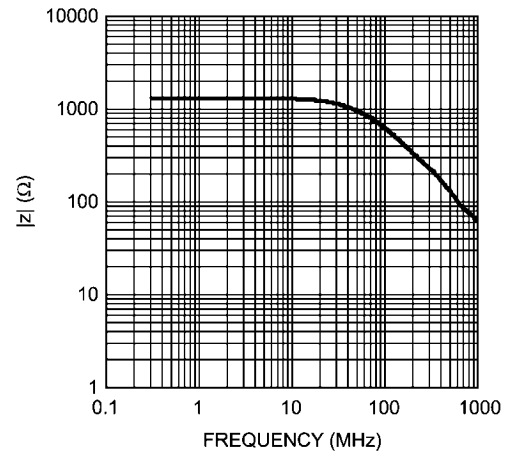
30007237

**Enabled Output Impedance**



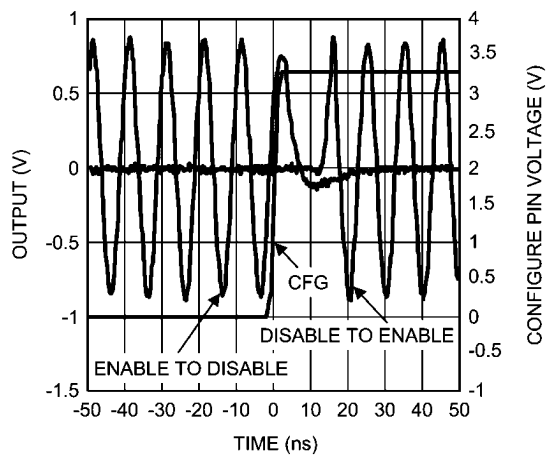
30007250

**Disabled Output Impedance**



30007251

**Switching Time**



30007257



## Application Information

### INTRODUCTION

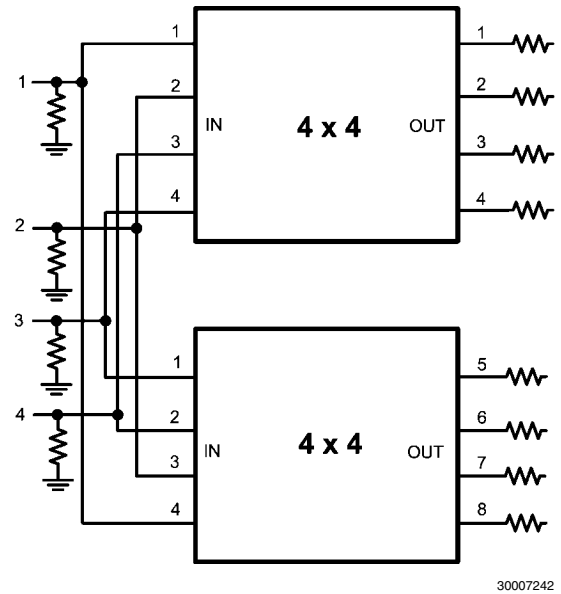
The LMH6580/LMH6581 are high speed, fully buffered, non-blocking, analog crosspoint switches. Having fully buffered inputs allows the LMH6580/LMH6581 to accept signals from low or high impedance sources without the worry of loading the signal source. The fully buffered outputs will drive 75Ω or 50Ω back terminated transmission lines with no external components other than the termination resistor. When disabled, the outputs are in a high impedance state. The LMH6580/LMH6581 can have any input connected to any (or all) output (s). Conversely, a given output can have only one associated input.

### INPUT AND OUTPUT EXPANSION

The LMH6580/LMH6581 have high impedance inactive states for both inputs and outputs allowing maximum flexibility for crosspoint expansion. In addition the LMH6580/LMH6581 employ diagonal symmetry in pin assignments. The diagonal symmetry makes it easy to use direct pin to pin vias when the parts are mounted on opposite sides of a board. As an example two LMH6580/LMH6581 chips can be combined on one board to form either an 8 x 8 crosspoint or a 16 x 4 crosspoint. To make an 8 x 8 crosspoint all 8 input pins would be tied together (Input 0 on side 1 to input 7 on side 2 and so on) while the 4 output pins on each chip would be left separate. To make the 16 x 4 crosspoint, the 4 outputs would be tied together while all 16 inputs would remain independent. In the 16 x 4 configuration it is important not to have 2 connected outputs active at the same time. With the 8 x 8 configuration, on the other hand, having two connected inputs active is a valid state. Crosspoint expansion as detailed above has the advantage that the signal will go through only one crosspoint. Expansion methods that have cascaded stages will suffer bandwidth loss far greater than the small loading effect of parallel expansion.

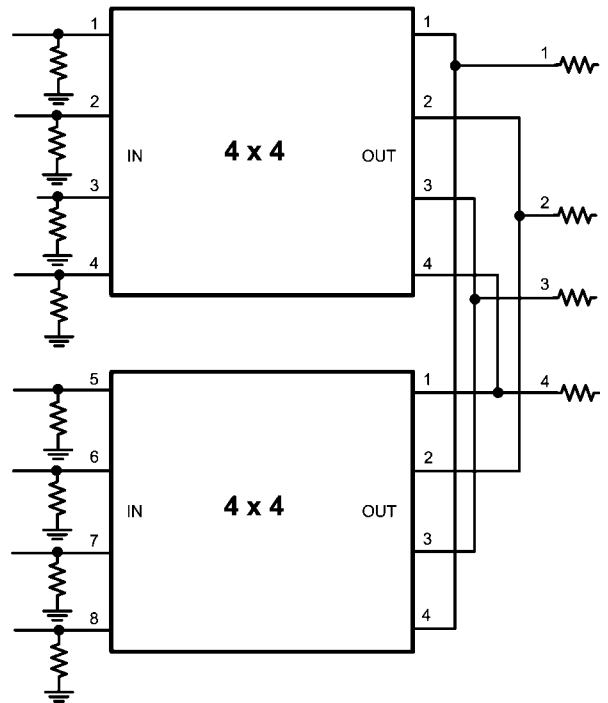
Output expansion as shown in *Figure 1* is very straight forward. Connecting the inputs of two crosspoint switches has a very minor impact on performance. Input expansion requires more planning. Input expansion, as show in *Figure 2* and *Figure 3* gives the option of two ways to connect the outputs of the crosspoint switches. In *Figure 2* the crosspoint switch outputs are connected directly together and share one termination resistor. This is the easiest configuration to implement and has only one drawback. Because the disabled output of the unused crosspoint (only one output can be active at a time) has a small amount of capacitance, the frequency response of the active crosspoint will show peaking. This is illustrated in *Figure 4* and *Figure 5*. In most cases this small amount of peaking is not a problem.

As illustrated in *Figure 3* each crosspoint output can be given its own termination resistor. This results in a frequency response nearly identical to the non expansion case. There is one drawback for the gain of 2 crosspoint, and that is gain error. With a 75Ω termination resistor the 1250Ω resistance of the disabled crosspoint output will cause a gain error. In order to counter act this the termination resistors of both crosspoints should be adjusted to approximately 80Ω. This will provide very good matching, but the gain accuracy of the system will now be dependent on the process variations of the crosspoint resistors which have a variability of approximately ±20%.



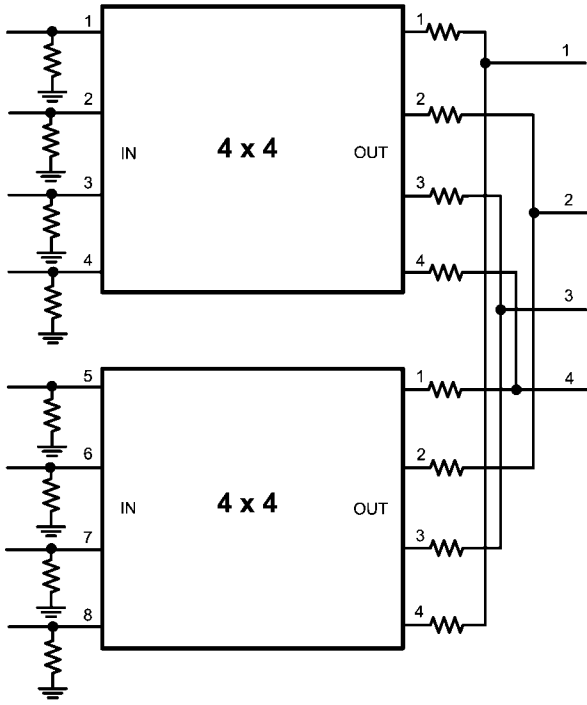
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FIGURE 1. Output Expansion



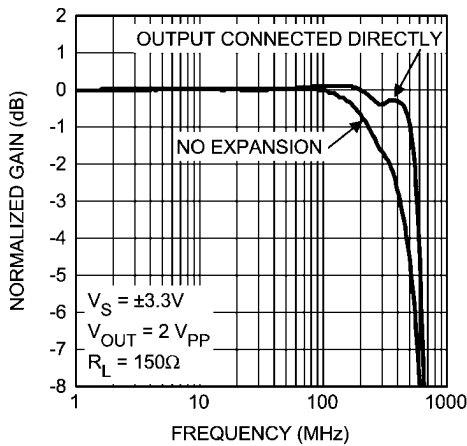
30007243

FIGURE 2. Input Expansion with Shared Termination Resistors



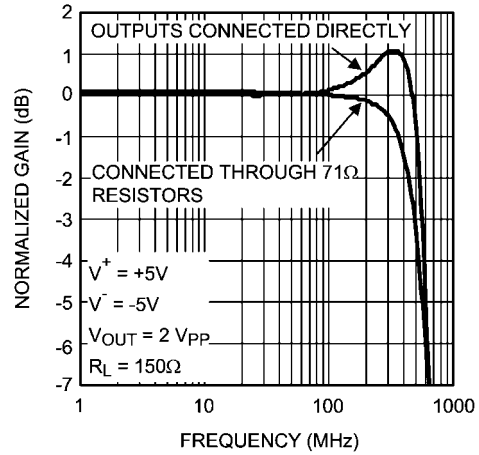
30007244

FIGURE 3. Input Expansion with Separate Termination Resistors



30007246

FIGURE 4. Input Expansion Frequency Response



30007247

FIGURE 5. Input Expansion Frequency Response

**DRIVING CAPACITIVE LOADS**

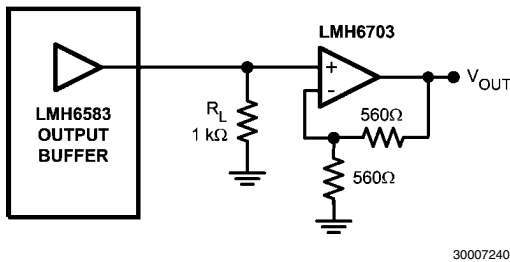
Capacitive output loading applications will benefit from the use of a series output resistor  $R_{OUT}$ . Capacitive loads of 5 pF to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. Since most capacitive loading is due to undesired parasitic capacitances the values of the capacitive loading will not usually be known exactly. It is best to start with a conservative value of  $R_{OUT}$  and decrease the value until the bandwidth shows slight peaking. At this point the value of the isolation resistor will be determined by whether flat frequency response or maximum bandwidth is the desired goal. Smaller values of  $R_{OUT}$  will produce some peaking, but maximum bandwidth. Larger resistor values will decrease bandwidth and suppress peaking.

As starting values, a capacitive load of 5 pF should have around 75  $\Omega$  of isolation resistance. A value of 120 pF would require around 12  $\Omega$ . When driving transmission lines, the output termination resistor is normally sufficient.

**USING OUTPUT BUFFERING TO ENHANCE BANDWIDTH AND INCREASE REBIABILITY**

The LMH6580/LMH6581 crosspoint switch can offer enhanced bandwidth and reliability with the use of external buffers on the outputs. The bandwidth is increased by unloading the outputs and driving the high impedance of an external buffer. See the **Frequency Response 1 kΩ Load** curve in the Typical Performance section for an example of bandwidth achieved with less loading on the outputs. For this technique to provide maximum benefit a very high speed amplifier such as the LMH6703 should be used. As shown in *Figure 6* the resistor  $R_L$  is placed between the crosspoint output and the buffer amplifier. This resistor will provide a load for the crosspoint output buffer and reduce peaking caused by the buffer input capacitance. A recommended value for  $R_L$  is 500Ω to 1000Ω. Higher values of  $R_L$  will give higher bandwidth, but also higher peaking. The optimum value of  $R_L$  will depend greatly on board layout and the input capacitance of the buffer amplifier.

Besides offering enhanced bandwidth performance using an external buffer provides greater system reliability. The first advantage is to reduce thermal loading on the crosspoint switch. This reduced die temperature will increase the life of the crosspoint. The second advantage is enhanced ESD reliability. It is very difficult to build high speed devices that can withstand all possible ESD events. With external buffers the crosspoint switch is isolated from ESD events on the external system connectors.

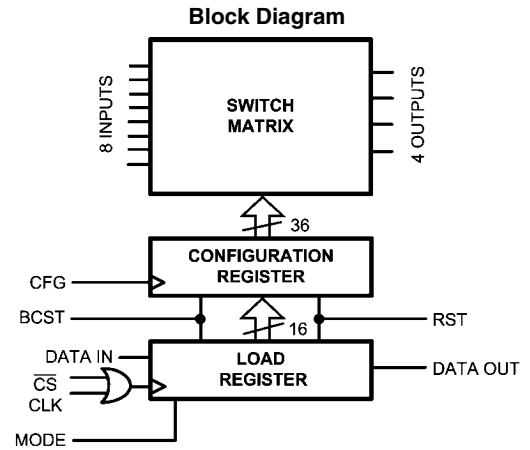


**FIGURE 6. Buffered Output**

**CROSSTALK**

When designing a large system such as a video router crosstalk can be a very serious problem. Extensive testing in our lab has shown that most crosstalk is related to board layout rather than occurring in the crosspoint switch. There are many ways to reduce board related crosstalk. Using controlled impedance lines is an important step. Using well decoupled power and ground planes will help as well. When crosstalk does occur within the crosspoint switch itself it is often due to signals coupling into the power supply pins. Using appropriate supply bypassing will help to reduce this mode of coupling. Another suggestion is to place as much grounded copper as possible between input and output signal traces. Care must be taken, though, not to influence the signal trace impedances by placing shielding copper too closely. One other caveat to consider is that as shielding materials come closer to the signal trace the trace needs to be smaller to keep the impedance from falling too low. Using thin signal traces will result in unacceptable losses due to trace resistance. This effect becomes even more pronounced at higher frequencies due to the skin effect. The skin effect reduces the effective thickness of the trace as frequency increases. Resistive losses make crosstalk worse because as the desired signal is attenuated with higher frequencies crosstalk increases at higher frequencies.

**DIGITAL CONTROL**



**FIGURE 7.**

**Logic Pins**

Pin Name	Level Sensitive	Edge Triggered	Triggered by
CLK	Yes		
CS		Yes	CLK rising edge
DATA IN		Yes	CLK falling edge
DATA OUT		Yes	CLK rising edge
CFG	Yes		
MODE	Yes		
RST	Yes		
BCST	Yes		

There are two modes for programming the LMH6580/LMH6581, Serial Mode and Addressed Mode. The LMH6580/LMH6581 have internal control registers that store the programming states of the crosspoint switch. The logic is two staged to allow for maximum programming flexibility. The first stage of the control logic is tied directly to the crosspoint switching matrix. This logic consists of one register for each output that stores the on/off state and the address of which input to connect to. These registers are not directly accessible to the user. The second level of logic is another bank of registers identical to the first, but set up as shift registers. These registers are accessed by the user via the serial input bus.

The LMH6580/LMH6581 is programmed via a serial input bus with the support of four other digital control pins. The Serial bus consists of a clock pin (CLK), a serial data in pin (DIN), and a serial data out pin (DOUT). The serial bus is gated by a chip select pin (CS). The chip select pin is active low. While the chip select pin is high all data on the serial input pin and clock pins is ignored. When the chip select pin is brought low the internal logic is set to begin receiving data by the first positive transition (0 to 1) of the clock signal. The chip select pin must be brought low at least 5 ns before the first rising edge of the clock signal. The first data bit is clocked in on the next negative transition (1 to 0) of the clock signal. All input data is read from the bus on the negative edge of the clock signal. Once the last valid data has been clocked in, either the

chip select pin must go high or, the clock signal must stop. Otherwise invalid data will be clocked into the chip. The data clocked into the chip is not transferred to the crosspoint matrix until the CFG pin is pulsed high. This is the case regardless of the state of the MODE pin. The CFG pin is not dependent on the state of the Chip select pin. If no new data is clocked into the chip subsequent pulses on the CFG pin will have no effect on device operation.

The programming format of the incoming serial data is selected by the MODE pin. When the MODE pin is HIGH the crosspoint can be programmed one output at a time by entering a string of data that contains the address of the output that is going to be changed (Addressed Mode). When the mode pin is LOW the crosspoint is in Serial Mode. In this mode the crosspoint accepts a 16 bit array of data that programs all of the outputs. In both modes the data fed into the chip does not change the chip operation until the Configure pin is pulsed high. The configure and mode pins are independent of the chip select pin.

**THREE WIRE VS. FOUR WIRE CONTROL**

There are two ways to connect the serial data pins. The first way is to control all four pins separately, and the second option is to connect the CFG and the CS pins together for a 3 wire interface. The benefit of the 4-wire interface is that the chip can be configured independently using the CS pin. This would be an advantage in a system with multiple crosspoint chips where all of them could be programmed ahead of time and then configured simultaneously. The 4-wire solution is also helpful in a system that has a free running clock on the CLK pin. In this case, the CS pin needs to be brought high after the last valid data bit to prevent invalid data from being clocked into the chip.

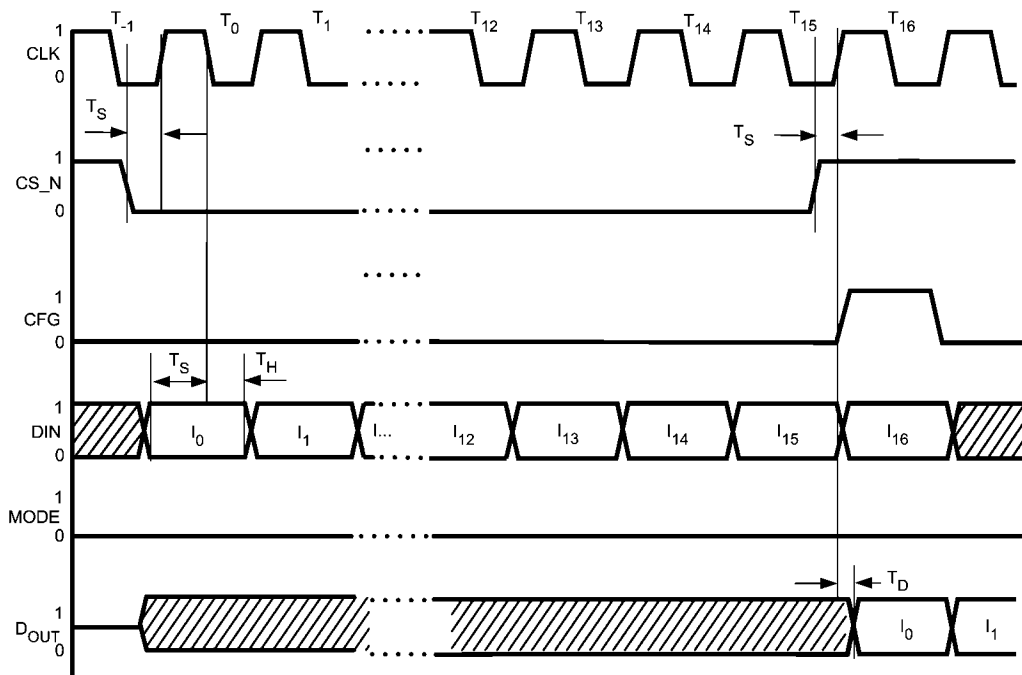
The 3-wire option provides the advantage of one less pin to control at the expense of having less flexibility with the con-

figure pin. One way around this loss of flexibility would be if the clock signal is generated by an FPGA or microcontroller where the clock signal can be stopped after the data is clocked in. In this case the Chip select function is provided by the presence or absence of the clock signal.

**SERIAL PROGRAMMING MODE**

Serial programming mode is the mode selected by bringing the MODE pin low. In this mode a stream of 16-bits programs all four outputs of the crosspoint. The data is fed to the chip as shown in the Serial Mode Data Frame tables below (two tables are required to show the entire data frame). The table is arranged such that the first bit clocked into the crosspoint register is labeled bit number 0. The register labeled Load Register in the block diagram is a shift register. If the chip select pin is left low after the valid data is shifted into the chip and if the clock signal keeps running then additional data will be shifted into the register, and the desired data will be shifted out.

Also illustrated is the timing relationships for the digital pins in the Timing Diagram for Serial Mode shown below. It is important to note that all the pin timing relationships are important, not just the data and clock pins. One example is that the Chip Select pin (CS) must transition low before the first rising edge of the clock signal. This allows the internal timing circuits to synchronize to allow data to be accepted on the next falling edge. The chip select pin must then transition high after the final data bit has been clocked in and before another clock signal positive edge occurs to prevent invalid data from being clocked into the chip. Another way to accomplish the same thing is to strobe the clock pin with only the desired number of pulses starting and ending with clock in the low condition. The configure (CFG) pin timing is not so critical, but it does need to be kept low until all data has been shifted into the crosspoint registers.



Timing Diagram for Serial Mode

30007209

## Serial Mode Data Frame (First Two Words)

Output 0				Output 1			
Input Address			On = 0	Input Address			On = 0
LSB		MSB	Off = 1	LSB	LSB		Off = 1
0	1	2	3	4	5	6	7

Off = TRI-STATE®, Bit 0 is first bit clocked into device.

## Serial Mode Data Frame (Continued)

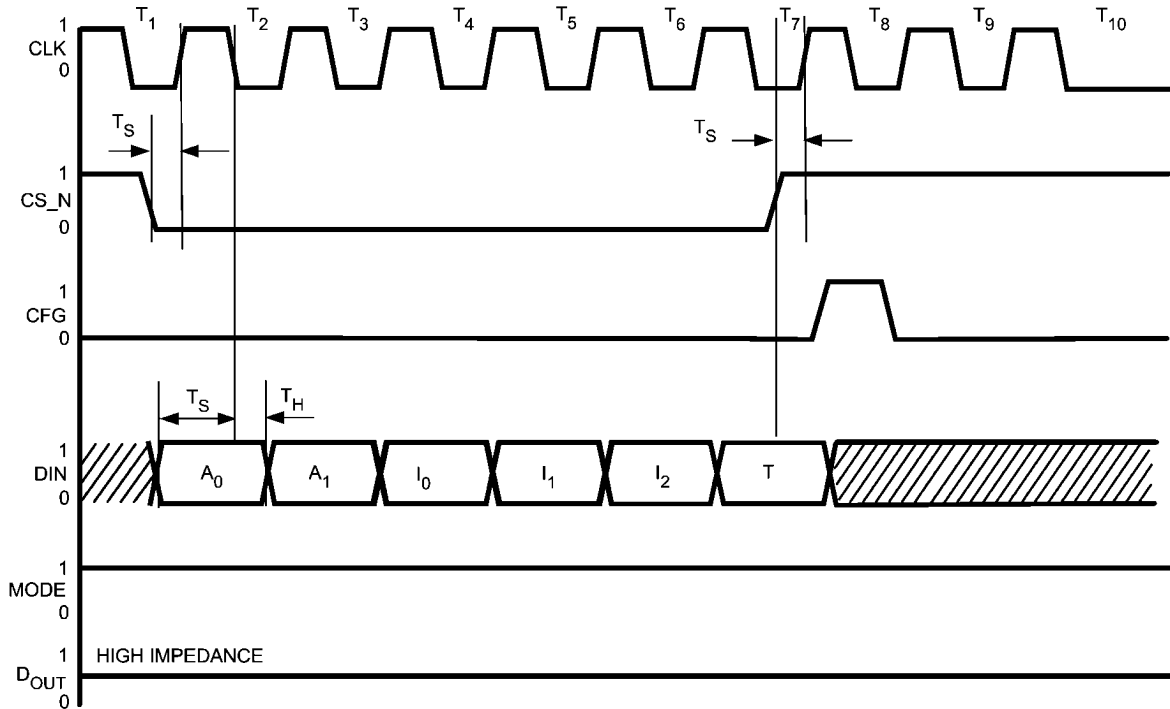
Output 2				Output 3			
Input Address			On = 0	Input Address			On = 0
LSB		MSB	Off = 1	LSB		MSB	Off = 1
8	9	10	11	12	13	14	15

### ADDRESSED PROGRAMMING MODE

Addressed programming mode makes it possible to change only one output register at a time. To utilize this mode the mode pin must be High. All other pins function the same as in serial programming mode except that the word clocked in is 5 bits and is directed only at the output specified. In addressed mode the data format is shown below in the table titled Addressed Mode Word Format.

Also illustrated is the timing relationships for the digital pins in the Timing Diagram for Addressed Mode shown below. It is important to note that all the pin timing relationships are important, not just the data and clock pins. One example is that the Chip Select pin (CS) must transition low before the

first rising edge of the clock signal. This allows the internal timing circuits to synchronize to allow data to be accepted on the next falling edge. The chip select pin must then transition high after the final data bit has been clocked in and before another clock signal positive edge occurs to prevent invalid data from being clocked into the chip. Also, in addressed mode is it necessary for the clock signal to make a low to high transition after the chip select pin has been brought high. If there is not a low to high transition of the clock after the chip select pin goes high subsequent data will not be loaded into the chip properly. The configure (CFG) pin timing is not critical, but it does need to be kept low until all data has been shifted into the crosspoint registers.



Timing Diagram for Addressed Mode

30007210

## Addressed Mode Word Format

Output Address		Input Address			TRI-STATE
LSB	MSB	LSB		MSB	1 = TRI-STATE 0 = On
0	1	2	3	4	5

Bit 0 is first bit clocked into device.

### DAISY CHAIN OPTION IN SERIAL MODE

The LMH6580/LMH6581 supports daisy chaining of the serial data stream between multiple chips. This feature is available only in the Serial Programming Mode. To use this feature serial data is clocked into the first chip  $D_{IN}$  pin, and the next chip  $D_{IN}$  pin is connected to the  $D_{OUT}$  pin of the first chip. Both chips may share a chip select signal, or the second chip can be enabled separately. When the chip select pin goes low on both chips a double length word is clocked into the first chip. As the first word is clocking into the first chip the second chip is receiving the data that was originally in the shift register of the first chip (invalid data). When a full 16 bits have been clocked into the first chip the next clock cycle begins moving the first frame of the new configuration data into the second chip. With a full 32 clock cycles both chips have valid data and the chip select pin of both chips should be brought high to prevent the data from overshooting. A configure pulse will activate the new configuration on both chips simultaneously, or each chip can be configured separately. The mode, chip select, configure and clock pins of both chips can be tied together and driven from the same sources.

### SPECIAL CONTROL PINS

The LMH6580/LMH6581 have two special control pins that function independent of the serial control bus. One of these pins is the reset (RST) pin. The RST pin is active high meaning that at logic 1 level the chip is configured with all outputs disabled and in a high impedance state. The RST pin programs all the registers with input address 0 and all the outputs are turned off. In this configuration the device draws only 11-mA. The RST pin can be used as a shutdown function to reduce power consumption. The other special control pin is the broadcast (BCST) pin. The BCST pin is also active high and sets all the outputs to the on state connected to input 0. This is sometimes referred to as broadcast mode, where input 0 is broadcast to all eight outputs.

### THERMAL MANAGEMENT

The LMH6580/LMH6581 are high performance devices that produce a significant amount of heat. With  $\pm 5V$  supplies, the LMH6580/LMH6581 will dissipate approximately 0.5 W of idling power with all outputs enabled. Idling power is calcu-

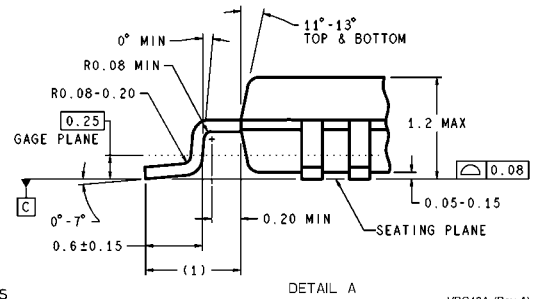
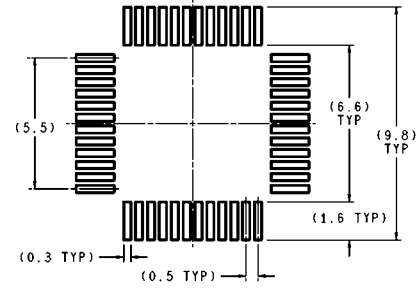
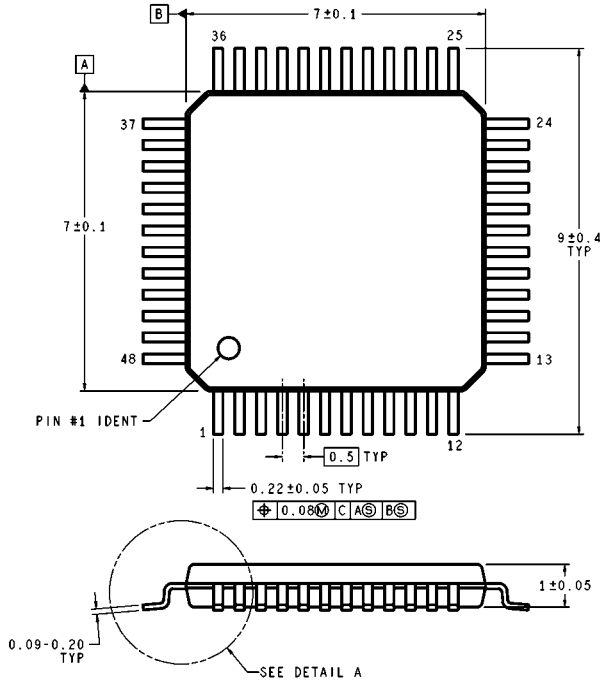
lated based on the typical supply current of 50 mA and a 10V supply voltage. This power dissipation will vary within the range of 0.4 W to 0.6 W due to process variations. In addition, each equivalent video load ( $150\Omega$ ) connected to the outputs should be budgeted 30 mW of power. For a typical application with one video load for each output this would be a total power of 0.62 W. With a  $\theta_{JA}$  of 44 °C/W this will result in the silicon being 27°C over the ambient temperature. A more aggressive application would be two video loads per output which would result in 0.74 W of power dissipation. This would result in a 33°C temperature rise. For heavier loading, the TQFP package thermal performance can be significantly enhanced with an external heat sink and by providing for moving air ventilation. Also, be sure to calculate the increase in ambient temperature from all devices operating in the system case. Because of the high power output of this device, thermal management should be considered very early in the design process. Generous passive venting and vertical board orientation may avoid the need for fan cooling or heat sinks. Also, the LMH6580/LMH6581 can be operated with a  $\pm 3.3V$  power supply. This will cut power dissipation substantially while only reducing bandwidth by about 10% ( $2 V_{PP}$  output). The LMH6580/LMH6581 are fully characterized and factory tested at the  $\pm 3.3V$  power supply condition for applications where reduced power is desired.

### PRINTED CIRCUIT LAYOUT

Generally, a good high frequency layout will keep power supply and ground traces away from the input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). If digital control lines must cross analog signal lines (particularly inputs) it is best if they cross perpendicularly. National Semiconductor suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMH6580	48-Pin	LMH730164EF

**Physical Dimensions** inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

**48-Pin QFP**  
**NS Package Number VBC48A**

VBC48A (Rev A)

# Notes

LMH6580/LMH6581



## Notes

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