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# DS91M125

## 125 MHz 1:4 M-LVDS Repeater with LVDS Input

### General Description

The DS91M125 is a 1:4 M-LVDS repeater designed for driving and distributing clock or data signals to up to four multipoint networks.

M-LVDS (Multipoint LVDS) is a new family of bus interface devices based on LVDS technology specifically designed for multipoint and multidrop cable and backplane applications. It differs from standard LVDS in providing increased drive current to handle double terminations that are required in multipoint applications. Controlled transition times minimize reflections that are common in multipoint configurations due to unterminated stubs.

A single DS91M125 channel is a 1:4 repeater that accepts M-LVDS/LVDS/CML/LVPECL signals and converts them to M-LVDS signal levels. Each output has an associated independent driver enable pin. The DS91M125 input conforms to the LVDS standard.

The DS91M125 has a flow-through pinout for easy PCB layout. It provides a new alternative for high speed multipoint interface applications. It is packaged in a space saving SOIC-16 package.

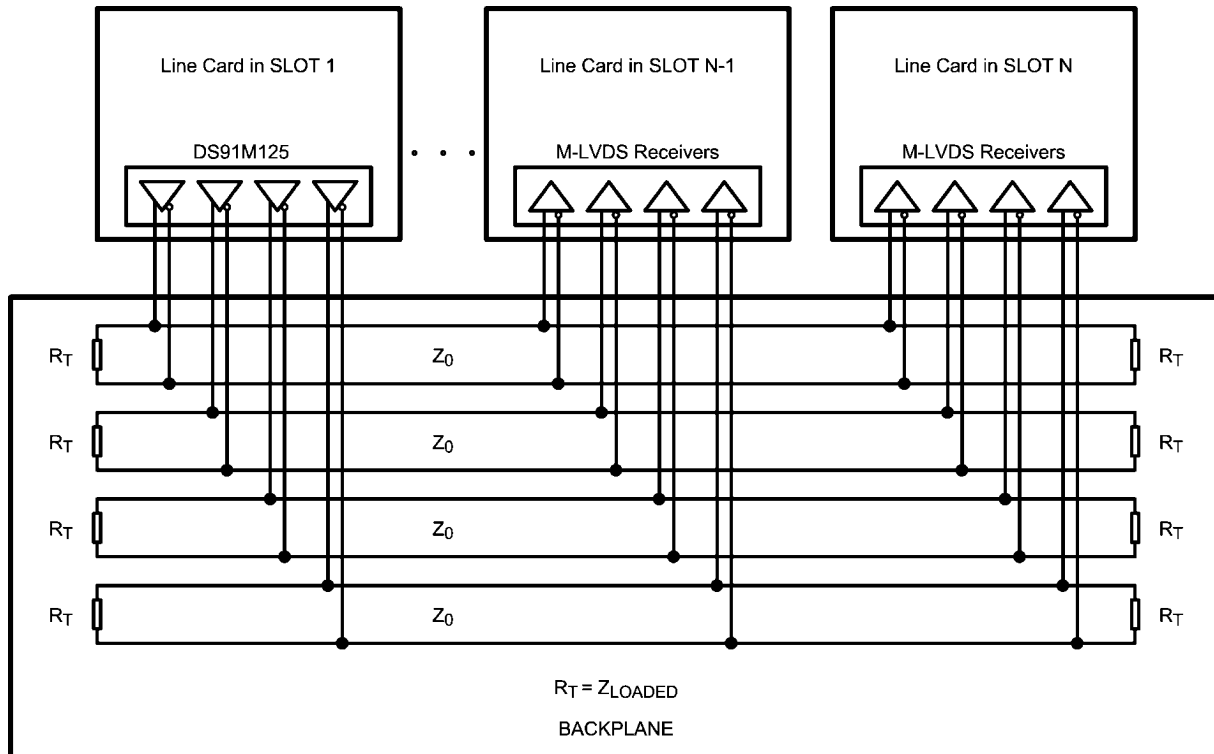
### Features

- DC - 125 MHz / 250 Mbps low jitter, low skew, low power operation
- Independent Driver Enable pins
- Outputs Conform to TIA/EIA-899 M-LVDS Standard
- Controlled transition times minimize reflections
- Inputs Conform to TIA/EIA-644-A LVDS Standard
- 8 kV ESD on M-LVDS output pins protects adjoining components
- Flow-through pinout simplifies PCB layout
- Industrial operating temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
- Available in a space saving SOIC-16 package

### Applications

- Multidrop / Multipoint clock and data distribution
- High-Speed, Low Power, Short-Reach alternative to TIA/EIA-485/422
- Clock distribution in AdvancedTCA (ATCA) and MicroTCA ( $\mu\text{TCA}$ ,  $u\text{TCA}$ ) backplanes

### Typical Application

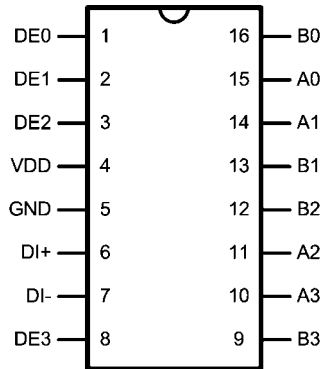


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## Ordering Information

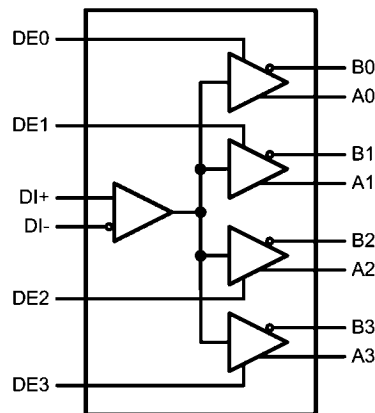
| Order Number | Function     | Package Type |
|--------------|--------------|--------------|
| DS91M125TMA  | 1:4 Repeater | SOIC-16      |

## Connection Diagram



30054201

## Logic Diagram



30054203

## Pin Descriptions

| Number         | Name            | I/O, Type | Description  |
|----------------|-----------------|-----------|--|
| 1, 2, 3, 8     | DE              | I, LVCMOS | Driver enable pins: When DE is low, the driver is disabled. When DE is high, the driver is enabled. There is a 300 k $\Omega$ pulldown resistor on each pin. |
| 6              | DI+             | I, LVDS   | Non-inverting receiver input pin.  |
| 7              | DI-             | I, LVDS   | Inverting receiver input pin.  |
| 5              | GND             | Power     | Ground pin.  |
| 10, 11, 14, 15 | A               | O, M-LVDS | Non-inverting driver output pin.   |
| 9, 12, 13, 16  | B               | O, M-LVDS | Inverting driver output pin.   |
| 4              | V <sub>DD</sub> | Power     | Power supply pin, +3.3V $\pm$ 0.3V   |

## Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|   |                              |
|---|------------------------------|
| Supply Voltage                                | -0.3V to +4V                 |
| LVC MOS Input Voltages                        | -0.3V to ( $V_{DD} + 0.3V$ ) |
| M-LVDS Output Voltages                        | -1.9V to +5.5V               |
| LVDS Input Voltages                           | -0.3V to ( $V_{DD} + 0.3V$ ) |
| Maximum Package Power Dissipation at +25°C    |                              |
| SOIC Package                                  | 2.21W                        |
| Derate SOIC Package                           | 19.2 mW/°C above +25°C       |
| Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC) |                              |
| $\theta_{JA}$                                 | 52°C/W                       |
| $\theta_{JC}$                                 | 19°C/W                       |
| Maximum Junction Temperature                  | 140°C                        |
| Storage Temperature Range                     | -65°C to +150°C              |
| Lead Temperature<br>(Soldering, 4 seconds)    | 260°C                        |

## ESD Susceptibility

|                             |         |
|-----------------------------|---------|
| HBM <small>(Note 1)</small> | ≥ 8 kV  |
| MM <small>(Note 2)</small>  | ≥ 250V  |
| CDM <small>(Note 3)</small> | ≥ 1250V |

**Note 1:** Human Body Model, applicable std. JESD22-A114C

**Note 2:** Machine Model, applicable std. JESD22-A115-A

**Note 3:** Field Induced Charge Device Model, applicable std. JESD22-C101-C

## Recommended Operating Conditions

|   | Min  | Typ | Max      | Units |
|---|------|-----|----------|-------|
| Supply Voltage, $V_{DD}$                | 3.0  | 3.3 | 3.6      | V     |
| Voltage at M-LVDS Outputs               | -1.4 |     | +3.8     | V     |
| Voltage at LVDS Inputs                  | 0    |     | $V_{DD}$ | V     |
| LVC MOS Input Voltage High $V_{IH}$     | 2.0  |     | $V_{DD}$ | V     |
| LVC MOS Input Voltage Low $V_{IL}$      | 0    |     | 0.8      | V     |
| Operating Free Air<br>Temperature $T_A$ | -40  | +25 | +85      | °C    |

## Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 5, Note 6, Note 7, Note 10)

| Symbol                                 | Parameter  | Conditions   | Min       | Typ | Max         | Units |
|--|--|--|-----------|-----|-------------|-------|
| <b>LVC MOS DC Specifications</b>       |  |  |           |     |             |       |
| $V_{IH}$                               | High-Level Input Voltage   |  | 2.0       |     | $V_{DD}$    | V     |
| $V_{IL}$                               | Low-Level Input Voltage  |  | GND       |     | 0.8         | V     |
| $I_{IH}$                               | High-Level Input Current   | $V_{IH} = 3.6V$  | -15       | ±1  | 15          | μA    |
| $I_{IL}$                               | Low-Level Input Current  | $V_{IL} = 0V$  | -15       | ±1  | 15          | μA    |
| $V_{CL}$                               | Input Clamp Voltage  | $I_{IN} = -18\text{ mA}$   | -1.5      |     |             | V     |
| <b>M-LVDS Driver DC Specifications</b> |  |  |           |     |             |       |
| $ V_{AB} $                             | Differential output voltage magnitude                                  | $R_L = 50\Omega, C_L = 5pF$  | 480       |     | 650         | mV    |
| $\Delta V_{AB}$                        | Change in differential output voltage magnitude between logic states   | Figures 1, 3   | -50       | 0   | +50         | mV    |
| $V_{OS(SS)}$                           | Steady-state common-mode output voltage                                | $R_L = 50\Omega, C_L = 5pF$  | 0.3       | 1.6 | 2.1         | V     |
| $ \Delta V_{OS(SS)} $                  | Change in steady-state common-mode output voltage between logic states | Figures 1, 2   | 0         |     | +50         | mV    |
| $V_{A(OC)}$                            | Maximum steady-state open-circuit output voltage                       | Figure 4   | 0         |     | 2.4         | V     |
| $V_{B(OC)}$                            | Maximum steady-state open-circuit output voltage                       |  | 0         |     | 2.4         | V     |
| $V_{P(H)}$                             | Voltage overshoot, low-to-high level output                            | $R_L = 50\Omega, C_L = 5pF, C_D = 0.5pF$<br>Figures 6, 7 <small>(Note 8)</small> |           |     | $1.2V_{SS}$ | V     |
| $V_{P(L)}$                             | Voltage overshoot, high-to-low level output                            |  | $-0.2V_s$ |     |             | V     |
| $I_{OS}$                               | Differential short-circuit output current                              | Figure 5 <small>(Note 9)</small>   | -43       |     | 43          | mA    |
| $I_A$                                  | Driver output current  | $V_A = 3.8V, V_B = 1.2V$   |           |     | 32          | μA    |
|  |  | $V_A = 0V$ or $2.4V, V_B = 1.2V$   | -20       |     | +20         | μA    |
|  |  | $V_A = -1.4V, V_B = 1.2V$  | -32       |     |             | μA    |
| $I_B$                                  | Driver output current  | $V_B = 3.8V, V_A = 1.2V$   |           |     | 32          | μA    |
|  |  | $V_B = 0V$ or $2.4V, V_A = 1.2V$   | -20       |     | +20         | μA    |
|  |  | $V_B = -1.4V, V_A = 1.2V$  | -32       |     |             | μA    |
| $I_{AB}$                               | Driver output differential current ( $I_A - I_B$ )                     | $V_A = V_B, -1.4V \leq V \leq 3.8V$  | -4        |     | +4          | μA    |

| Symbol                                 | Parameter  | Conditions  | Min  | Typ     | Max             | Units   |
|--|--|---|------|---------|-----------------|---------|
| $I_{A(OFF)}$                           | Driver output power-off current  | $V_A = 3.8V, V_B = 1.2V,$<br>$DE = 0V$<br>$0V \leq V_{DD} \leq 1.5V$            |      |         | 32              | $\mu A$ |
|  |  | $V_A = 0V$ or $2.4V, V_B = 1.2V,$<br>$DE = 0V$<br>$0V \leq V_{DD} \leq 1.5V$    | -20  |         | +20             | $\mu A$ |
|  |  | $V_A = -1.4V, V_B = 1.2V,$<br>$DE = 0V$<br>$0V \leq V_{DD} \leq 1.5V$           | -32  |         |                 | $\mu A$ |
| $I_{B(OFF)}$                           | Driver output power-off current  | $V_B = 3.8V, V_A = 1.2V,$<br>$DE = 0V$<br>$0V \leq V_{DD} \leq 1.5V$            |      |         | 32              | $\mu A$ |
|  |  | $V_B = 0V$ or $2.4V, V_A = 1.2V,$<br>$DE = 0V$<br>$0V \leq V_{DD} \leq 1.5V$    | -20  |         | +20             | $\mu A$ |
|  |  | $V_B = -1.4V, V_A = 1.2V,$<br>$DE = 0V$<br>$0V \leq V_{DD} \leq 1.5V$           | -32  |         |                 | $\mu A$ |
| $I_{AB(OFF)}$                          | Driver output power-off differential current ( $I_{A(OFF)} - I_{B(OFF)}$ ) | $V_A = V_B, -1.4V \leq V \leq 3.8V,$<br>$DE = 0V$<br>$0V \leq V_{DD} \leq 1.5V$ | -4   |         | +4              | $\mu A$ |
| $C_A$                                  | Driver output capacitance  | $V_{DD} = OPEN$   |      | 7.8     |                 | pF      |
| $C_B$                                  | Driver output capacitance  |   |      | 7.8     |                 | pF      |
| $C_{AB}$                               | Driver output differential capacitance                                     |   |      | 3       |                 | pF      |
| $C_{A/B}$                              | Driver output capacitance balance ( $C_A/C_B$ )                            |   |      | 1       |                 |         |
| <b>LVDS Receiver DC Specifications</b> |  |   |      |         |                 |         |
| $V_{IT+}$                              | Positive-going differential input voltage threshold                        |   |      | -5      | 100             | mV      |
| $V_{IT-}$                              | Negative-going differential input voltage threshold                        |   | -100 | -5      |                 | mV      |
| $V_{CMR}$                              | Common mode voltage range  | $VID = 100$ mV  | 0.05 |         | $V_{DD} - 0.05$ | V       |
| $I_{IN}$                               | Input current  | $V_{IN} = 3.6V, V_{DD} = 3.6V$  |      | $\pm 1$ | $\pm 10$        | $\mu A$ |
|  |  | $V_{IN} = 0V, V_{DD} = 3.6V$  |      | $\pm 1$ | $\pm 10$        | $\mu A$ |
| $C_{IN}$                               | Input capacitance  | $V_{DD} = OPEN$   |      | 5       |                 | pF      |
| <b>POWER SUPPLY CURRENT</b>            |  |   |      |         |                 |         |
| $I_{CCD}$                              | Driver Supply Current  | $R_L = 50\Omega, DE = V_{DD}$   |      | 67      | 78              | mA      |
| $I_{CCZ}$                              | TRI-STATE Supply Current   | $DE = GND$  |      | 21      | 26              | mA      |

**Note 4:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

**Note 5:** The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

**Note 6:** Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except  $V_{OD}$  and  $\Delta V_{OD}$ .

**Note 7:** Typical values represent most likely parametric norms for  $V_{DD} = +3.3V$  and  $T_A = +25^\circ C$ , and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

**Note 8:** Specification is guaranteed by characterization and is not tested in production.

**Note 9:** Output short circuit current ( $I_{OS}$ ) is specified as magnitude only, minus sign indicates direction only.

**Note 10:**  $C_L$  includes fixture capacitance and  $C_D$  includes probe capacitance.

## Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 11, Note 12, Note 18)

| Symbol                         | Parameter   | Conditions                       | Min | Typ | Max | Units |
|--------------------------------|---|----------------------------------|-----|-----|-----|-------|
| <b>DRIVER AC SPECIFICATION</b> |   |                                  |     |     |     |       |
| $t_{PLH}$                      | Differential Propagation Delay Low to High            | $R_L = 50\Omega$ , $C_L = 5$ pF, | 3.0 | 5.5 | 8.5 | ns    |
| $t_{PHL}$                      | Differential Propagation Delay High to Low            | $C_D = 0.5$ pF                   | 3.0 | 5.5 | 8.5 | ns    |
| $t_{SKD1}$ ( $t_{sk(p)}$ )     | Pulse Skew $ t_{PLHD} - t_{PHLD} $ (Note 14, Note 19) | Figures 6, 7                     |     | 65  | 350 | ps    |
| $t_{SKD2}$                     | Channel-to-Channel Skew (Note 15, Note 19)            |                                  |     | 65  | 400 | ps    |
| $t_{SKD3}$                     | Part-to-Part Skew (Note 16, Note 19)                  |                                  |     | 2.2 | 2.5 | ns    |
| $t_{SKD4}$                     | Part-to-Part Skew (Note 17)                           |                                  |     |     | 5.5 | ns    |
| $t_{TLH}$ ( $t_r$ )            | Rise Time (Note 19)                                   |                                  | 1.1 | 2.0 | 3.0 | ns    |
| $t_{THL}$ ( $t_f$ )            | Fall Time (Note 19)                                   |                                  | 1.1 | 2.0 | 3.0 | ns    |
| $t_{PZH}$                      | Enable Time (Z to Active High)                        | $R_L = 50\Omega$ , $C_L = 5$ pF, |     | 6   | 11  | ns    |
| $t_{PZL}$                      | Enable Time (Z to Active Low)                         | $C_D = 0.5$ pF                   |     | 6   | 11  | ns    |
| $t_{PLZ}$                      | Disable Time (Active Low to Z)                        | Figures 8, 9                     |     | 6   | 11  | ns    |
| $t_{PHZ}$                      | Disable Time (Active High to Z)                       |                                  |     | 6   | 11  | ns    |
| $f_{MAX}$                      | Maximum Operating Frequency (Note 19)                 |                                  | 125 |     |     | MHz   |

**Note 11:** The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes.

**Note 12:** Typical values represent most likely parametric norms for  $V_{DD} = +3.3V$  and  $T_A = +25^\circ C$ , and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

**Note 13:** Specification is guaranteed by characterization and is not tested in production.

**Note 14:**  $t_{SKD1}$ ,  $|t_{PLHD} - t_{PHLD}|$ , is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

**Note 15:**  $t_{SKD2}$ , Channel-to-Channel Skew, is the difference in propagation delay ( $t_{PLHD}$  or  $t_{PHLD}$ ) among all output channels.

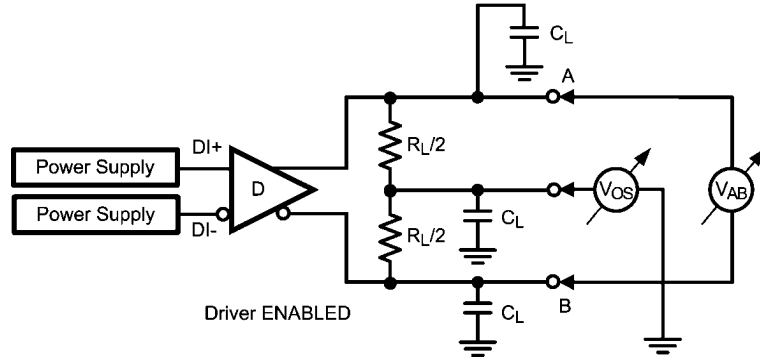
**Note 16:**  $t_{SKD3}$ , Part-to-Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same  $V_{DD}$  and within  $5^\circ C$  of each other within the operating temperature range.

**Note 17:**  $t_{SKD4}$ , Part-to-Part Skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution.  $t_{SKD4}$  is defined as  $|Max - Min|$  differential propagation delay.

**Note 18:**  $C_L$  includes fixture capacitance and  $C_D$  includes probe capacitance.

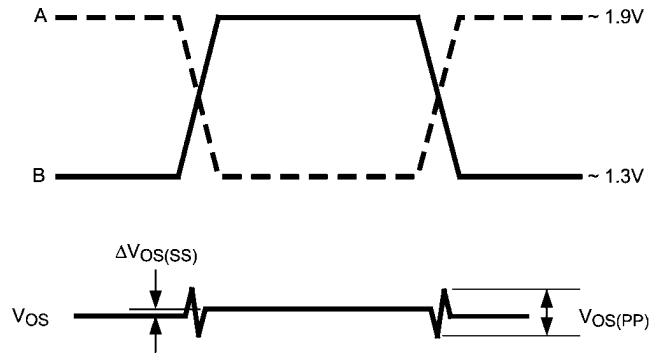
**Note 19:** Specification is guaranteed by characterization and is not tested in production.

# Test Circuits and Waveforms



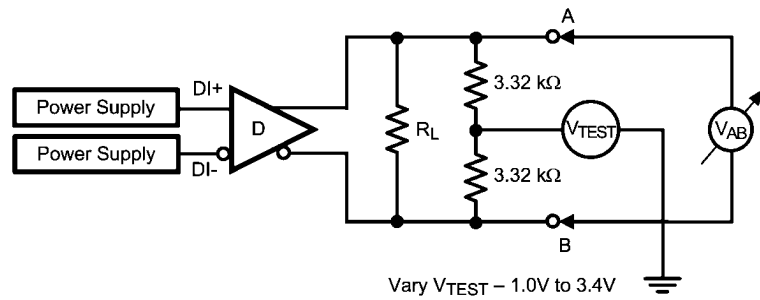
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FIGURE 1. Differential Driver Test Circuit



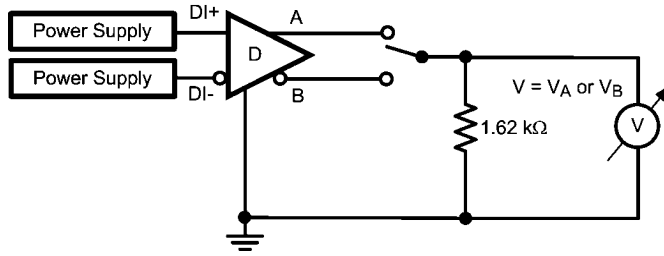
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FIGURE 2. Differential Driver Waveforms



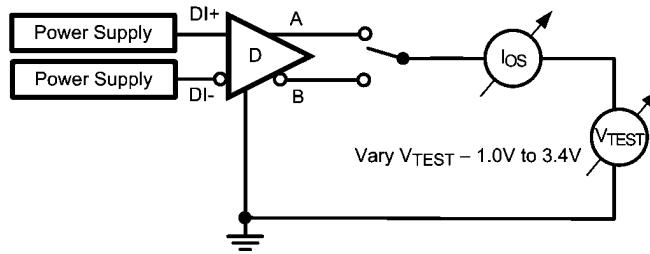
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FIGURE 3. Differential Driver Full Load Test Circuit



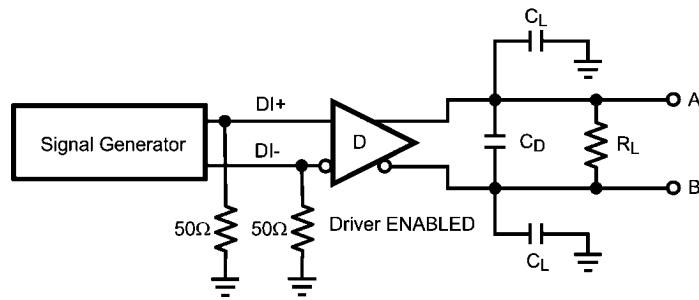
30054212

FIGURE 4. Differential Driver DC Open Test Circuit



30054225

FIGURE 5. Differential Driver Short-Circuit Test Circuit



30054216

FIGURE 6. Driver Propagation Delay and Transition Time Test Circuit



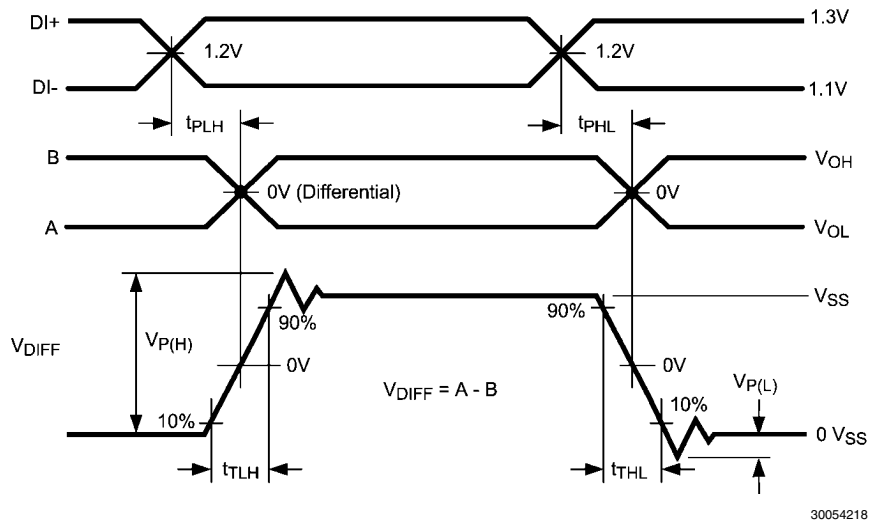


FIGURE 7. Driver Propagation Delays and Transition Time Waveforms

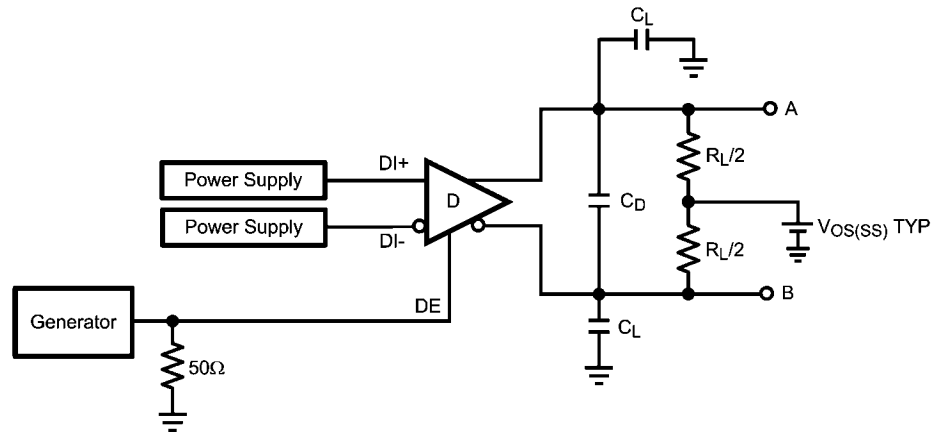


FIGURE 8. Driver TRI-STATE Delay Test Circuit

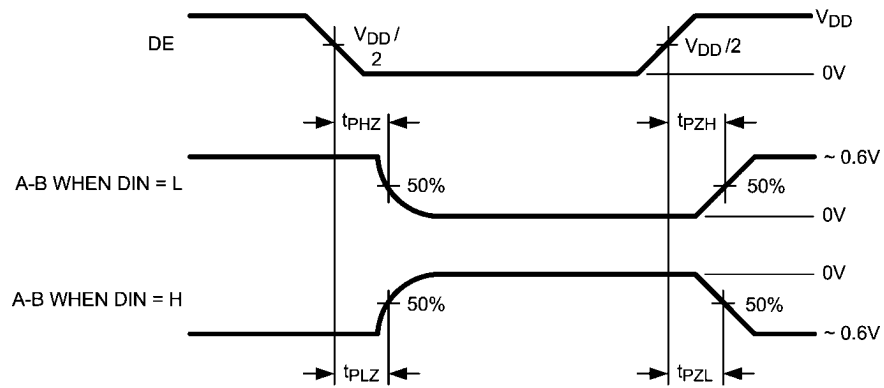
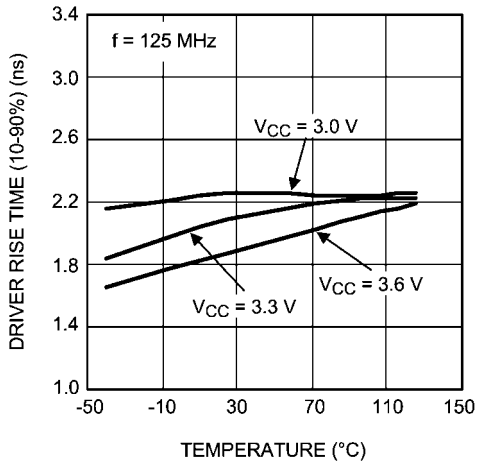
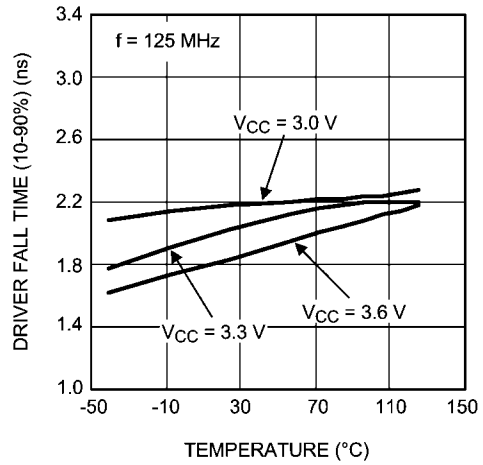


FIGURE 9. Driver TRI-STATE Delay Waveforms

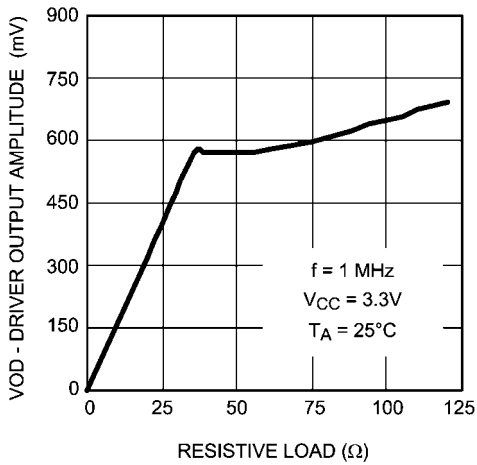
# Typical Performance Characteristics



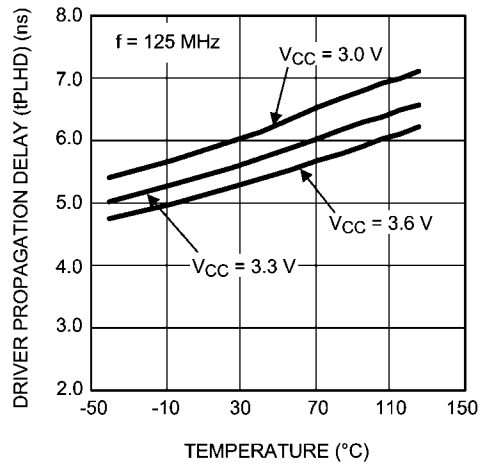
Driver Rise Time as a Function of Temperature



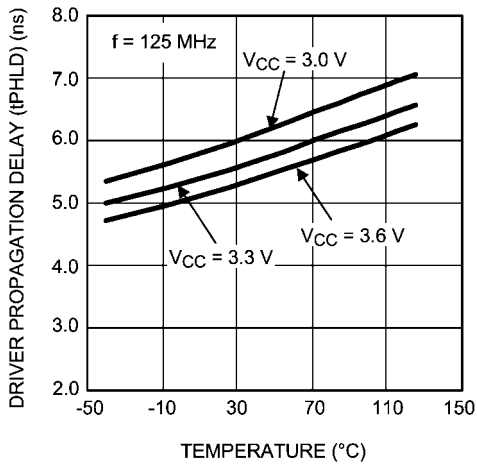
Driver Fall Time as a Function of Temperature



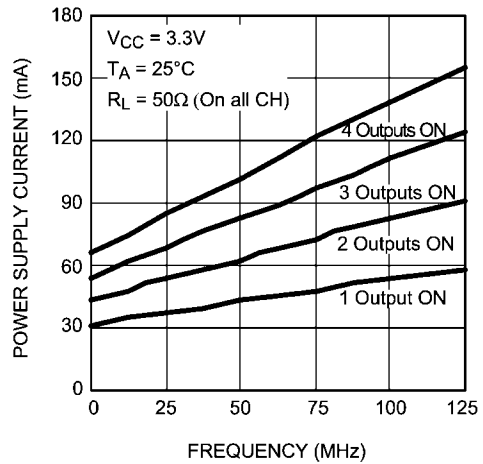
Driver Output Signal Amplitude as a Function of Resistive Load



Driver Propagation Delay (tPLHD) as a Function of Temperature

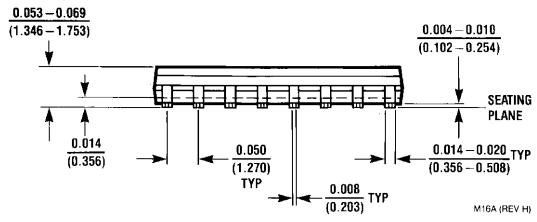
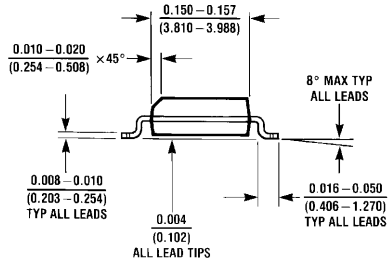
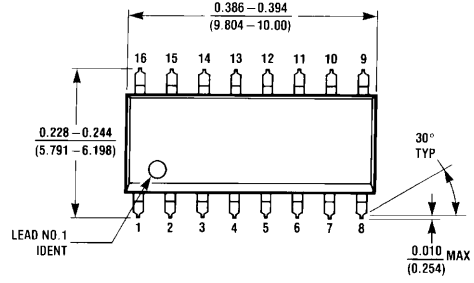


Driver Propagation Delay (tPHLD) as a Function of Temperature



Driver Power Supply Current as a Function of Frequency

**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead (0.150 Wide) Molded Small Outline Package, JEDEC  
Order Number DS91M125TMA  
NS Package Number M16A**

# Notes

DS91M125

## Notes

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| Switching Regulators           | <a href="http://www.national.com/switchers">www.national.com/switchers</a>   | Distributors                 | <a href="http://www.national.com/contacts">www.national.com/contacts</a>           |
| LDOs                           | <a href="http://www.national.com/ldo">www.national.com/ldo</a>               | Quality and Reliability      | <a href="http://www.national.com/quality">www.national.com/quality</a>             |
| LED Lighting                   | <a href="http://www.national.com/led">www.national.com/led</a>               | Feedback/Support             | <a href="http://www.national.com/feedback">www.national.com/feedback</a>           |
| Voltage Reference              | <a href="http://www.national.com/vref">www.national.com/vref</a>             | Design Made Easy             | <a href="http://www.national.com/easy">www.national.com/easy</a>                   |
| PowerWise® Solutions           | <a href="http://www.national.com/powerwise">www.national.com/powerwise</a>   | Solutions                    | <a href="http://www.national.com/solutions">www.national.com/solutions</a>         |
| Serial Digital Interface (SDI) | <a href="http://www.national.com/sdi">www.national.com/sdi</a>               | Mil/Aero                     | <a href="http://www.national.com/milaero">www.national.com/milaero</a>             |
| Temperature Sensors            | <a href="http://www.national.com/tempensors">www.national.com/tempensors</a> | SolarMagic™                  | <a href="http://www.national.com/solarmagic">www.national.com/solarmagic</a>       |
| Wireless (PLL/VCO)             | <a href="http://www.national.com/wireless">www.national.com/wireless</a>     | PowerWise® Design University | <a href="http://www.national.com/training">www.national.com/training</a>           |

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