Complete 10-Bit, 36 MSPS CCD Signal Processor

AD9840

FEATURES

36 MSPS Correlated Double Sampler (CDS)
2 ~ 36 dB 10-Bit Variable Gain Amplifier (VGA)
Low Noise Clamp Circuits
Analog Preblanking Function
10-Bit 36 MSPS A/D Converter
No Missing Codes Guaranteed
Auxiliary Inputs with VGA and Input Clamp
3-Wire Serial Digital Interface
3 V Single Supply Operation
Low Power CMOS: 140 mW @ 3.0 V Supply
48-Lead LQFP Package

APPLICATIONS

Digital Still Cameras
Digital Video Camcorders

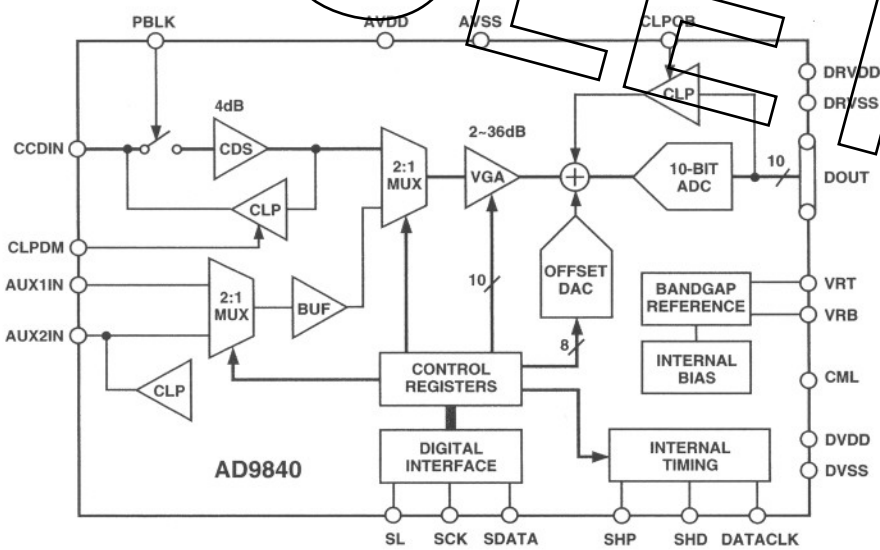
PRODUCT DESCRIPTION

The AD9840 is a complete analog signal processor for CCD applications. It features a 36 MHz single-channel architecture designed to sample and condition the outputs of interlaced and progressive scan area CCD arrays. The AD9840's signal chain consists of an input clamp, correlated double sampler (CDS), digitally controlled VGA, black level clamp, and a 10-bit A/D converter. Additional input modes are provided for processing analog video signals.

The internal registers are programmed through a 3-wire serial digital interface. Programmable features include gain adjustment, black level adjustment, input configuration, and power-down modes.

The AD9840 operates from a 3 V power supply, typically consumes 140 mW, and is packaged in a 48-lead LQFP.

FUNCTIONAL BLOCK DIAGRAM



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AD9840–TARGET SPECIFICATIONS

AUX2-MODE SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = DVDD = 3.0 V, $f_{DATACLK}$ = 36 MHz, unless otherwise noted)

Parameter	Min	Typ	Max	Unit
POWER CONSUMPTION		98		mW
MAXIMUM CLOCK RATE	36			MHz
INPUT BUFFER		(Same as AUX1-MODE)		
VGA				
Max Output Range	2.0			V p-p
Gain (Selected in VGA Gain Register)				
Gain Control Resolution		512		Steps
Min Gain		0		dB
Max Gain		18		dB
ACTIVE CLAMP				
Clamp Level (Measured at ADC Output)				
Clamp Level Resolution		256		Steps
Min Clamp Level		0		LSB
Max Clamp Level		63.75		LSB

Specifications subject to change without notice.

CCD-MODE TIMING SPECIFICATIONS (C_L = 20 pF, Timing Shown in Figures 1 and 2)

Parameter	Symbol	Min	Typ	Max	Unit
CLOCK PARAMETERS					
DATACLK, SHP, SHD Clock Period	t_{CP}	27.6			ns
DATACLK Hi/Low Pulsewidth	t_{ADC}	10	13.8		ns
SHP Pulsewidth	t_{SHP}	5	7		ns
SHD Pulsewidth	t_{SHD}	5	7		ns
CLPDM Pulsewidth[1]	t_{CDM}	4	10		Pixels
CLPOB Pulsewidth[1]	t_{COB}	2	20		Pixels
SHP Rising Edge to SHD Falling Edge	t_{S1}	0	7		ns
SHP Rising Edge to SHD Rising Edge	t_{S2}	10	13.8		ns
Internal Clock Delay	t_{ID}		3.0		ns
Inhibited Clock Period	t_{INH}	10			ns
DATA OUTPUTS					
Output Delay	t_{OD}		14.5		ns
Output Hold Time	t_H		7.6		ns
Pipeline Delay			9		Cycles

NOTES
[1]Minimum CLPOB and CLPDM pulsewidth is for functional operation only. Wider pulses are recommended to achieve lower clamp noise performance.
Specifications subject to change without notice.

AUX1-MODE TIMING SPECIFICATIONS (C_L = 20 pF, Timing Shown in Figure 3)

Parameter	Symbol	Min	Typ	Max	Unit
CLOCK PARAMETERS					
DATACLK Clock Period	t_{CP}	27.6			ns
DATACLK Hi/Low Pulsewidth	t_{CLK}	10	13.8		ns
Internal Clock Delay	t_{ID}		3.0		ns
DATA OUTPUTS					
Output Delay	t_{OD}		14.5		ns
Output Hold Time	t_H		7.6		ns
Pipeline Delay			9		Cycles

Specifications subject to change without notice.

AUX2-MODE TIMING SPECIFICATIONS (Same as AUX1-MODE)

SERIAL INTERFACE TIMING SPECIFICATIONS (Timing Shown in Figure 5)

Parameter	Symbol	Min	Typ	Max	Unit
Maximum SCK Frequency	f_{SCLK}	6			MHz
SL to SCK Setup Time	t_{LS}	10			ns
SCK to SL Hold Time	t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns
SCK Falling Edge to SDATA Valid Hold	t_{DH}	10			ns

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

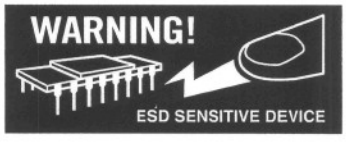
Parameter	With Respect to	Min	Max	Unit
AVDD	AVSS	–0.3	+3.9	V
DVDD	DVSS	–0.3	+3.9	V
DRVDD	DRVSS	–0.3	+3.9	V
Digital Outputs	DRVSS	–0.3	DRVDD + 0.3	V
SHP, SHD, DATACLK	DVSS	–0.3	DVDD + 0.3	V
CLPOB, CLPDM, PBLK	DVSS	–0.3	DVDD + 0.3	V
SCK, SL, SDATA	DVSS	–0.3	DVDD + 0.3	V
VRT, VRB, CMLEVEL	AVSS	–0.3	AVDD + 0.3	V
BYP1, 2, 4, CCDIN	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			150	°C
Lead Temperature (10 sec)			300	°C

ORDERING GUIDE

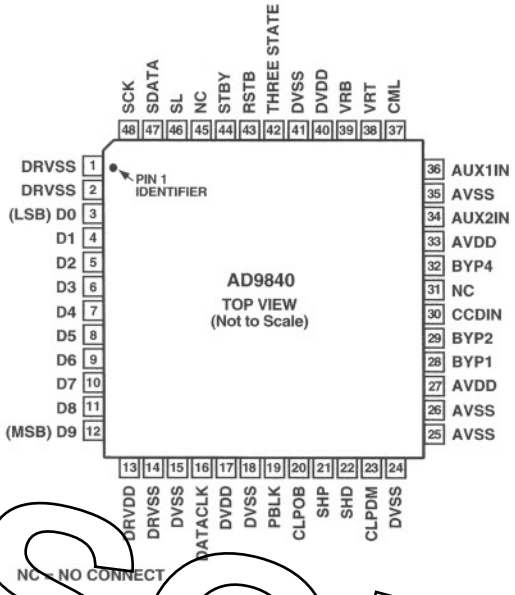
Model	Temperature Range	Package Description	Package Option
AD9840JST	–20°C to +75°C	Thin Plastic Quad Flatpack (LQFP)	ST-48

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9840 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



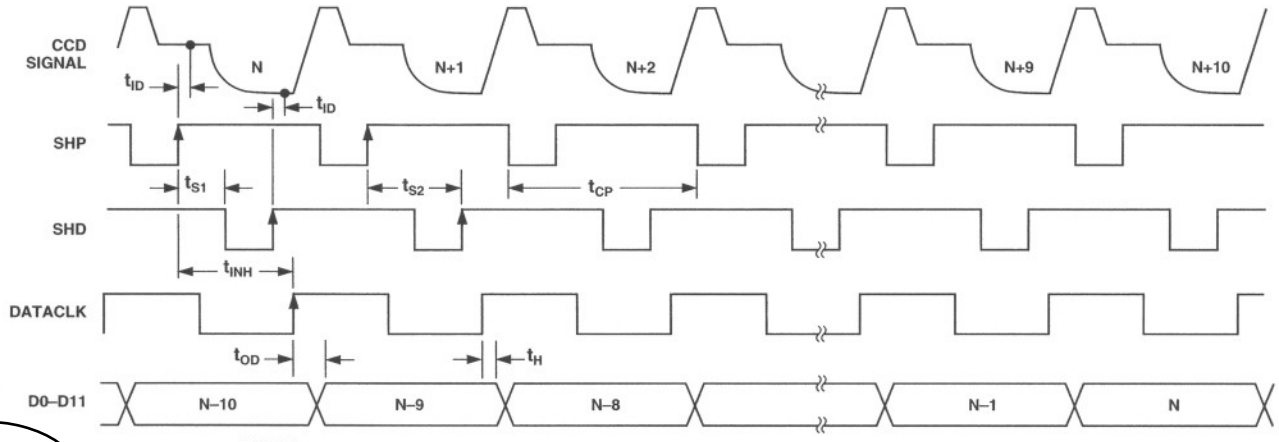
PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

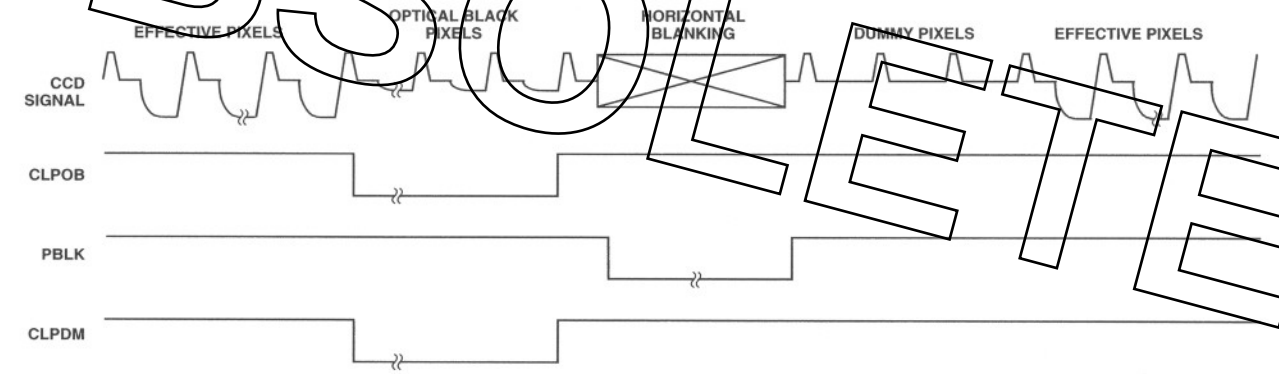
Pin Number	Name	Type	Description
1, 2, 14	DRVSS	P	Digital Output Driver Ground.
3–12	D0–D9	DO	Digital Data Outputs.
13	DRVDD	P	Digital Output Driver Supply.
15, 18, 24, 41	DVSS	P	Digital Ground.
16	DATACLK	DI	Digital Data Output Latch Clock.
17, 40	DVDD	P	Digital Supply.
19	PBLK	DI	Preblanking Clock Input.
20	CLPOB	DI	Black Level Clamp Clock Input.
21	SHP	DI	CDS Sampling Clock for CCD's Reference Level.
22	SHD	DI	CDS Sampling Clock for CCD's Data Level.
23	CLPDM	DI	Input Clamp Clock Input.
25, 26, 35	AVSS	P	Analog Ground.
27, 33	AVDD	P	Analog Supply.
28	BYP1	AO	Internal Bias Level Decoupling.
29	BYP2	AO	Internal Bias Level Decoupling.
30	CCDIN	AI	Analog Input for CCD Signal.
31, 45	NC	NC	Internally Unconnected.
32	BYP4	AO	Internal Bias Level Decoupling.
34	AUX2IN	AI	Analog Input.
36	AUX1IN	AI	Analog Input.
37	CML	AO	Internal Bias Level Decoupling.
38	VRT	AO	A/D Converter Top Reference Voltage Decoupling.
39	VRB	AO	A/D Converter Bottom Reference Voltage Decoupling.
42	THREE-STATE	DI	Digital Output Disable. Active High.
43	RSTB	DI	Reset Control for Internal Registers. Active Low.
44	STBY	DI	Standby Mode. Active High.
46	SL	DI	Serial Digital Interface Load Pulse. Short to SEN.
47	SDATA	DI	Serial Digital Interface Data.
48	SCK	DI	Serial Digital Interface Clock.

TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power.



NOTES:
1. RECOMMENDED PLACEMENT FOR DATACLK RISING EDGE IS BETWEEN THE SHD RISING EDGE AND NEXT SHP FALLING EDGE.
2. CCD SIGNAL IS SAMPLED AT SHP AND SHD RISING EDGES.

Figure 1. CCD-Mode Timing



NOTES:
1. CLPOB AND CLPDM WILL OVERWRITE PBLK. PBLK WILL NOT AFFECT CLAMP OPERATION IF OVERLAPPING CLPDM AND/OR CLPOB.
2. PBLK SIGNAL IS OPTIONAL.

Figure 2. Typical CCD-Mode-Line Clamp Timing

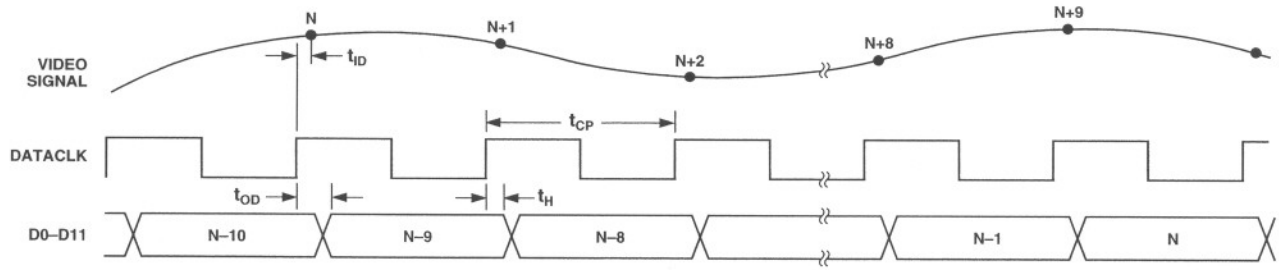


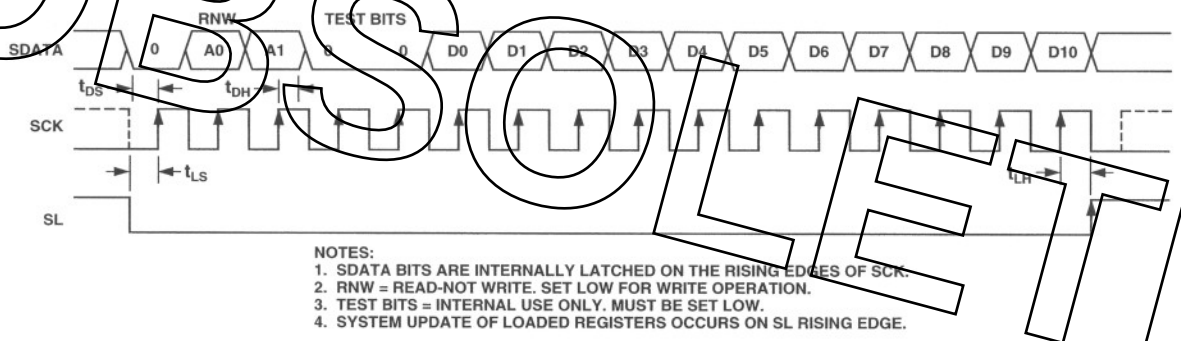
Figure 3. AUX-Mode Timing

INTERNAL REGISTER DESCRIPTION

Table I. Internal Register Map Overview

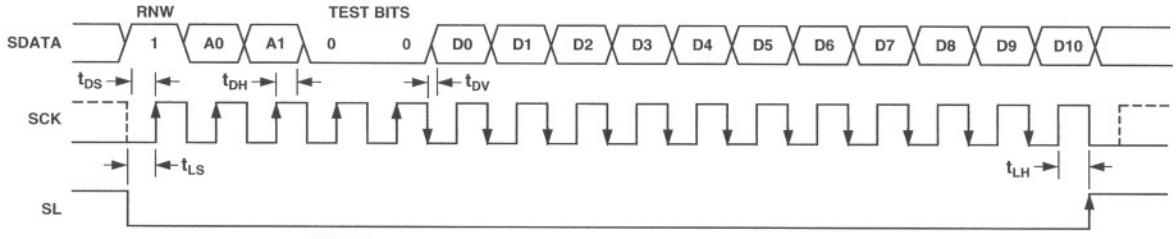
Register Name	Address A0	A1	Data Bits D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
Operation	0	0	Channel Select CCD/AUX		Power-Down Modes		0*	Clamp On/Off	0*	1**	0*	0*	0*
VGA Gain	1	0	LSB									MSB	X
Clamp Level	0	1	LSB							MSB	X	X	X
Control	1	1	0*	0*	0*	0*	Clock Polarity Select for SHP/SHD/CLP/DATA			0*	0**	Three-State	X

*Internal use only. Must be set to zero.
**Must be set to one.



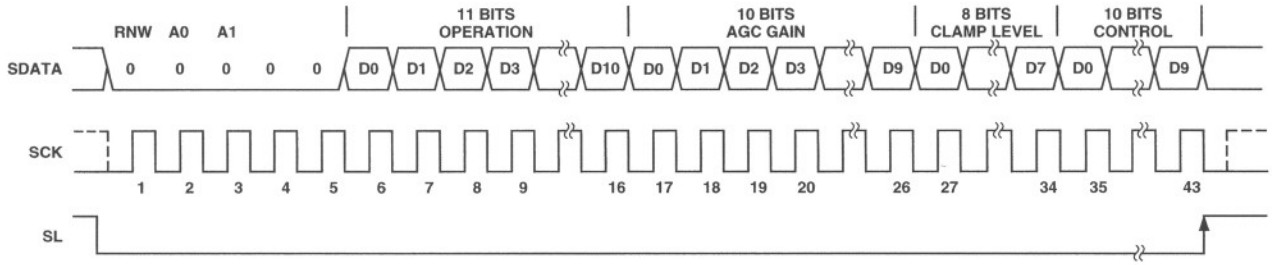
NOTES:
1. SDATA BITS ARE INTERNALLY LATCHED ON THE RISING EDGES OF SCK.
2. RNW = READ-NOT WRITE. SET LOW FOR WRITE OPERATION.
3. TEST BITS = INTERNAL USE ONLY. MUST BE SET LOW.
4. SYSTEM UPDATE OF LOADED REGISTERS OCCURS ON SL RISING EDGE.

Figure 4. Wire Serial Write Operation



NOTES:
1. RNW = READ-NOT WRITE. SET HIGH FOR READ OPERATION.
2. TEST BITS = INTERNAL USE ONLY. MUST BE SET LOW.
3. SERIAL DATA FROM THE SELECTED REGISTER IS VALID STARTING AFTER THE 5TH SCK FALLING EDGE, AND IS UPDATED ON SCK FALLING EDGES.

Figure 5. Serial Readback Operation



NOTES:
1. ANY NUMBER OF ADJACENT REGISTERS MAY BE LOADED SEQUENTIALLY, BEGINNING WITH THE LOWEST DESIRED ADDRESS AND INCREMENTING, ONE ADDRESS AT A TIME.
2. WHEN SEQUENTIALLY LOADING MULTIPLE REGISTERS, THE EXACT REGISTER LENGTH (SHOWN ABOVE) MUST BE USED FOR EACH REGISTER.
3. ALL LOADED REGISTERS WILL BE UPDATED SIMULTANEOUSLY WITH THE RISING EDGE OF SL.

Figure 6. Continuous Serial Write Operation to All Registers

Table II. Operation Register Contents (Default Value x000)

D10	D9	D8	D7	D6	Optical Black Clamp D5	D4	Power-Down Modes D3	D2		Channel Selection D1	D0	
0*	0*	0*	1**	0*	0 Enable Clamping 1 Disable Clamping	0*	0	0	Normal Power	0	0	CCD Mode
							0	1	Fast Recovery	0	1	AUX1 Mode
							1	0	Standby	1	0	AUX2 Mode
							1	1	Total Shutdown	1	1	Test Only

*Must be set to Zero
**Set to One

Table III. VGA Gain Register Contents (Default Value x096)

D10	MSB D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0	Gain (dB)
X	0	0	0	1	0	1	0	1	1	1	2.0
					•						•
					•						•
					•						•
	1	1	1	1	1	1	1	1	1	0	35.965
	1	1	1	1	1	1	1	1	1	1	36.0

Table IV. Clamp Level Register Contents (Default Value x080)

D10	D9	D8	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	Clamp Level (LSB)
X	X	X	0	0	0	0	0	0	0	0	0
			0	0	0	0	0	0	0	1	0.25
			0	0	0	0	0	0	1	0	0.5
						•					•
						•					•
						•					•
			1	1	1	1	1	1	1	0	63.5
			1	1	1	1	1	1	1	1	63.75

Table V. Control Register Contents (Default Value x000)

D10	Data Out D9	D8	D7	DATACLK D6	CLP/PBLK D5	SHP/SHD D4	D3	D2	D1	D0
X	0 Enable 1 Three-State	0*	0*	0 Rising Edge Trigger 1 Falling Edge Trigger	0 Active Low 1 Active High	0 Active Low 1 Active High	0*	0*	0*	0*

*Must be set to Zero

VARIABLE GAIN AMPLIfiER (VGA) OPERATION DETAILS

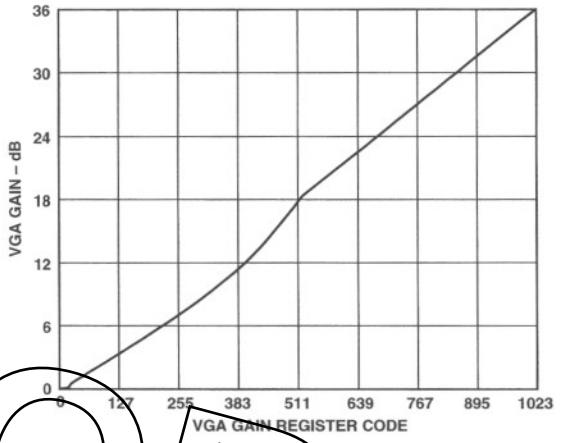


Figure 7. VGA Gain Curve (4 dB from CDS Stage Not Included)

The VGA gain curve is divided into two separate regions. When the VGA Gain Register Code is between 0 and Code 511, the curve follows a $(1 + x)/(1 - x)$ shape, which is similar to a *linear-in-dB* characteristic. From Code 512 to Code 1023, the curve follows a *linear-in-dB* shape. The exact VGA gain can be calculated for any Gain Register value by using the following two equations:

Code Range	Gain Equation (dB)
0–511	$Gain = 20 \log_{10} ([658 + Code]/[658 - Code]) - 0.3$
512–1023	$Gain = (0.0354)(Code) - 0.21$

As shown in the CCD-mode specifications, only the VGA gain range from 2 dB to 36 dB has tested and guaranteed accuracy. This corresponds to a gain code range of 87 to 1023.

APPLICATIONS

Generating the Reset (RSTB) Signal

After power-on, the AD9840 must be reset using Pin 43 (RSTB). The reset pulse must be an active low signal, which goes low for at least 100 ns after the power supplies have settled. After the RSTB signal goes back high, the AD9840 is internally reset to the default register values. If a system reset pulse is not available, a simple RC network may be used, as shown in Figure 8. The time constant of this network should be comparable to the power-on time of the AD9840's power supplies. For example, if the power supplies have a power-on time of 10 ms, the RC network should have a time constant of 10 ms, given R = 10 kΩ and C = 1.0 µF.

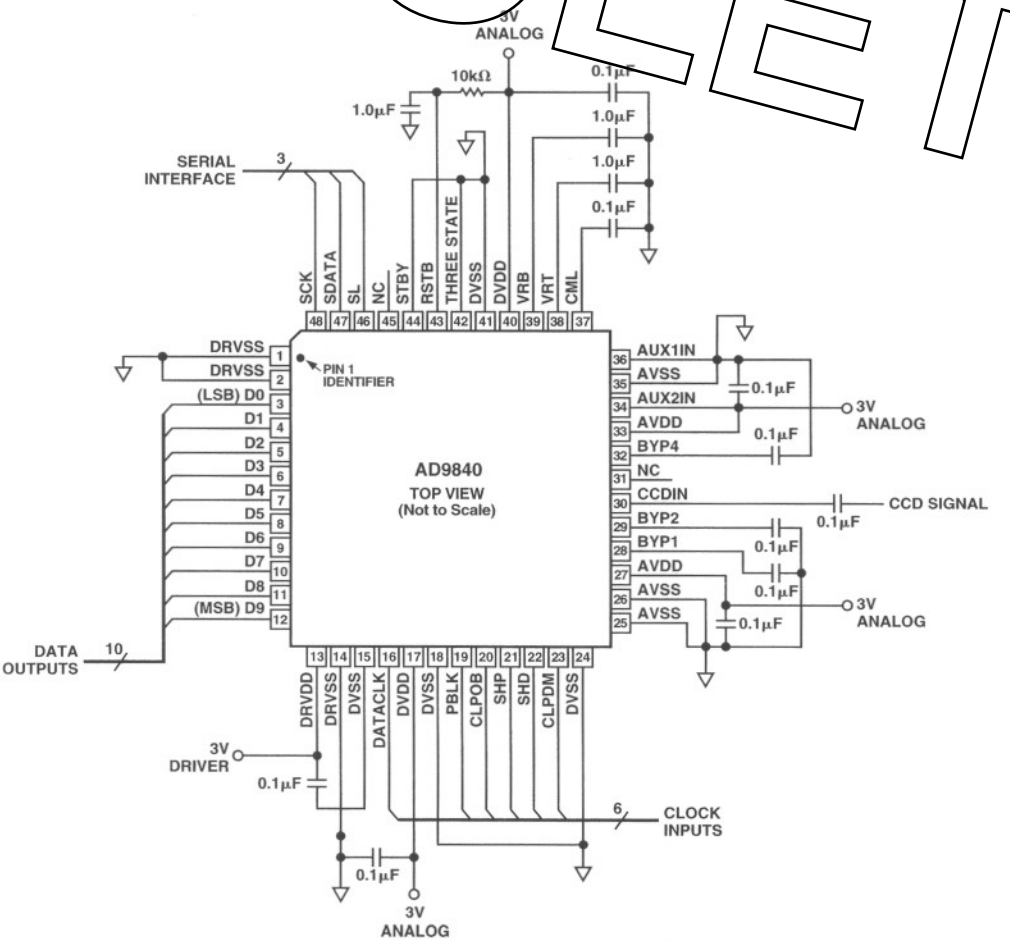


Figure 8. Recommended Circuit Configuration for CCD Mode

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead LQFP
(ST-48)