FAIRCHILD SEMICONDUCTOR®

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FIN24AC 22-Bit Bi-Directional Serializer/Deserializer

Features

- Low power for minimum impact on battery life
  - Multiple power-down modes
  - AC coupling with DC balance
- 100nA in standby mode, 5mA typical operating conditions
- Cable reduction: 25:4 or greater
- Bi-directional operation 50:7 reduction or greater
- Differential signaling:
  - -90dBm EMI when using CTL™ in lab conditions using a near field probe
  - Minimized shielding
  - Minimized EMI filter
  - Minimum susceptibility to external interference
- Up to 22 bits in either direction
- Up to 20MHz parallel interface operation
- Voltage translation from 1.65V to 3.6V
- Ultra-small and cost-effective packaging
- High ESD protection: >8kV HBM
- Parallel I/O power supply (V_{DDP}) range between 1.65V to 3.6V

Applications

- Microcontroller or pixel interfaces
- Image sensors
- Small displays
  - LCD, cell phone, digital camera, portable gaming, printer, PDA, video camera, automotive

Description

The FIN24AC is a low-power Serializer/Deserializer (µSerDes™) that can help minimize the cost and power of transferring wide signal paths. Through the use of serialization, the number of signals transferred from one point to another can be significantly reduced. Typical reduction is 4:1 to 6:1 for unidirectional paths. For bi-directional operation, using half duplex for multiple sources, it is possible to increase the signal reduction to close to 10:1. Through the use of differential signaling, shielding and EMI filters can also be minimized, further reducing the cost of serialization. The differential signaling is also important for providing a noise-insensitive signal that can withstand radio and electrical noise sources. Major reduction in power consumption allows minimal impact on battery life in ultra-portable applications. A single PLL is adequate for most applications, including bi-directional operation.

Ordering Information

Order Number	Eco Status	Operating Temperature Range	Package Description	Packing Method
FIN24ACGFX	RoHS	-30 to +70°C	42-Ball Ultra Small Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5mm Wide	Tape and Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

µSerDes™ is a trademark of Fairchild Semiconductor Corporation.

Functional Block Diagram

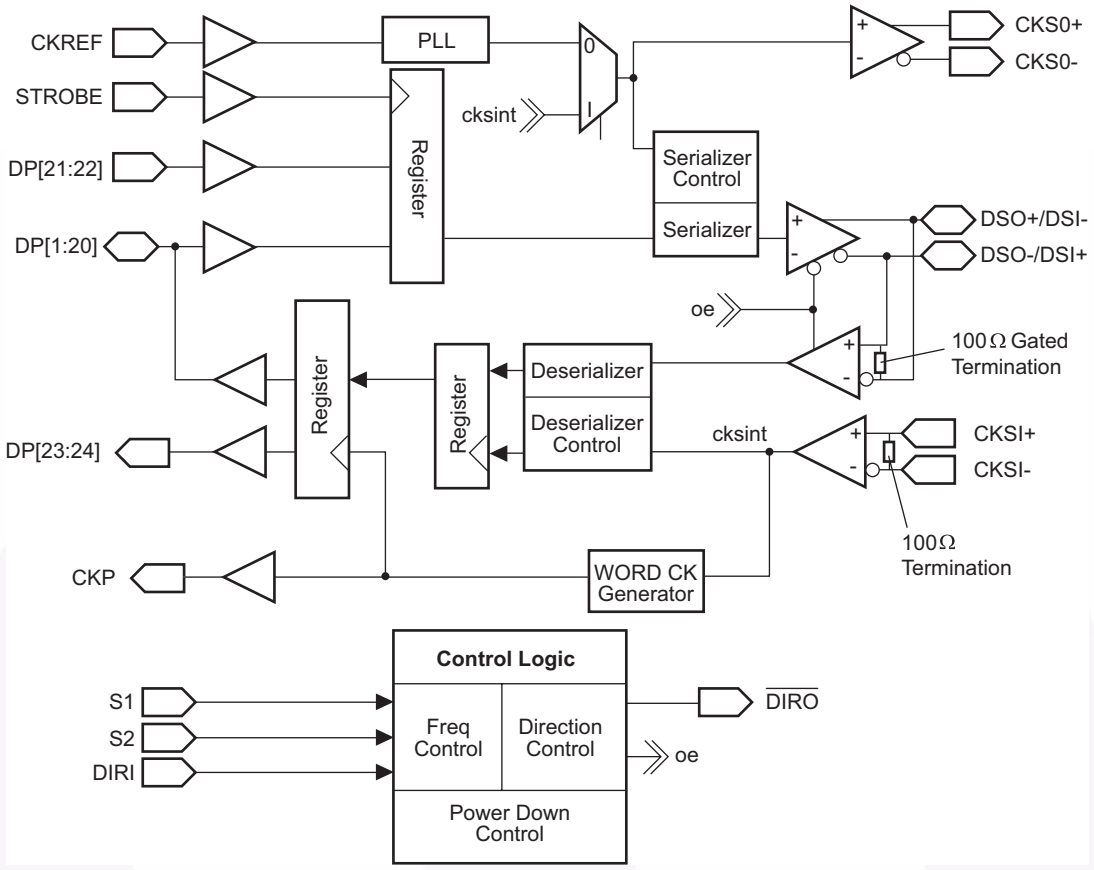


Figure 1. Block Diagram

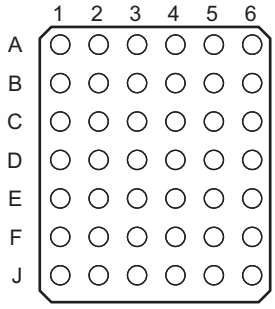
Terminal Description

Terminal Name	I/O Type	Number of Terminals	Description of Signals
DP[1:20]	I/O	20	LVCMOS Parallel I/O, direction controlled by DIRI pin
DP[21:22]	I	2	LVCMOS Parallel Unidirectional Inputs
DP[23:24]	O	2	LVCMOS Unidirectional Parallel Outputs
CKREF	IN	1	LVCMOS Clock Input and PLL Reference
STROBE	IN	1	LVCMOS Strobe Signal for Latching Data into the Serializer
CKP	OUT	1	LVCMOS Word Clock Output
DSO+ / DSI– DSO– / DSI+	DIFF-I/O	2	CTL Differential Serial I/O Data Signals(1) DSO: Refers to output signal pair DSI: Refers to input signal pair DSO(I)+: Positive signal of DSO(I) pair DSO(I)–: Negative signal of DSO(I) pair
CKSI+, CKSI–	DIFF-IN	2	CTL Differential Deserializer Input Bit Clock CKSI: Refers to signal pair CKSI+: Positive signal of CKSI pair CKSI–: Negative signal of CKSI pair
CKSO+, CKSO–	DIFF-OUT	2	CTL Differential Serializer Output Bit Clock CKSO: Refers to signal pair CKSO+: Positive signal of CKSO pair CKSO–: Negative signal of CKSO pair
S1	IN	1	LVCMOS Mode Selection terminals used to select Frequency Range for the RefClock, CKREF
S2	IN	1	
DIRI	IN	1	LVCMOS Control Input Used to control direction of Data Flow: DIRI = “1” Serializer, DIRI = “0” Deserializer
$\overline{\text{DIRO}}$	OUT	1	LVCMOS Control Output Inversion of DIRI
V_{DDP}	Supply	1	Power Supply for Parallel I/O and Translation Circuitry
V_{DDS}	Supply	1	Power Supply for Core and Serial I/O
V_{DDA}	Supply	1	Power Supply for Analog PLL Circuitry
GND	Supply	0	Use Bottom Ground Plane for Ground Signals

Note:

1 The DSO/DSI serial port terminals have been arranged such that when one device is rotated 180° to the other device, the serial connections properly align without the need for any traces or cable signals to cross. Other layout orientations may require that traces or cables cross.

Connection Diagrams



(Top View)

Pin Assignments

	1	2	3	4	5	6
A	DP[9]	DP[7]	DP[5]	DP[3]	DP[1]	CKREF
B	DP[11]	DP[10]	DP[6]	DP[2]	STROBE	$\overline{\text{DIRO}}$
C	CKP	DP[12]	DP[8]	DP[4]	CKSO+	CKSO-
D	DP[13]	DP[14]	V_{DDP}	GND	DSO- / DSI+	DSO+ / DSI-
E	DP[15]	DP[16]	GND	V_{DDS}	CKSI+	CKSI-
F	DP[17]	DP[18]	DP[21]	V_{DDA}	S2	DIRI
J	DP[19]	DP[20]	DP[22]	DP[23]	DP[24]	S1

Figure 2. Terminal Assignments for µBGA

Control Logic Circuitry

The FIN24AC has the ability to be used as a 24-bit Serializer or a 24-bit Deserializer. Pins S1 and S2 must be set to accommodate the clock reference input frequency range of the serializer. Table 1 shows the pin programming of these options based on the S1 and S2 control pins. The DIRI pin controls whether the device is a serializer or a deserializer. When DIRI is asserted LOW, the device is configured as a deserializer. When the DIRI pin is asserted HIGH, the device is configured as a serializer. Changing the state on the DIRI signal reverses the direction of the I/O signals and generates the opposite state signal on $\overline{\text{DIRO}}$. For unidirectional operation, the DIRI pin should be hardwired to the HIGH or LOW state and the $\overline{\text{DIRO}}$ pin should be left floating. For bi-directional operation, the DIRI of the master device is driven by the system and the $\overline{\text{DIRO}}$ signal of the master is used to drive the DIRI of the slave device.

Serializer/Deserializer with Dedicated I/O Variation

The serialization and deserialization circuitry is setup for 24 bits. Because of the dedicated inputs and outputs, only 22 bits of data are serialized or deserialized. Bits 23 and 24 of the serializer always contain the value of zero and are discarded by the deserializer. DP[21:22] inputs to the serializer are transmitted to DP[23:24] outputs on the deserializer.

Turn-Around Functionality

The device passes and inverts the $\overline{\text{DIRI}}$ signal through the device asynchronously to the $\overline{\text{DIRO}}$ signal. Care must be taken during design to ensure that no contention occurs between the deserializer outputs and the other devices on this port. Optimally the peripheral device driving the serializer should be in a HIGH-impedance state prior to the DIRI signal being asserted.

When a device with dedicated data outputs turns from a deserializer to a serializer, the dedicated outputs remain at the last logical value asserted. This value only changes if the device is once again turned around into a deserializer and the values are overwritten.

Power-Down Mode: (Mode 0)

Mode 0 is used for powering down and resetting the device. When both of the mode signals are driven to a LOW state, the PLL and references are disabled, differential input buffers are shut off, differential output buffers are placed into a HIGH-impedance state, LVCMOS outputs are placed into a HIGH-impedance state, LVCMOS inputs are driven to a valid level internally, and all internal circuitry is reset. The loss of CKREF state is also enabled to ensure that the PLL only powers up if there is a valid CKREF signal.

In a typical application, signals do not change states other than between the desired frequency range and the power-down mode. This allows for system-level power-down functionality to be implemented via a single wire for a SerDes pair. The S1 and S2 selection signals that have their operating mode driven to a “logic 0” should be hardwired to GND. The S1 and S2 signals that have their operating mode driven to a “logic 1” should be connected to a system level power-down signal.

Table 1. Control Logic Circuitry

Mode Number	S2	S1	DIRI	Description
0	0	0	x	Power-Down Mode
1	0	1	1	24-Bit Serializer, 2MHz to 5MHz CKREF
	0	1	0	24-Bit Deserializer
2	1	0	1	24-Bit Serializer, 5MHz to 15MHz CKREF
	1	0	0	24-Bit Deserializer
3	1	1	1	24-Bit Serializer, 10MHz to 20MHz CKREF
	1	1	0	24-Bit Deserializer

Serializer Operation Mode

Serializer configurations are described in the following sections. The basic serialization circuitry works essentially the same in these modes, but actual data and clock streams differ depending on CKREF matching the STROBE signal. When the CKREF equals STROBE, the CKREF and STROBE signals have an identical frequency of operation, but may or may not be phase aligned. When CKREF does not equal STROBE, each signal is distinct and CKREF must be running at a frequency high enough to avoid any loss of data condition. CKREF must never be a lower frequency than STROBE.

Serializer Operation: MODE 1, 2, or 3; DIRI = 1, CKREF = STROBE

The Phase-Locked Loop (PLL) must receive a stable CKREF signal to achieve lock prior to any valid data being sent. The CKREF signal can be used as the data STROBE signal, provided that data can be ignored during the PLL lock phase.

Once the PLL is stable and locked, the device can begin to capture and serialize data. Data is captured on the rising edge of the STROBE signal and serialized. When in serializer mode, the internal deserializer circuitry is disabled; including the serial clock, serial data input buffers, the bi-directional parallel outputs, and the CKP word clock. The CKP word clock is driven HIGH.

Serailizer Operation: DIRI = 1, CKREF Does Not = STROBE

If the same signal is not used for CKREF and STROBE, the CKREF signal must be run at a higher frequency than the STROBE rate to serialize the data correctly. The actual serial transfer rate remains at 26 times the CKREF frequency. A data bit value of zero is sent when no valid data is present in the serial bit stream. The operation of the serializer otherwise remains the same. The exact frequency that the reference clock needs is dependent upon the stability of the CKREF and STROBE signal. If the source of the CKREF signal implements spread spectrum technology, the minimum frequency of this spread spectrum clock should be used in calculating the ratio of STROBE frequency to the CKREF frequency. If the STROBE signal has significant cycle-to-cycle variation, the maximum cycle-to-cycle time needs to be factored into the selection of the CKREF frequency.

Serializer Operation: DIRI = 1, No CKREF

A third method of serialization can be accomplished with a free running bit clock on the CKSI signal. This mode is enabled by grounding the CKREF signal and driving the DIRI signal HIGH.

At power-up, the device is configured to accept a serialization clock from CKSI. If a CKREF is received, this device enables the CKREF serialization mode. The device remains in this mode even if CKREF is stopped. To re-enable this mode, the device must be powered down and powered back up with a “logic 0” on CKREF.

Deserializer Operation Mode

The operation of the deserializer is dependent on the data received on the DSI data signal pair and the CKSI clock signal pair. The following sections describe the operation of the deserializer under distinct serializer source conditions. References to the CKREF and STROBE signals refer to signals associated with the serializer device generating the serial data and clock signals that are inputs to the deserializer.

In deserializer mode, the internal serializer circuitry is disabled; including the parallel data input buffers. If there is a CKREF signal provided, the CKSO serial clock continues to transmit bit clocks. Upon device power-up (S1 or S2 = 1), all deserializer output data pins are driven LOW until valid data is passed through the deserializer.

Deserializer Operation: DIRI = 0, (Serializer Source: CKREF = STROBE)

When the DIRI signal is asserted LOW, the device is configured as a deserializer. Data is captured on the serial port and deserialized through use of the bit clock sent with the data.

Deserializer Operation: DIRI = 0, (Serializer Source: CKREF Does Not = STROBE)

The logical operation of the deserializer remains the same if the CKREF is equal in frequency to the STROBE or at a higher frequency than the STROBE. The actual serial data stream presented to the deserializer, however, differs because it has non-valid data bits sent between words. The duty cycle of CKP varies based on the ratio of the frequency of the CKREF signal to the STROBE signal. The frequency of the CKP signal is equal to the STROBE frequency. The LOW time of the CKP signal is equal to half (13 bit times) of the CKREF period. The CKP HIGH time is equal to STROBE period - half of the CKREF period.

LVCMOS Data I/O

The LVCMOS input buffers have a nominal threshold value equal to half V_{DDP}. The input buffers are only operational when the device is operating as a serializer. When the device is operating as a deserializer, the inputs are gated off to conserve power.

The LVCMOS 3-STATE output buffers are rated for a source/sink current of 2mA at 1.8V. The outputs are active when the DIRI signal is asserted LOW. When the DIRI signal is asserted HIGH, the bi-directional LVCMOS I/Os are in a HIGH-Z state. Under purely capacitive load conditions, the output swings between GND and V_{DDP}.

Unused LVCMOS input buffers must be tied off to either a valid logic LOW or a valid logic HIGH level to prevent static current draw due to a floating input. Unused LVCMOS output should be left floating. Unused bi-directional pins should be connected to GND through a high-value resistor. If a FIN24AC device is configured as an unidirectional serializer, unused data I/O can be treated as unused inputs. If hardwired as a deserializer, unused data I/O can be treated as unused outputs.

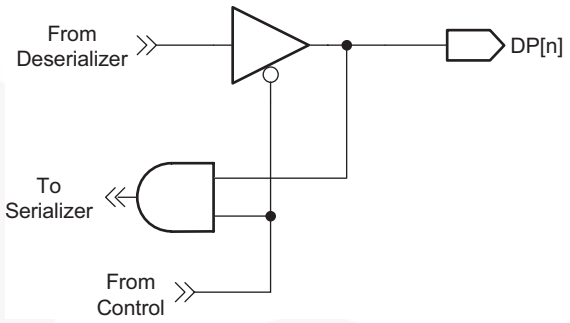


Figure 3. LVCMOS I/O

Application Mode Diagrams

Unidirectional Data Transfer

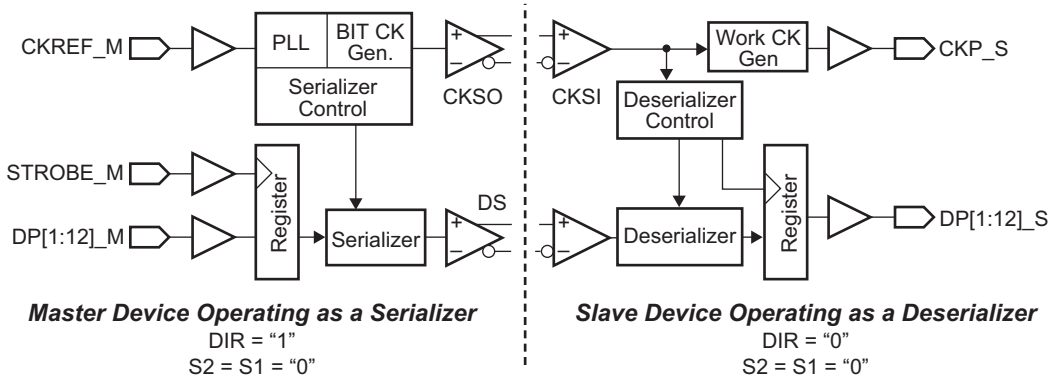


Figure 4. Simplified Block Diagram for Unidirectional Serializer and Deserializer

Figure 5 shows basic operation when a pair of SerDes is configured in an unidirectional operation mode.

In Master Operation, the device:

1. Is configured as a serializer at power-up based on the value of the DIRI signal.
2. Accepts CKREF_M word clock and generates a bit clock, which is sent to the slave device through the CKSO port.
3. Receives parallel data on the rising edge of STROBE_M.
4. Generates and transmits serialized data on the DS signals source synchronously with CKSO.
5. Generates an embedded word clock for each strobe signal.

In Slave Operation, the device:

1. Is configured as a deserializer at power-up based on the value of the DIRI signal.
2. Accepts the bit clock on CKSI.
3. Deserializes the DS data stream using the CKSI input clock.
4. Writes parallel data onto the DP_S port and generates the CKP_S (only when a valid data word occurs).

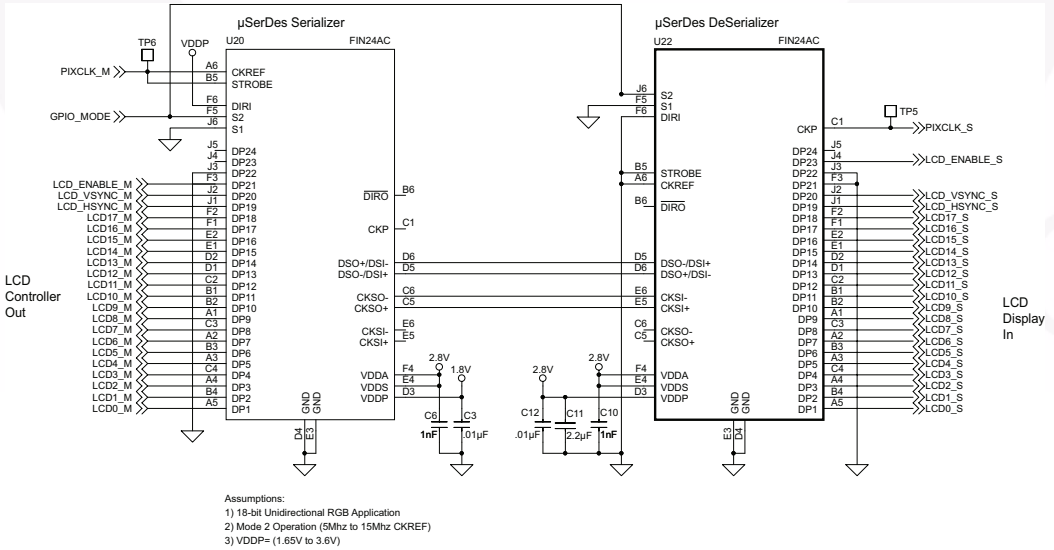


Figure 5. FIN24AC RGB

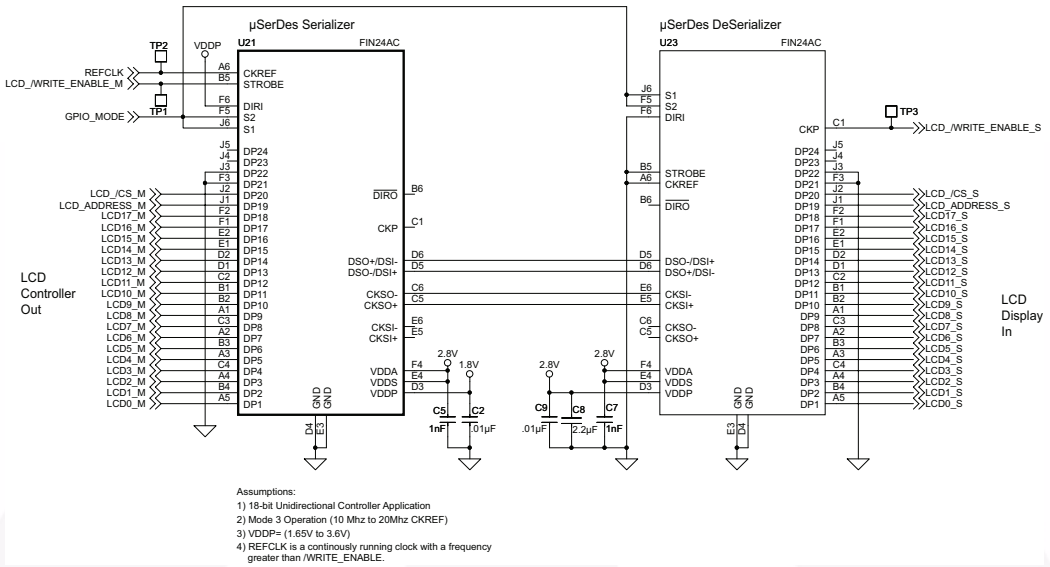


Figure 6. FIN24AC Microcontroller

Figure 6 shows a half-duplex connectivity diagram. This connectivity allows for two unidirectional data streams to be sent across a single pair of SerDes devices. Data is sent on a frame-by-frame basis. For this mode, there must be some synchronization between when the camera sends its data frame and when the LCD sends its data. One option is to have the LCD send data during the camera blanking period. External logic may be needed for this mode of operation.

Devices alternate frames of data controlled by a direction control and a direction sense. When DIRI on the right-hand FIN24AC is HIGH, data is sent from the camera to the camera interface at the base. When DIRI on the right-hand FIN24AC goes LOW, is sent from the baseband process to the LCD. The direction is then changed at $\overline{\text{DIRO}}$ on the right-hand FIN24AC, indicating to the left-hand FIN24AC to change direction. Data is sent from the base LCD unit to the LCD. The $\overline{\text{DIRO}}$ pin on the left-hand FIN24AC is used to indicate to the base control unit that the signals are changing direction and the LCD is available to receive data. DIRI on the right-hand FIN24AC could typically use a timing reference signal, such as VSYNC from the camera interface, to indicate direction change. A derivative of this signal may be required to make sure that no data is lost in the final data transfer.

Flex Circuit Design Guidelines

The serial I/O information is transmitted at a high serial rate. Care must be taken implementing this serial I/O flex cable. The following best practices should be used when developing the flex cabling or Flex PCB:

- Keep all four differential wires the same length.
- Allow no noisy signals over or near differential serial wires. Example: No LVCMOS traces over differential wires.
- Use only one ground plane or wire over the differential serial wires. Do not run ground over top and bottom.
- Do not place test points on differential serial wires.
- Use differential serial wires a minimum of 2cm away from the antenna.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage	-0.5	+4.6	V
	ALL Input/Output Voltage	-0.5	+4.6	V
I_{OS}	CTL™ Output Short-Circuit Duration	Continuous		
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Maximum Junction Temperature		+150	°C
T_L	Lead Temperature (Soldering, 4 Seconds)		+260	°C
ESD	Human Body Model, JESD22-A114, Serial I/O Pins		8.0	kV
	Human Body Model, JESD22-A114, All Pins		2.0	
	Charged Device Model, JESD22-C101		1.5	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DDA}, V_{DDS}	Supply Voltage	2.5	2.9	V
V_{DDP}	Supply Voltage	1.65	3.6	V
T_A	Operating Temperature	-30	+70	°C
V_{DDA-PP}	Supply Noise Voltage		100	mV_{PP}

DC Electrical Characteristics

Values are provided for over-supply voltage and operating temperature ranges, unless otherwise specified.Typical values are given for V_{DD} = 2.775V and T_A = 25°C. Positive current values refer to the current flowing into device and negative values means current flowing out of pins. Voltage is referenced to GROUND unless otherwise specified (except ΔV_{OD} and V_{OD}).

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
LVCMOS I/O							
V_{IH}	Input High Voltage			0.65 x V_{DDP}		V_{DDP}	V
V_{IL}	Input Low Voltage			GND		0.35 x V_{DDP}	V
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	V_{DDP} = 3.3 ± 0.3	0.75 x V_{DDP}			V
			V_{DDP} = 2.5 ± 0.2				
			V_{DDP} = 1.8 ± 0.15				
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	V_{DDP} = 3.3 ± 0.3			0.25 x V_{DDP}	V
			V_{DDP} = 2.5 ± 0.2				
			V_{DDP} = 1.8 ± 0.15				
I_{IN}	Input Current	V_{IN} = 0V to 3.6V		–5.0		5.0	µA
DIFFERENTIAL I/O							
I_{ODH}	Output High Source Current	V_{OS} = 1.0V, Figure 8.			–1.75		mA
I_{ODL}	Output Low Sink Current	V_{OS} = 1.0V, Figure 8.			0.950		mA
I_{OZ}	Disabled Output Leakage Current	CKSO, DSO = 0V to V_{DDS}, S2 = S1 = 0V			±0.1	±5.0	µA
I_{IZ}	Disabled Input Leakage Current	CKSI, DSI = 0V to V_{DDS}, S2 = S1 = 0V			±0.1	±5.0	µA
V_{ICM}	Input Common Mode Range	V_{DDS} = 2.775 ± 5%			V_{GO} + 0.80		V
V_{GO}	Input Voltage Ground Offset Relative to Driver(2)	Figure 9.			0		V
R_{TRM}	CKSI Internal Receiver Termination Resistor	V_{ID} = 50mV, V_{IC} = 925mV, DIRI = 0, | CKSI+ – CKSI- | = V_{ID}		80.0	100	120	Ω
R_{TRM}	DSI Internal Receiver, Termination Resistor	V_{ID} = 50mV, V_{IC} = 925mV, DIRI = 0, | DSI+ – DSI- | = V_{ID}		80.0	100	120	Ω

Note:

2 V_{GO} is the difference in device ground levels between the CTL driver and the CTL receiver.

Power Supply Currents

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Units
I_{DDA1}	V_{DDA} Serializer Static Supply Current	All DP and Control Inputs at 0V or V_{DD}, No CKREF, S2 = 0, S1 = 1, DIR = 1				450		µA
I_{DDA2}	V_{DDA} Deserializer Static Supply Current	All DP and Control Inputs at 0V or V_{DD}, No CKREF, S2 = 0, S1 = 1, DIR = 0				550		µA
I_{DDS1}	V_{DDS} Serializer Static Supply Current	All DP and Control Inputs at 0V or V_{DD}, No CKREF, S2 = 0, S1 = 1, DIR = 1				4.0		mA
I_{DDS2}	V_{DDS} Deserializer Static Supply Current	All DP and Control Inputs at 0V or V_{DD}, No CKREF, S2 = 0, S1 = 1, DIR = 0				4.5		mA
I_{DD_PD}	V_{DD} Power-Down Supply Current $I_{DD\_PD} = I_{DDA} + I_{DDS} + I_{DDP}$	S1 = S2 = 0, All Inputs at GND or V_{DD}				0.1		µA
I_{DD_SER1}	26:1 Dynamic Serializer Power Supply Current $I_{DD\_SER1} = I_{DDA} + I_{DDS} + I_{DDP}$	CKREF = STROBE DIRI = H Figure 10.	S2 = L, S1 = H	2MHz		9.0		mA
				5MHz		14.0		
			S2 = H, S1 = L	5MHz		9.5		
				15MHz		17.0		
			S2 = H, S1 = H	10MHz		11.0		
				20MHz		15.5		
I_{DD_DES1}	1:26 Dynamic Deserializer Power Supply Current $I_{DD\_DES1} = I_{DDA} + I_{DDS} + I_{DDP}$	CKREF = STROBE DIRI = L Figure 10.	S2 = L, S1 = H	2MHz		5.5		mA
				5MHz		6.0		
			S2 = H, S1 = L	5MHz		4.0		
				15MHz		5.5		
			S2 = H, S1 = H	10MHz		7.5		
				20MHz		10.0		
I_{DD_SER2}	26:1 Dynamic Serializer Power Supply Current $I_{DD\_SER2} = I_{DDA} + I_{DDS} + I_{DDP}$	NO CKREF STROBE → Active CKSI = 15X Strobe DIRI = H, Figure 10.		2MHz		8.0		mA
				5MHz		8.5		
				10MHz		10.0		
				15MHz		12.0		

AC Electrical Characteristics

Values are provided for over-supply voltage and operating temperature ranges, unless otherwise specified. Typical values are given for V_{DD} = 2.775V and T_A = 25°C. Positive current values refer to the current flowing into device and negative values refer to current flowing out of pins. Voltage is referenced to GROUND unless otherwise specified (except ΔV_{OD} and V_{OD}).

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
SERIALIZER INPUT OPERATING CONDITIONS							
t_{TCP}	CKREF Clock Period (2MHz–20MHz)	Figure 14. CKREF = STROBE	S2 = 0, S1 = 1	200.0		500	ns
			S2 = 1, S1 = 0	66.0		200	
			S2 = 1, S1 = 1	50.0		100	
f_{REF}	CKREF Frequency Relative to Strobe Frequency	CKREF does not equal STROBE	S2 = 0, S1 = 1	1.1 x f_{ST}		5.0	MHz
			S2 = 1, S1 = 0			15.0	
			S2 = 1, S1 = 1			20.0	
t_{CPWH}	CKREF Clock High Time	Figure 14.		0.2	0.5		T
t_{CPWL}	CKREF Clock Low Time			0.2	0.5		T
t_{CLKT}	LVCMOS Input Transition Time	Figure 14.				90.0	ns

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
t_{SPWH}	STROBE Pulse Width HIGH/LOW	Figure 14.		(T x 4) / 26		(T x 22) / 26	ns
f_{MAX}	Maximum Serial Data Rate	CKREF x 26	S2 = 0 S1 = 1	52.0		130	Mb/s
			S2 = 1 S1 = 0	130		390	
			S2 = 1 S1 = 1	260		520	
t_{STC}	$DP_{(n)}$ Setup to STROBE	DIRI = 1		2.5			ns
t_{HTC}	$DP_{(n)}$ Hold to STROBE	Figure 13. (f = 5MHz)		2.0			ns
f_{REF}	CKREF Frequency Relative to Strobe Frequency	CKREF Does Not Equal STROBE		1.1 x f_{STROBE}		20.0	MHz
SERIALIZER AC ELECTRICAL CHARACTERISTICS							
t_{TCCD}	Transmitter Clock Input to Clock Output Delay	DIRI = 1, CKREF = STROBE		33a + 1.5		35a + 6.5	ns
t_{SPOS}	CKSO Position Relative to DS(3)	Figure 18.		–50.0		250	ps
PLL AC ELECTRICAL CHARACTERISTICS							
t_{TPLLS0}	Serializer PLL Stabilization Time	Figure 16.				200	µs
t_{TPLLD0}	PLL Disable Time Loss of Clock	Figure 19.				30.0	µs
t_{TPLLD1}	PLL Power-Down Time(4)	Figure 20.				20.0	ns
DESERIALIZER INPUT OPERATION CONDITIONS							
t_{S_DS}	Serial Port Setup Time(5) DS-to-CKSI	Figure 17.		1.4			ns
t_{H_DS}	Serial Port Hold Time(5) DS-to-CKS	Figure 17.		–250			ps
DESERIALIZER AC ELECTRICAL CHARACTERISTICS							
t_{RCOP}	Deserializer Clock Output (CKP OUT) Period	Figure 15.		50.0		500	ns
t_{RCOL}	CKP OUT Low Time	Figure 15. (Rising Edge Strobe) Serializer Source STROBE = CKREF where a = (1/f) / 26		13a-3		13a+3	ns
t_{RCOH}	CKP OUT High Time(6)			13a-3		13a+3	ns
t_{PDV}	Data Valid to CKP LOW(6)	Figure 15. (Rising Edge Strobe) where a = (1/f) / 26		8a-6		8a+1	ns
t_{ROLH}	Output Rise Time (20% to 80%)	C_L = 5pF, Figure 12.			2.5		ns
t_{ROHL}	Output Fall Time (80% to 20%)				2.5		ns

Notes:

3 Skew is measured form either the rising or falling edge of CKSO clock to the rising or falling edge of data (DSO). Signals are edge aligned. Both outputs should have identical load conditions for this test to be valid.

4 The power-down time is a function of the CKREF frequency prior to CKREF being stopped HIGH or LOW and the state of the S1/S2 mode pins. The specific number of clock cycles required for the PLL to be disabled varies based on the operating mode of the device.

5 Signals are transmitted from the serializer source synchronously. In some cases, data is transmitted when the clock remains at a high state. Skew should only be measured when data and clock are transitioning at the same time. Total measured input skew is a combination of output skew from the serializer, load variations, and ISI and jitter effects.

6 Rising edge of CKP appears approximately 13 bit times after the falling edge of the CKP output. Falling edge of CKP occurs approximately eight bit times after a data transition or six bit times after the falling edge of CKSO. Variation of the data with respect of the CKP signal is due to internal propagation delay differences of the data and CKP path and propagation delay differences on the various data pins. If the CKREF is not equal to STROBE for the serializer, the CKP signal does not maintain a 50% duty cycle. The low time of CKP remains 13 bit times.

Control Logic Timing Controls

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL_DIR}, t_{PLH_DIR}	Propagation Delay DIRI-to-$\overline{DIRO}$	DIRI LOW-to-HIGH or HIGH-to-LOW			17	ns
t_{PLZ}, t_{PHZ}	Propagation Delay DIRI-to-DP	DIRI LOW-to-HIGH			25	ns
t_{PZL}, t_{PZH}	Propagation Delay DIRI-to-DP	DIRI HIGH-to-LOW			25	ns
t_{PLZ}, t_{PHZ}	Deserializer Disable Time: S0 or S1 to DP	DIRI = 0, S1(2) = 0 and S2(1) = LOW-to-HIGH, Figure 22.			25	ns
t_{PZL}, t_{PZH}	Deserializer Enable Time: S0 or S1 to DP	DIRI = 0,(7) S1(2) = 0 and S2(1) = LOW-to-HIGH, Figure 22.			2	µs
t_{PLZ}, t_{PHZ}	Serializer Disable Time: S0 or S1 to CKSO, DS	DIRI = 1, S1(2) = 0 and S2(1) = HIGH-to-LOW, Figure 21.			25	ns
t_{PZL}, t_{PZH}	Serializer Enable Time: S0 or S1 to CKSO, DS	DIRI = 1, S1(2) and S2(1) = LOW-to-HIGH, Figure 21.			65	ns

Note:

7 Deserializer Enable Time includes the amount of time required for internal voltage and current references to stabilize. This time is significantly less than the PLL lock time and does not impact overall system startup time.

Capacitance

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Capacitance of Input Only Signals, CKREF, STROBE, S1, S2, DIRI	DIRI = 1, S1 = S2 = 0, V_{DD} = 2.5V		2		pF
C_{IO}	Capacitance of Parallel Port Pins $DP_{1:12}$	DIRI = 1, S1 = S2 = 0, V_{DD} = 2.5V		2		pF
$C_{IO-DIFF}$	Capacitance of Differential I/O Signals	DIRI = 0, S1 = S2 = 0, V_{DD} = 2.775V		2		pF

AC Loading and Waveforms

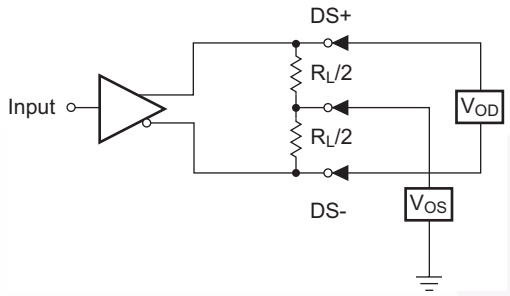


Figure 8. Differential CTL Output DC Test Circuit

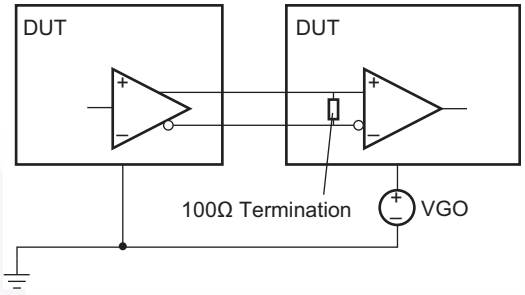
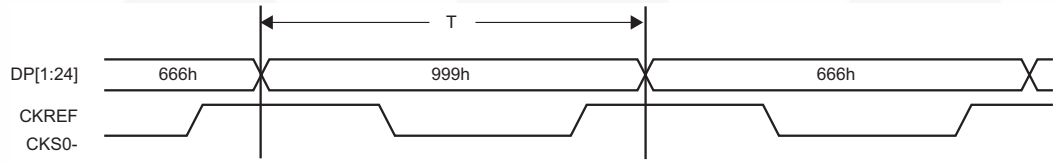


Figure 9. CTL Input Common Mode Test Circuit



Note:
The "worst-case" test pattern produces a maximum toggling of internal digital curcuits, CTL I/O and LVCMOS I/O with PLL operating at the reference frequency, unless otherwise specified. Maximum power is measured at the maximum V_{DD} values. Minimum values are measured at the minimum V_{DD} values. Typical values are measured at V_{DD} = 2.5V.

Figure 10. "Worst-Case" Serializer Test Pattern

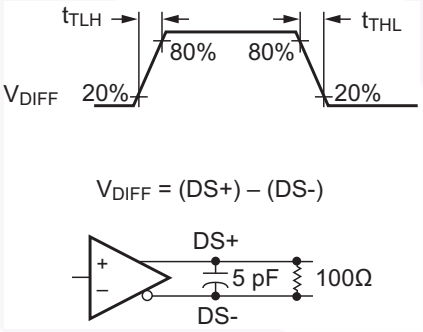


Figure 11. CTL Output Load and Transition Times

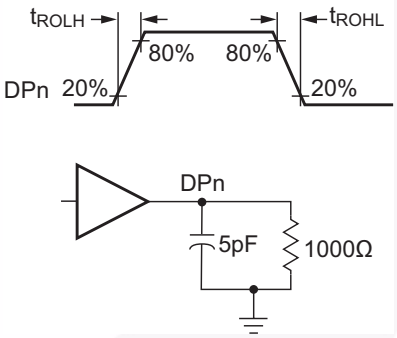
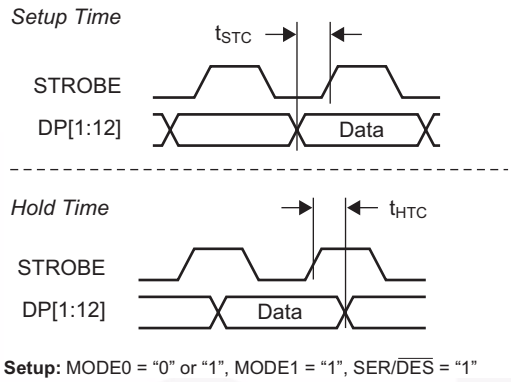


Figure 12. LVCMOS Output Load and Transition Times

AC Loading and Waveforms (Continued)



Setup: MODE0 = "0" or "1", MODE1 = "1", SER/$\overline{DES}$ = "1"

Figure 13.Serial Setup and Hold Time

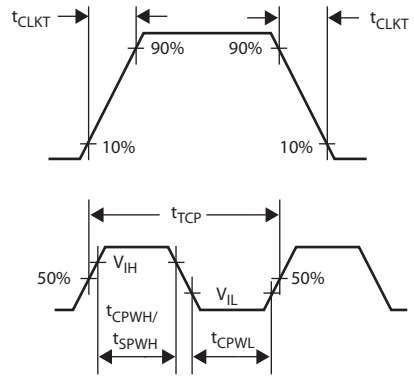
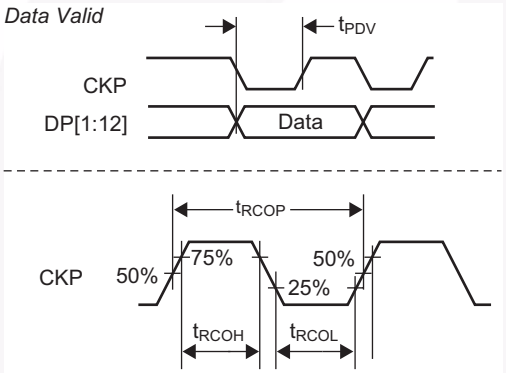
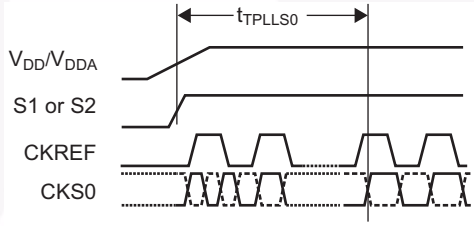


Figure 14. LVCMOS Clock Parameters



Setup: EN_DES = "1", CKSI, and DSI are valid signals.

Figure 15. Deserializer Data Valid Window Time and Clock Output Parameters



Note: CKREF Signal is free running.

Figure 16. Serializer PLL Lock Time

AC Loading and Waveforms (Continued)

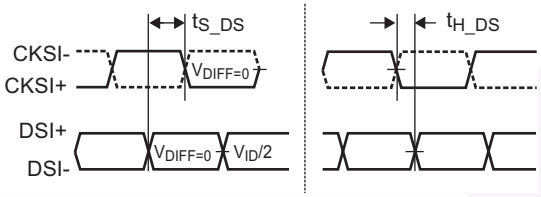
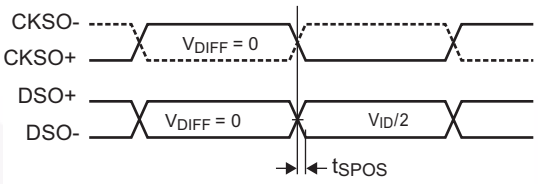
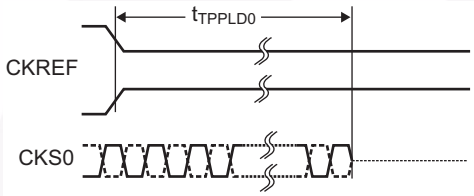


Figure 17.Differential Input Setup and Hold Times



Note: Data is typically edge aligned with the clock.

Figure 18. Differential Output Signal Skew



Note: CKREF Signal can be stopped either HIGH or LOW.

Figure 19. PLL Loss of Clock Disable Time

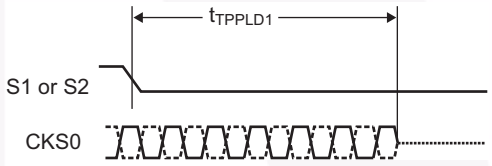
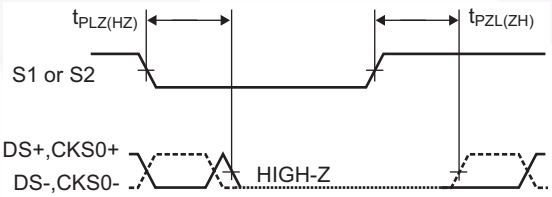
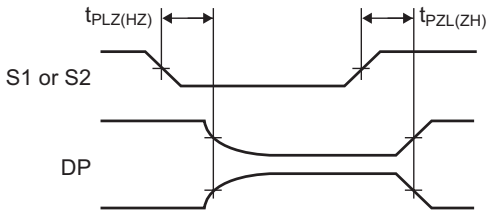


Figure 20. PLL Power-Down Time



Note: CKREF must be active and PLL must be stable.

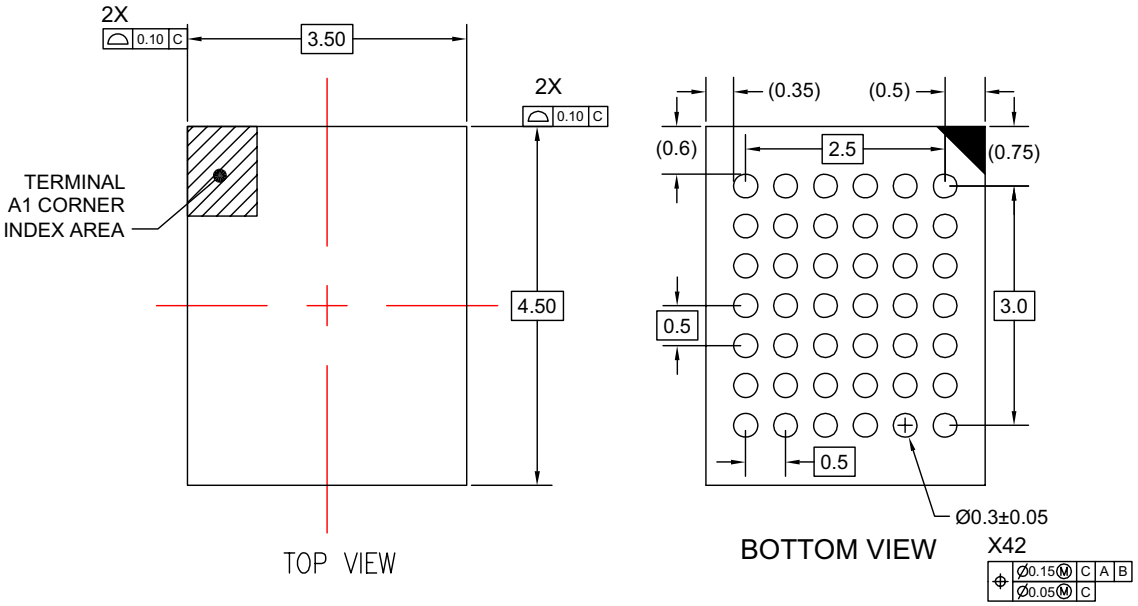
Figure 21. Serializer Enable and Disable Time

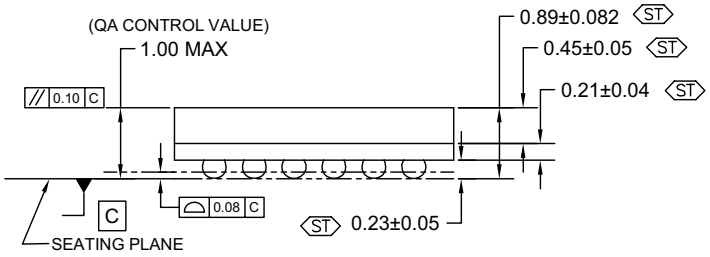


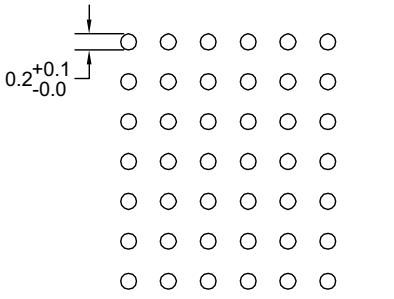
Note: If S1(2) transitioning, S2(1) must = 0 for test to be valid.

Figure 22. Deserializer Enable and Disable Times

Physical Dimensions







LAND PATTERN
RECOMMENDATION

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−195,
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
D. STATISTICAL TOLERANCING FOR REFERENCE REFER TO MAX DIMENSION FOR QA INSPECTION
E. LAND PATTERN RECOMENDATION PER IPC−7351 TABLE14−15 LAND PATTERN NAME PER TABLE 3−15: BGA50P+6X7−42

BGA42ArevB

Figure 23. 42-Ball, Ultra Small Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5mm Wide

Note: Click here for tape and reel specifications, available at:

http://www.fairchildsemi.com/products/analog/packaging/bga42.html.

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