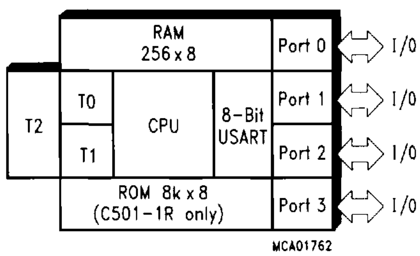
SIEMENS

8-Bit CMOS Microcontroller C501

Preliminary

- Fully compatible to standard 8051 microcontroller
- Versions for 12/24/40 MHz operating frequency
- 8 K × 8 ROM (C501-1R only)
- 256 × 8 RAM
- Four 8-bit ports
- Three 16-bit Timers / Counters (Timer 2 with Up/Down Counter feature)
- USART
- Six interrupt sources, two priority levels
- Power Saving Modes
- P-DIP-40, P-LCC-44 package, and P-MQFP-44
- Temperature ranges: SAB-C501G T_A : 0 °C to 70 °C
  SAF-C501G T_A : – 40 °C to 85 °C
  SAF-C501G T_A : – 40 °C to 110 °C (on request)

C501



The C501-L/C501-1R described in this document is compatible with the SAB 80C32/C52 and can be used for all present SAB 80C52 applications.

The C501-1R contains a non-volatile 8K × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four ports, three 16-bit timers counters, a seven source, two priority level interrupt structure and a serial port. The C501-L is identical, except that it lacks the program memory on chip. Therefore, the term C501 refers to both versions within this specification unless otherwise noted. Further, the term C501 refers to all versions which are available in the different temperature ranges, marked with SAB-C501G.... or SAF-C501G.... .

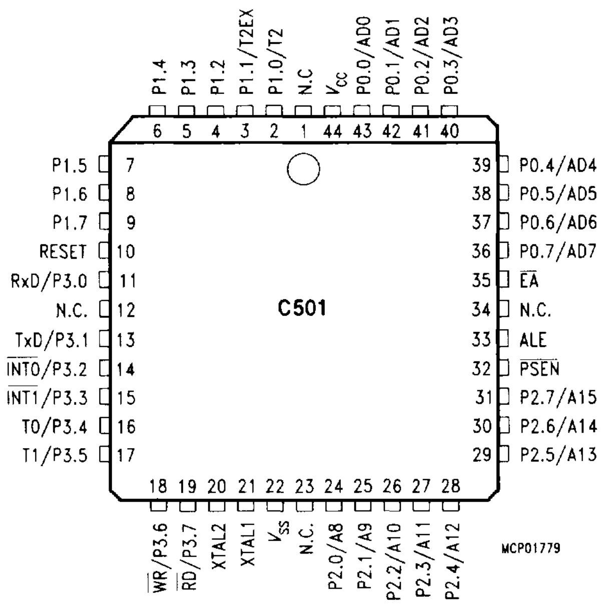
Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
SAB-C501G-LN SAB-C501G-LP SAB-C501G-LM	Q67120-C0969 Q67120-C0968 Q67126-C0970	P-LCC-44 P-DIP-40 P-MQFP-44	for external memory (12 MHz)
SAB-C501G-1RN SAB-C501G-1RP SAB-C501G-1RM	Q67120-DXXX Q67120-DXXX Q67126-DXXX	P-LCC-44 P-DIP-40 P-MQFP-44	with mask-programmable ROM (12 MHz)
SAB-C501G-L24N SAB-C501G-L24P SAB-C501G-L24M	Q67120-C1001 Q67120-C0999 Q67126-C1014	P-LCC-44 P-DIP-40 P-MQFP-44	for external memory (24 MHz)
SAB-C501G-1R24N SAB-C501G-1R24P SAB-C501G-1R24M	Q67120-DXXX Q67120-DXXX Q67126-DXXX	P-LCC-44 P-DIP-40 P-MQFP-44	with mask-programmable ROM (24 MHz)
SAB-C501G-L40N SAB-C501G-L40P SAB-C501G-L40M	Q67120-C1002 Q67120-C1000 Q67126-C1009	P-LCC-44 P-DIP-40 P-MQFP-44	for external memory (40 MHz)
SAB-C501G-1R40N SAB-C501G-1R40P SAB-C501G-1R40M	Q67120-DXXX Q67120-DXXX Q67126-DXXX	P-LCC-44 P-DIP-40 P-MQFP-44	with mask-programmable ROM (40 MHz)
SAF-C501G-LN SAF-C501G-LM	Q67120-C1013 Q67127-C1041	P-LCC-44 P-MQFP-44	for external memory (12 MHz) ext. temp. – 40 °C to 85 °C
SAF-C501G-LN SAF-C501G-LP	Q67120-C1010 Q67120-C1011	P-LCC-44 P-DIP-40	for external memory (24 MHz) ext. temp. – 40 °C to 85 °C
SAF-C501G-L40N	Q67126-C1051	P-LCC-44	for external memory (40 MHz) ext. temp. – 40 °C to 85 °C

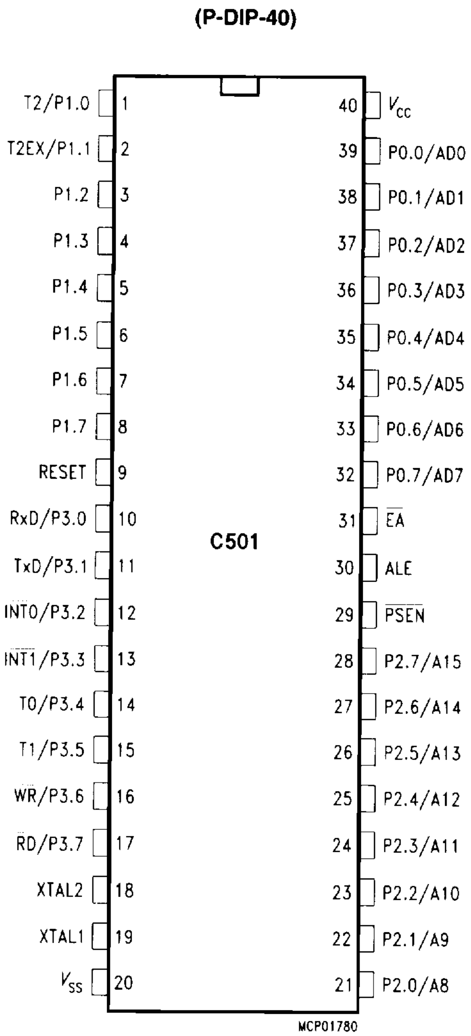
Note: Versions for extended temperature range – 40 °C to 110 °C (SAH-C501G) on request. The ordering number of ROM types (DXXX extensions) is defined after program release (verification) of the customer.

Pin Configuration
(top view)

(P-LCC-44)

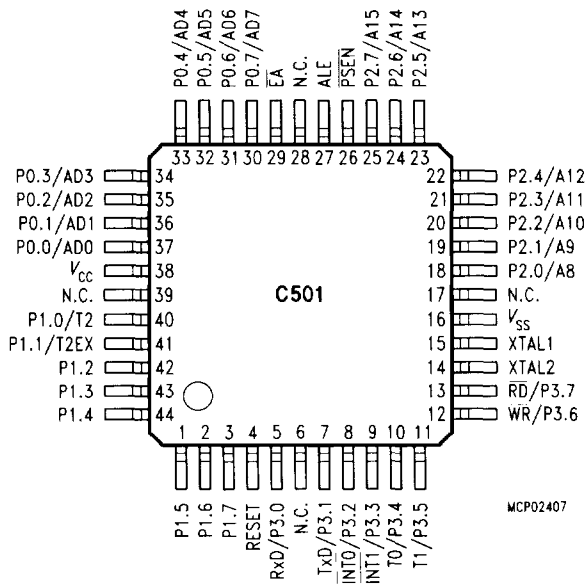


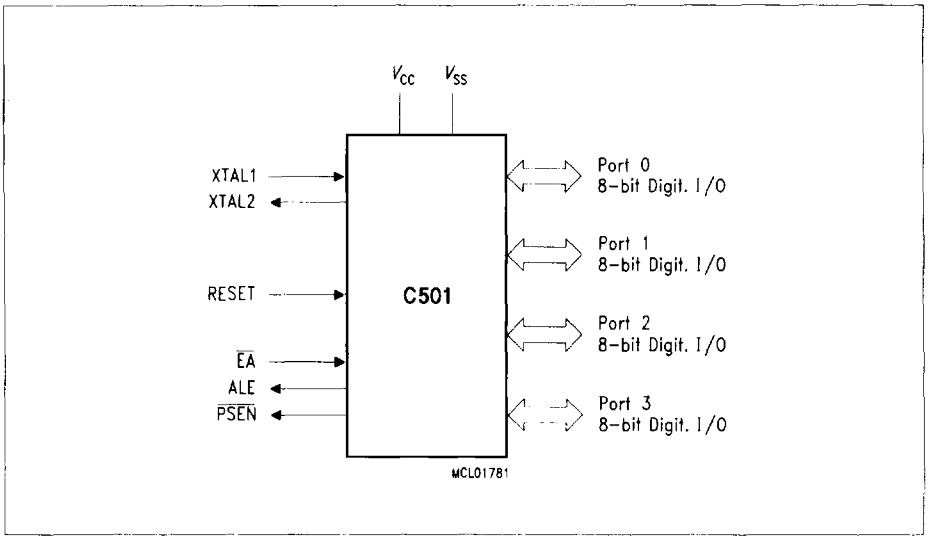
Pin Configuration
(top view)



Pin Configuration
(top view)

(P-MQFP-44)





Logic Symbol

Pin Definitions and Functions

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P1.0 – P1.7	2–9	1–8	40–44, 1–3,	I/O	**Port 1** is a bidirectional I/O port with internal pull-up resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 1 also contains the timer 2 pins as secondary function. The output latch corresponding to a secondary function must be pro-grammed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows:
	2	1	40		P1.0 T2 Input to counter 2
	3	2	41		P1.1 T2EX Capture - Reload trigger of timer 2 / Up-Down count

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P3.0 – P3.7	11, 13–19	10–17	5, 7–13	I/O	**Port 3** is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins which are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows:
	11	10	5		P3.0 R×D receiver data input (asynchronous) or data input output (synchronous) of serial interface 0
	13	11	7		P3.1 T×D transmitter data output (asynchronous) or clock output (synchronous) of the serial interface 0
	14	12	8		P3.2 $\overline{\text{INT0}}$ interrupt 0 input/timer 0 gate control
	15	13	9		P3.3 $\overline{\text{INT1}}$ interrupt 1 input/timer 1 gate control
	16	14	10		P3.4 T0 counter 0 input
	17	15	11		P3.5 T1 counter 1 input
	18	16	12		P3.6 $\overline{\text{WR}}$ the write control signal latches the data byte from port 0 into the external data memory
	19	17	13		P3.7 $\overline{\text{RD}}$ the read control signal enables the external data memory to port 0

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
XTAL2	20	18	14	–	**XTAL2** Output of the inverting oscillator amplifier.
XTAL1	21	19	15	–	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise fall times specified in the AC characteristics must be observed.
P2.0 – P2.7	24–31	21–28	18–25	I/O	**Port 2** is a bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
$\overline{PSEN}$	32	29	26	O	**The Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.
RESET	10	9	4	I	**RESET** A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.
ALE	33	30	27	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	35	31	29	I	**External Access Enable** When held at high level, instructions are fetched from the internal ROM (C501-1R only) when the PC is less than 2000_H. When held at low level, the C501 fetches all instructions from external program memory. For the C501-L this pin must be tied low.

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P0.0 – P0.7	43–36	39–32	37–30	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the C501-1R. External pull-up resistors are required during program verification.
V_{SS}	22	20	16	–	**Circuit ground potential**
V_{CC}	44	40	38	–	**Supply terminal** for all operating modes
N.C.	1, 12, 23, 34	–	6, 17, 28, 39	–	**No connection**

Functional Description

The C501 is fully compatible to the standard 8051 microcontroller family.

It is compatible with the SAB 80C52. While maintaining all architectural and operational characteristics of the SAB 80C52, the C501 incorporates some enhancements in the Timer2 Unit.

Figure 1 shows a block diagram of the C501.

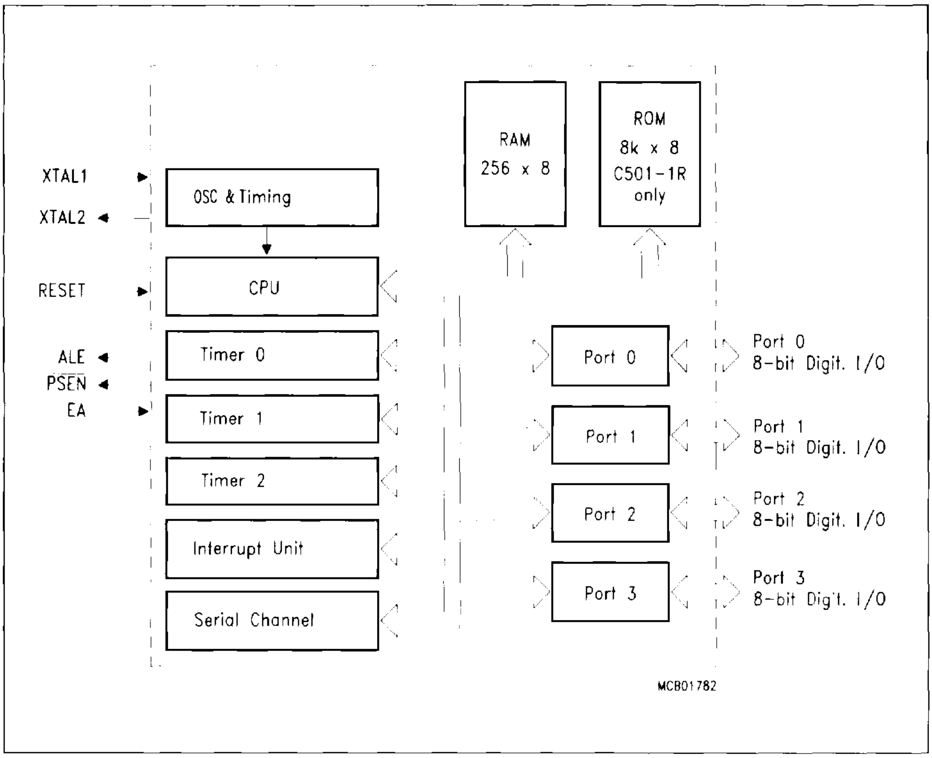


Figure 1
Block Diagram of the C501

CPU

The C501 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15% three- byte instructions. With a 12 MHz crystal, 58% of the instructions are executed in 1.0µs 24 MHz: 500 ns, 40 MHz : 300 ns).

Special Function Register PSW

	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
Addr. $D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit		Function
CY		**Carry Flag**
AC		**Auxiliary Carry Flag** (for BCD operations)
F0		**General Purpose Flag**
RS1	**RS0**	**Register Bank select control bits**
0	0	Bank 0 selected, data address 00_H – 07_H
0	1	Bank 1 selected, data address 08_H – $0F_H$
1	0	Bank 2 selected, data address 10_H – 17_H
1	1	Bank 3 selected, data address 18_H – $1F_H$
OV		**Overflow Flag**
F1		**General Purpose Flag**
P		**Parity Flag** Set/cleared by hardware each instruction cycle to indicate an odd/ even number of “one” bits in the accumulator, i.e. even parity.

Reset value of PSW is 00_H.

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 27 special function registers (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.

All SFRs are listed in **table 1**, **table 2**, and **table 3**.

In **table 1** they are organized in numeric order of their addresses. In **table 2** they are organized in groups which refer to the functional blocks of the C501. **Table 3** illustrates the contents of the SFRs.

Table 1
Special Function Registers in Numeric Order of their Addresses

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80_H	**P0** [1]	**FF_H**	**98_H**	**SCON** [1]	**00_H**
81_H	SP	07_H	99_H	SBUF	XX_H [2]
82_H	DPL	00_H	$9A_H$	reserved	XX_H [2]
83_H	DPH	00_H	$9B_H$	reserved	XX_H [2]
84_H	reserved	XX_H [2]	$9C_H$	reserved	XX_H [2]
85_H	reserved	XX_H [2]	$9D_H$	reserved	XX_H [2]
86_H	reserved	XX_H [2]	$9E_H$	reserved	XX_H [2]
87_H	PCON	$0XXX0000_B$ [2]	$9F_H$	reserved	XX_H [2]
88_H	**TCON** [1]	**00_H**	**$A0_H$**	**P2** [1]	**FF_H**
89_H	TMOD	00_H	$A1_H$	reserved	XX_H [2]
$8A_H$	TL0	00_H	$A2_H$	reserved	XX_H [2]
$8B_H$	TL1	00_H	$A3_H$	reserved	XX_H [2]
$8C_H$	TH0	00_H	$A4_H$	reserved	XX_H [2]
$8D_H$	TH1	00_H	$A5_H$	reserved	XX_H [2]
$8E_H$	reserved	XX_H [2]	$A6_H$	reserved	XX_H [2]
$8F_H$	reserved	XX_H [2]	$A7_H$	reserved	XX_H [2]
90_H	**P1** [1]	**FF_H**	**$A8_H$**	**IE** [1]	**$0X000000_B$** [2]
91_H	reserved	00_H	$A9_H$	reserved	XX_H [2]
92_H	reserved	XX_H [2]	AA_H	reserved	XX_H [2]
93_H	reserved	XX_H [2]	AB_H	reserved	XX_H [2]
94_H	reserved	XX_H [2]	AC_H	reserved	XX_H [2]
95_H	reserved	XX_H [2]	AD_H	reserved	XX_H [2]
96_H	reserved	XX_H [2]	AE_H	reserved	XX_H [2]
97_H	reserved	XX_H [2]	AF_H	reserved	XX_H [2]

[1] Bit-addressable Special Function Register
[2] X means that the value is indeterminate and the location is reserved

Table 1
Special Function Registers in Numeric Order of their Addresses (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
B0$_H$	**P3**[1]	**FF$_H$**	**D8$_H$**	reserved	XX$_H$[2]
B1$_H$	reserved	XX$_H$[2]	D9$_H$	reserved	XX$_H$[2]
B2$_H$	reserved	XX$_H$[2]	DA$_H$	reserved	XX$_H$[2]
B3$_H$	reserved	XX$_H$[2]	DB$_H$	reserved	XX$_H$[2]
B4$_H$	reserved	XX$_H$[2]	DC$_H$	reserved	XX$_H$[2]
B5$_H$	reserved	XX$_H$[2]	DD$_H$	reserved	XX$_H$[2]
N6$_H$	reserved	XX$_H$[2]	DE$_H$	reserved	XX$_H$[2]
B7$_H$	reserved	XX$_H$[2]	DF$_H$	reserved	XX$_H$[2]
B8$_H$	**IP**[1]	**XX000000$_B$**[2]	**E0$_H$**	**ACC**[1]	**00$_H$**
B9$_H$	reserved	XX$_H$[2]	E1$_H$	reserved	XX$_H$[2]
BA$_H$	reserved	XX$_H$[2]	E2$_H$	reserved	XX$_H$[2]
BB$_H$	reserved	XX$_H$[2]	E3$_H$	reserved	XX$_H$[2]
BC$_H$	reserved	XX$_H$[2]	E4$_H$	reserved	XX$_H$[2]
BD$_H$	reserved	XX$_H$[2]	E5$_H$	reserved	XX$_H$[2]
BE$_H$	reserved	XX$_H$[2]	E6$_H$	reserved	XX$_H$[2]
BF$_H$	reserved	XX$_H$[2]	E7$_H$	reserved	XX$_H$[2]
C0$_H$	reserved	XX$_H$[2]	**E8$_H$**	reserved	XX$_H$[2]
C1$_H$	reserved	XX$_H$[2]	E9$_H$	reserved	XX$_H$[2]
C2$_H$	reserved	XX$_H$[2]	EA$_H$	reserved	XX$_H$[2]
C3$_H$	reserved	XX$_H$[2]	EB$_H$	reserved	XX$_H$[2]
C4$_H$	reserved	XX$_H$[2]	EC$_H$	reserved	XX$_H$[2]
C5$_H$	reserved	XX$_H$[2]	ED$_H$	reserved	XX$_H$[2]
C6$_H$	reserved	XX$_H$[2]	EE$_H$	reserved	XX$_H$[2]
C7$_H$	reserved	XX$_H$[2]	EF$_H$	reserved	XX$_H$[2]
C8$_H$	**T2CON**	**00$_H$**	**F0$_H$**	**B**[1]	**00$_H$**
C9$_H$	T2MOD	XXXXXXX0$_B$[2]	F1$_H$	reserved	XX$_H$[2]
CA$_H$	RC2L	00$_H$	F2$_H$	reserved	XX$_H$[2]
CB$_H$	RC2H	00$_H$	F3$_H$	reserved	XX$_H$[2]
CC$_H$	TL2	00$_H$	F4$_H$	reserved	XX$_H$[2]
CD$_H$	TH2	00$_H$	F5$_H$	reserved	XX$_H$[2]
CE$_H$	reserved	XX$_H$[2]	F6$_H$	reserved	XX$_H$[2]
CF$_H$	reserved	XX$_H$[2]	F7$_H$	reserved	XX$_H$[2]
D0$_H$	**PSW**[1]	**00$_H$**	**F8$_H$**	reserved	XX$_H$[2]
D1$_H$	reserved	XX$_H$[2]	F9$_H$	reserved	XX$_H$[2]
D2$_H$	reserved	XX$_H$[2]	FA$_H$	reserved	XX$_H$[2]
D3$_H$	reserved	XX$_H$[2]	FB$_H$	reserved	XX$_H$[2]
D4$_H$	reserved	XX$_H$[2]	FC$_H$	reserved	XX$_H$[2]
D5$_H$	reserved	XX$_H$[2]	FD$_H$	reserved	XX$_H$[2]
D6$_H$	reserved	XX$_H$[2]	FE$_H$	reserved	XX$_H$[2]
D7$_H$	reserved	XX$_H$[2]	FF$_H$	reserved	XX$_H$[2]

[1] Bit-addressable Special Function Register
[2] X means that the value is indeterminate and the location is reserved

Table 2
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**E0H** [1]	00H
	B	B-Register	**F0H** [1]	00H
	DPH	Data Pointer, High Byte	83H	00H
	DPL	Data Pointer, Low Byte	82H	00H
	PSW	Program Status Word Register	**D0H** [1]	00H
	SP	Stack Pointer	81H	07H
Interrupt System	IE	Interrupt Enable Register	**A8H** [1]	0X000000B [2]
	IP	Interrupt Priority Register	**B8H** [1]	XX000000B [2]
Ports	P0	Port 0	**80H** [1]	FFH
	P1	Port 1	**90H** [1]	FFH [3]
	P2	Port 2	**A0H** [1]	FFH
	P3	Port 3	**B0H** [1]	FFH
Serial Channels	PCON [2]	Power Control Register	87H	0XXX0000B [2]
	SBUF	Serial Channel Buffer Reg.	99H	XXH [3]
	SCON	Serial Channel 0 Control Reg.	**98H** [1]	00H
Timer 0 / Timer 1	TCON	Timer 0/1 Control Register	**88H** [1]	00H
	TH0	Timer 0, High Byte	8CH	00H
	TH1	Timer 1, High Byte	8DHH	00H
	TL0	Timer 0, Low Byte	8AH	00H
	TL1	Timer 1, Low Byte	8BH	00H
	TMOD	Timer Mode Register	89H	00H
Timer 2	T2CON	Timer 2 Control Register	**C8H** [1]	00H
	T2MOD	Timer 2 Mode Register	C9H	00H
	RC2H	Timer 2 Reload Capture Reg., High Byte	CBH	00H
	RC2L	Timer 2 Reload Capture Reg., Low Byte	CAH	00H
	TH2	Timer 2, High Byte	CDH	00H
	TL2	Timer 2, Low Byte	CCH	00H
Pow. Sav. Modes	PCON	Power Control Register	87H	0XXX0000B [2]

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks
3) X means that the value is indeterminate and the location is reserved

Table 3
Contents of SFRs, SFRs in Numeric Order

Address	Register	Bit 7	6	5	4	3	2	1	0
80_H	P0								
81_H	SP								
82_H	DPL								
83_H	DPH								
87_H	PCON	SMOD	–	–	–	GF1	GF0	PDE	IDLE
88_H	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89_H	TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0								
$8B_H$	TL1								
$8C_H$	TH0								
$8D_H$	TH1								
90_H	P1								
98_H	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF								
$A0_H$	P2								
$A8_H$	IE	EA	–	ET2	ES	ET1	EX1	ET0	EX0
$B0_H$	P3								
$B8_H$	IP	–	–	PT2	PS	PT1	PX1	PT0	PX0
$C8_H$	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
$C9_H$	T2MOD	–	–	–	–	–	–	–	DCEN

[Solid boxes] SFR bit and byte addressable

[Dashed boxes] SFR not bit addressable

– : = this bit location is reserved

Table 3
Contents of SFRs, SFRs in Numeric Order (cont'd)

Address	Register	Bit 7	6	5	4	3	2	1	0
CA_H	RC2L								
CB_H	RC2H								
CC_H	TL2								
CD_H	TH2								
$D0_H$	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
$E0_H$	ACC								
$F0_H$	B								

SFR bit and byte addressable

SFR not bit addressable

– : = this bit location is reserved

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **table 4**:

Table 4
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD				Input Clock	
		Gate	C/$\overline{T}$	M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	$f_{OSC}/12 \cdot 32$	$f_{OSC}/24 \cdot 32$
1	16-bit timer/counter	X	X	1	1	$f_{OSC}/12$	$f_{OSC}/24$
2	8-bit timer/counter with 8-bit autoreload	X	X	0	0	$f_{OSC}/12$	$f_{OSC}/24$
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	$f_{OSC}/12$	$f_{OSC}/24$

In the "timer" function (C/$\overline{T}$ = '0') the register is incremented every machine cycle. Therefore the count rate is $f_{OSC}/12$.

In the "counter" function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{OSC}/24$. External inputs $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 2** illustrates the input clock logic.

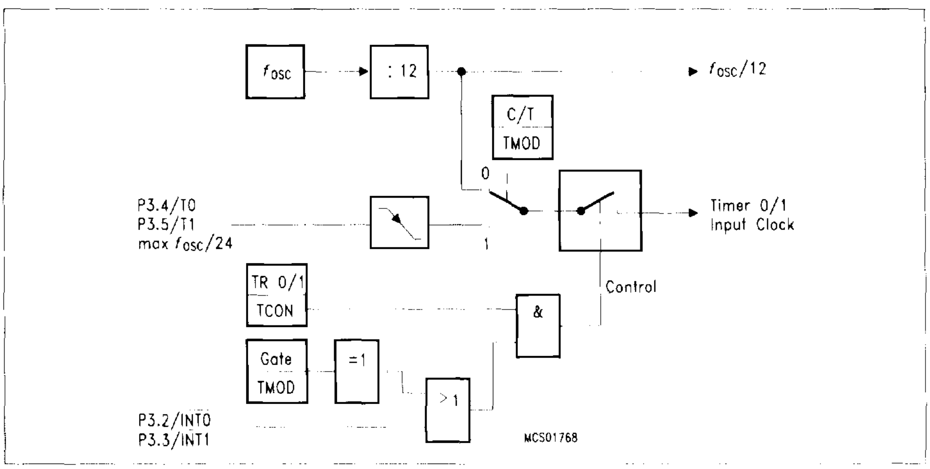


Figure 2
Timer/Counter 0 and 1 Input Clock Logic

Timer 2

Timer 2 is a 16-bit Timer/Counter with an up/down count feature. It can operate either as timer or as an event counter which is selected by bit C/$\overline{T2}$ (T2CON.1). It has three operating modes as shown in **table 5**.

Table 5
Timer/Counter 2 Operating Modes

Mode	T2CON RxCLK or TxCLK	T2CON CP/$\overline{RL2}$	T2CON TR2	T2MOD DCEN	T2CON EXEN	P1.1/ T2EX	Remarks	Input Clock internal	Input Clock external (P1.0/T2)
16-bit Auto-reload	0	0	1	0	0	X	reload upon overflow	$f_{OSC}/12$	max $f_{OSC}/24$
	0	0	1	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	Down counting		
	0	0	1	1	X	1	Up counting		
16-bit Capture	0	1	1	X	0	X	16 bit Timer/ Counter (only up-counting)	$f_{OSC}/12$	max $f_{OSC}/24$
	0	1	1	X	1	↓	capture TH2, TL2 → RC2H, RC2L		
Baud Rate Generator	1	X	1	X	0	X	no overflow interrupt request (TF2)	$f_{OSC}/2$	max $f_{OSC}/24$
	1	X	1	X	1	↓	extra external interrupt ("Timer 2")		
off	X	X	0	X	X	X	Timer 2 stops	–	–

Note: ↓ = falling edge

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **table 6**. The possible baudrates can be calculated using the formulas given in **table 7**.

Table 6
USART Operating Modes

Mode	SCON		Baudrate	Description
	SM0	SM1		
0	0	0	$f_{OSC}/12$	Serial data enters and exits through R×D. T×D outputs the shift clock. 8-bit are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate	8-bit UART 10 bits are transmitted (through T×D) or received (R×D)
2	1	0	$f_{OSC}/32$ or $f_{OSC}/64$	9-bit UART 11 bits are transmitted (T×D) or received (R×D)
3	1	1	Timer 1/2 overflow rate	9-bit UART Like mode 2 except the variable baud rate

Table 7
Formulas for Calculating Baudrates

Baud Rate derived from	Interface Mode	Baudrate
Oscillator	0 2	$f_{OSC}/12$ $(2^{SMOD} \times f_{OSC}) / 64$
Timer 1 (16-bit timer) (8-bit timer with 8-bit autoreload)	1,3 1,3	$(2^{SMOD} \times$ timer 1 overflow rate) /32 $(2^{SMOD} \times f_{OSC}) / (32 \times 12 \times (256\text{-TH1}))$
Timer 2	1,3	$f_{OSC} / (32 \times (65536\text{-(RC2H, RC2L)})$

Interrupt System

The C501 provides 6 interrupt sources with two priority levels. **Figure 3** gives a general overview of the interrupt sources and illustrates the request and control flags.

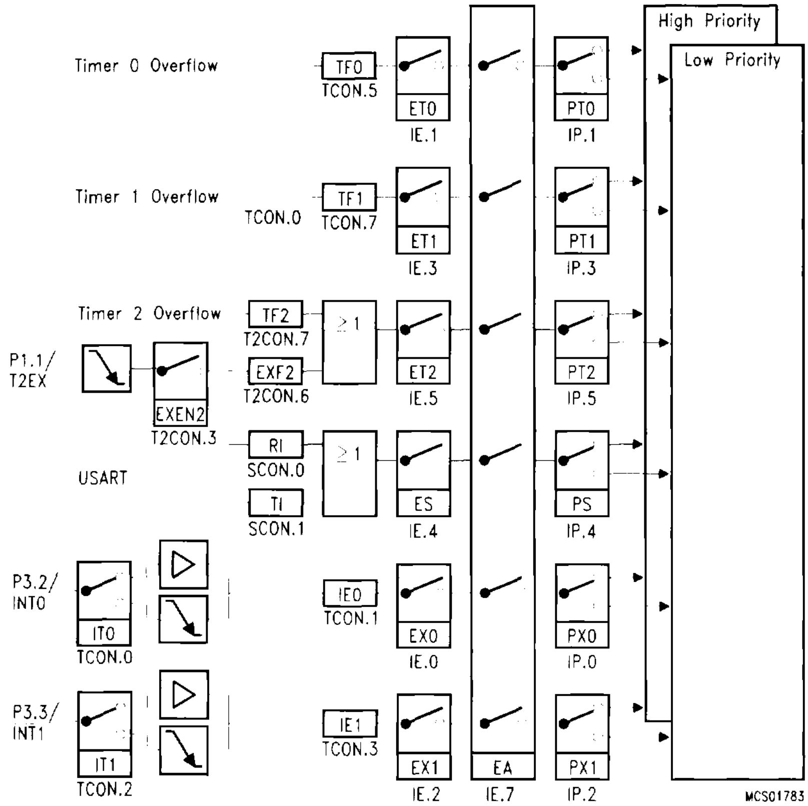


Figure 3
Interrupt Request Sources

Table 8
Interrupt Sources and their Corresponding Interrupt Vectors

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003_H
TF0	Timer 0 interrupt	$000B_H$
IE1	External interrupt 1	0013_H
TF1	Timer 1 interrupt	$001B_H$
RI + TI	Serial port interrupt	0023_H
TF2 + EXF2	Timer 2 interrupt	$002B_H$

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in **table 9**.

Table 9
Interrupt Priority-Within-Level

Interrupt Source		Priority
External Interrupt 0,	IE0	High
Timer 0 Interrupt,	TF0	
External Interrupt 1,	IE1	↓
Timer 1 Interrupt,	TF1	
Serial Channel,	RI + TI	
Timer 2 Interrupt,	TF2 + EXF2	Low

Power Saving Modes

Two power down modes are available, the Idle Mode and Power Down Mode.

The bits PDE and IDLE of the register PCON select the Power Down mode or the Idle mode, respectively. If the Power Down mode and the Idle mode are set at the same time, the Power Down mode takes precedence. **Table 10** gives a general overview of the power saving modes.

Table 10
Power Saving Modes Overview

Mode	Entering Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H	– enabled interrupt – Hardware Reset	CPU is gated off CPU status registers maintain their data. Peripherals are active
Power-Down Mode	ORL PCON, #02H	Hardware Reset	Oscillator is stopped, contents of on-chip RAM and SFR's are maintained (leaving Power Down Mode means redefinition of SFR contents).

In the Power Down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the Power Down mode is invoked, and that V_{CC} is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power Down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

Absolute Maximum Ratings

Ambient temperature under bias (T_A) .... – 40 to + 85 °C
Storage temperature (T_{ST})... – 65 to + 150 °C

Voltage on V_{CC} pins with respect to ground (V_{SS}) .... – 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS})... – 0.5 V to V_{CC} + 0.5 V

Input current on any pin during overload condition.................................... – 10 mA to + 10 mA
Absolute sum of all input currents during overload condition .... | 100 mA |

Power dissipation.. TBD

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.*

DC Characteristics
V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V; T_A = 0 °C to 70 °C for the SAB-C501
T_A = – 40 °C to 85 °C for the SAF-C501

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, RESET)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage (RESET)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except XTAL1, $\overline{EA}$, RESET)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL1	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	
Input high voltage to $\overline{EA}$, RESET	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage (ports 1, 2, 3)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 80 µA, I_{OH} = – 10 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH1}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 800 µA [2], I_{OH} = – 80 µA [2]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	– 10	– 50	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25 °C
Power supply current:					
Active mode, 12 MHz [7]	I_{CC}	–	21	mA	V_{CC} = 5 V, [4]
Idle mode, 12 MHz [7]	I_{CC}	–	4.8	mA	V_{CC} = 5 V, [5]
Active mode, 24 MHz [7]	I_{CC}	–	36.2	mA	V_{CC} = 5 V, [4]
Idle mode, 24 MHz [7]	I_{CC}	–	8.2	mA	V_{CC} = 5 V, [5]
Active mode, 40 MHz [7]	I_{CC}	–	56.5	mA	V_{CC} = 5 V, [4]
Idle mode, 40 MHz [7]	I_{CC}	–	12.7	mA	V_{CC} = 5 V, [5]
Power Down Mode	I_{PD}	–	50	µA	V_{CC} = 2 … 5.5 V [3]

[1] Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

[2] Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall bellow the 0.9 V_{CC} specification when the address lines are stabilizing.

[3] I_{PD} (Power Down Mode) is measured under following conditions:
$\overline{EA}$ = Port0 = V_{CC}; RESET = V_{SS}; XTAL2 = N.C.; XTAL1 = V_{SS}; all other pins are disconnected.

[4] I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, $V_{IL} = V_{SS}$ + 0.5 V, $V_{IH} = V_{CC}$ – 0.5 V; XTAL2 = N.C.;
$\overline{EA}$ = Port0 = RESET= V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

[5] I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, $V_{IL} = V_{SS}$ + 0.5 V, $V_{IH} = V_{CC}$ – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS}; Port0 = V_{CC}; all other pins are disconnected;

[7] $I_{CC\,max}$ at other frequencies is given by:
active mode: I_{CC} = 1.27 x f_{OSC} + 5.73
idle mode: I_{CC} = 0.28 x f_{OSC} + 1.45
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.