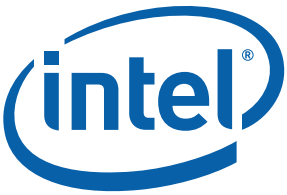

Intel®413808 and Intel®413812 SAS/SATA I/O Controllers

Datasheet

Product Features

May 2007

- The Intel® 413808 SAS/SATA I/O Controller is an 800 MHz Intel XScale® two core controller
- The Intel® 413812 SAS/SATA I/O Controller is a 1200 MHz Intel XScale® two core controller
- Two Integrated Intel XScale® processors
  - 800 MHz or 1.2 GHz
  - ARM* V5TE Compliant
  - Instruction/Data Cache: 32 KByte, 4-way Set Associative, NRU Replacement Algorithm, Lockable
  - Unified Level 2 Cache: 512 KByte Set Associative, NRU Replacement Algorithm
  - 128-Entry Branch Target Buffer
  - 8-Entry Write Buffer
  - 8-Entry Fill and Pend Buffer
- Internal Bus 400 MHz/128-bit
- Can support either PCI-X or PCI Express* as an endpoint
- Support for PCI Express* Lane Widths of x1, x2, x4, x8
- Eight Serial-Attached SCSI links — also capable of supporting direct-attached SATA targets
- Eight General Purpose I/O Pins
- Eight ACTIVITY/STATUS pairs — one per SAS port
- One I^2C Bus Interface Unit
- One UART (16550) Unit
  - 64 Byte Receive and Transmit FIFOs
  - 4 pin Master/Slave Capable
- Peripheral Bus Interface
  - 8-, 16-bit Data Bus with Two Chip Selects
  - 25 Demultiplexed Address Lines
- Interrupt Controller Unit
  - Four Priority Levels
  - Interrupt Pending Register
  - Vector Generation
  - 16 External Interrupt Pins with High Priority Interrupt (HPI#)
- Transport SRAM Memory Controller (1 MB)
- 1357-ball, Flip Chip Ball Grid Array (FCBGA), 37.5 mm x 37.5 mm and 1.0 mm ball pitch

Order Number: 315040-002US
May 2007

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Revision History

Date	Revision	Description
May 2007	002	Updated Legal page 2. Edited text in Section 2.2.2. Revise PCIXCAP description in Table 4. Updated Table 18 for Cgp, Cpcix, and Lpin values. Revised Table 17 for Tcase (Tc) maximum value to 100C. Revised Figure 24.
October 2006	001	Initial release

1.0 Introduction

1.1 About This Document

This document is a reference guide for the external architecture of the Intel®413808 and Intel®413812 SAS/SATA I/O Controllers (413808 and 413812).

1.1.1 Terminology

To aid the discussion of the 413808 and 413812 architecture, the following terminology is used:

Downstream	At or toward a PCI bus with a higher number (after configuration)
Word	16 bits of data
Dword	32 bits of data
Qword	64 bits of data
Host processor	Processor located upstream from the 413808 and 413812
Local processor	Intel XScale® processor within the 413808 and 413812
Local bus	413808 and 413812 internal bus
Upstream	At or toward a PCI bus with a lower number (after configuration)

1.1.2 Other Relevant Documents

1. Intel XScale® *Microarchitecture Developer's Manual* (Order Number 273473)—Intel Corporation
2. Intel® 413808 and 413812 I/O Controllers *Design Guide* (Order number 315055)
3. *Intel® 81348 I/O Processor Developer's Manual* (Order number 315036)
4. *PCI Local Bus Specification*, Revision 2.3—PCI Special Interest Group
5. *PCI Hot-Plug Specification,* Revision 1.0—PCI Special Interest Group
6. *PCI Bus Power Management Interface Specification*, Revision 1.1—PCI Special Interest Group
7. *PCI Express Specification*, Revision 1.0a—PCI Special Interest Group

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2.0 Features

The Intel® 413808 and 413812 SAS/SATA I/O Controllers are single or dual PCI devices that integrates the Intel XScale® processors with intelligent peripherals including a PCI bus interface and eight Serial-Attached SCSI (SAS) Engines. Intel® 413808 and 413812 SAS/SATA I/O Controllers also support two internal busses: North XSI bus and South XSI bus. With the two internal busses, transactions can take place simultaneously on each bus. The north XSI bus provides the interface to the Intel XScale® processors and the SAS Engines control registers. Peripherals that generate large burst transactions are located on the south XSI bus, thus allowing the two Intel XScale® processors exclusive access to the north XSI bus.

2.1 About Intel® 413808 and 413812 SAS/SATA I/O Controllers

The Intel® 413808 and 413812 SAS/SATA I/O Controllers consolidate, into a single system:

- Two Intel XScale® processors running at speed up to 1.2 GHz
- Eight Serial Protocol Links capable of Serial-Attached SCSI or Serial ATA operation
- Transport DMA Controllers
- Peripheral Bus Interface Unit
- Transport SRAM Memory Controller
- One I^2C Bus Interface Unit
- One Serial Port Unit
- Eight General-Purpose Input Output (GPIO) ports
- Eight ACTIVITY/STATUS pin pairs — one per SAS Engine
- Internal North Bus-South Bus Bridge

It is an integrated controller that addresses the needs of intelligent I/O storage applications and helps reduce intelligent I/O system costs.

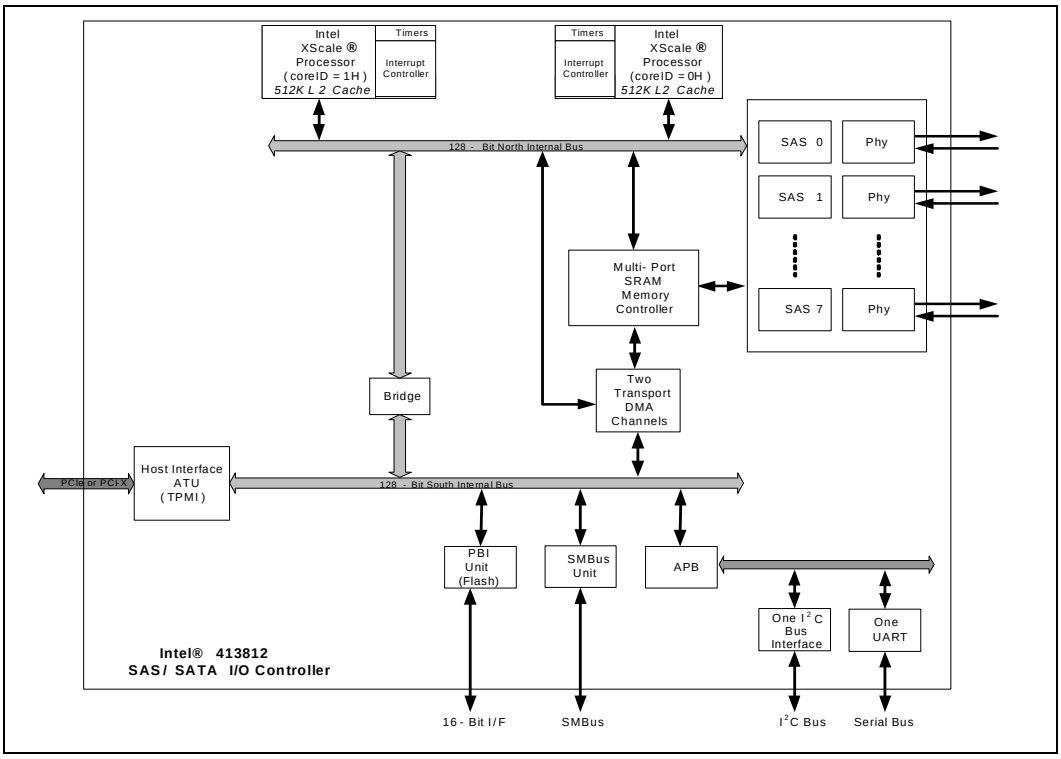
Intel® 413808 and 413812 SAS/SATA I/O Controllers can support either PCI-X 1.0b or PCI Express* as a reset option. The PCI bus is an industry-standard, high-performance, low-latency system bus. The Intel® 413808 and 413812 SAS/SATA I/O Controllers PCI bus is capable of 133 MHz operation in PCI-X 1.0b mode as defined by the *PCI-X Addendum to the Local Bus Specification,* Revision 1.0b. Also, the processor supports a 66 MHz conventional PCI mode as defined by the *PCI Local Bus Specification*, Revision 2.3. Intel® 413808 and 413812 SAS/SATA I/O Controllers supports a x8 PCI Express* interface.

The Intel® 413808 and 413812 SAS/SATA I/O Controllers can be set up as a dual-function PCI device or a single-function device at reset using an external strap. Refer to the Termination Chapter found in the Intel® 413808 and 413812 I/O Controllers *Design Guide* that describes the reset options.

Both the address and data busses on the 413808 and 413812 XSI bus are byte-wise parity protected. All the peripherals connected to the south XSI bus can check and generate parity.

Figure 1 is a block diagram of the Intel® 413808 and 413812 SAS/SATA I/O Controllers.

Figure 1. 413808 and 413812 Functional Block Diagram



2.2 413808 and 413812 Features

The subsections that follow provide a brief overview of each feature.

2.2.1 Host Interface

Intel® 413808 and 413812 SAS/SATA I/O Controllers can be set up as either a single or dual-function PCI device, and provides either a PCI-X 1.0b or PCI Express* host interface. Intel® 413808 SAS/SATA I/O Controller is a single function PCI device, and provides either a PCI-X 1.0b or PCI Express* host interface.

2.2.2 Internal Busses

The Intel® 413808 and 413812 SAS/SATA I/O Controllers are built around two internal busses: north internal bus and south internal bus. The two busses use the same bus protocol. The north internal bus is 128 bits wide and operates at 400 MHz. The north bus connects the two Intel XScale® processors, which have direct access to the SRAM. The Intel XScale® processors also have direct access to the SAS/SATA engine memory-mapped registers.

The south internal bus is 128 bits wide and operates at 400 MHz. The south XSI bus provides the data paths for burst transactions generated by the DMAs. The south and north XSI bus internal address and data busses are parity-protected on a byte-wise basis. Agents on the south XSI bus can generate and check address and data parity. The point-to-point interfaces between the agents and SRAM Memory Controllers are also parity-protected on a byte-wise basis.

2.2.3 Third-Party Messaging Interface (TPMI)

The Third-Party Messaging Interface (TPMI) provides messaging interface between the PCI system and the controllers. The TPMI uses interrupts to notify each system when new data arrives. The TPMI has three messaging mechanisms: Mailbox Registers, Doorbell Registers, and Circular Queues. Each allows a host processor or external PCI device and the Intel® 413808 and 413812 SAS/SATA I/O Controllers to communicate through message-passing and interrupt generation.

2.2.4 Peripheral Bus Interface

The Peripheral Bus Interface Unit is a data communication path to the flash memory components or other peripherals of a Intel® 413808 and 413812 SAS/SATA I/O Controllers hardware system. The PBI includes support for either 8- or 16-bit devices. To perform these tasks at high bandwidth, the bus features a burst-transfer capability which allows successive 8/16-bit data transfers.

2.2.5 I²C Bus Interface Unit

There is one I²C (Inter-Integrated Circuit) Bus Interface Unit that allow the Intel XScale® processor to serve as a master and slave device residing on the I²C bus. The I²C unit uses a serial bus developed by Philips Semiconductor consisting of a two-pin interface. The bus allows the Intel® 413808 and 413812 SAS/SATA I/O Controllers to interface to a SEP device. For more information, refer to *I²C Peripherals for Microcontrollers* (Philips Semiconductor)[1].

2.2.6 UART Unit

The Intel® 413808 and 413812 SAS/SATA I/O Controllers includes a UART unit. The UART allows the core to serve as a master and slave device residing on the UART bus. The UART uses a serial bus consisting of a two-pin interface. Also refer to the National Semiconductor* 16550 device specification[2].

Note: This UART is dedicated for transport firmware debug only.

2.2.7 Interrupt Controller Unit

Each Intel XScale® processor supports an Interrupt Controller Unit (ICU). The ICU aggregates interrupt sources both external and internal of sources of Intel® 413808 and 413812 SAS/SATA I/O Controllers to the Intel XScale® processor. The ICU supports high-performance interrupt processing with direct interrupt service routine vector generation on a per-source basis. Each source has programmability for masking, core processor interrupt input, and priority.

2.2.8 XSI System Controller

Each XSI bus (north and south) employs an XSI system controller. The XSI system controller observes all the address or data bus requests from requestors and completors connected to the XSI bus. The XSI system controller handles XSI address

1. http://www.semiconductors.philips.com/buses/i2c/
2. http://www.national.com/pf/PC/PC16550D.html

bus arbitration, XSI data bus arbitration, framing Address bus cycles, and framing Data bus cycles. The XSI system controller provides the shared address and shared data paths from/to units.

2.2.9 GPIO

The Intel® 413808 and 413812 SAS/SATA I/O Controllers include eight General-Purpose I/O (GPIO) pins, and eight ACTIVITY/STATUS pin pairs. Each SAS engine uses one ACTIVITY/STATUS pin pair for Link Status and Link Activity indicators.

3.0 Package Information

3.1 Package Introduction

The Intel® 413808 and Intel® 413812 SAS/SATA I/O Controllers are offered in a 1357-ball FCBGA5 package.

3.2 Functional Signal Definitions

This section defines the pins and signals.

3.2.1 Signal Pin Descriptions

Table 1. Pin Description Nomenclature

Symbol	Description
I	Input pin only
O	Output pin only
I/O	Pin can be either an input or an output
OD	Open-drain pin
PWR	Power pin
GND	Ground pin
—	Pin must be connected as described
Sync(...)	Synchronous. Signal meets timings relative to a clock. • Sync(P): Synchronous to **P_CLKIN** • Sync(T): Synchronous to **TCK**
Async	Asynchronous. Inputs can be asynchronous relative to all clocks. All asynchronous signals are level-sensitive.
R/W	Indicates read or write capability.
Rst(P)	The pin is reset with **WARM_RST#** or **P_RST#**.
Rst(PB)	The pin is reset with **PB_RSTOUT#**. **PB_RSTOUT#** is asserted when the Peripheral Bus Interface subsystem is reset.
Rst(T)	The pin is reset with **TRST#**.
ActLow	The pin is an active-low signal.
Diff	The pin is a differential signal pair. • "P" at the end of a differential pin name indicates "positive". • "N" at the end of a differential pin name indicates "negative".

Table 2. Peripheral Bus Interface Signals

Name	Count	Type	Description
A[24:0]	25	O Rst(PB)	Peripheral Address Bus: carries the address bits for the current access. The PBI interface can address up to 32 MBytes.
D[15:0]	16	I/O Rst(PB)	Peripheral Data Bus: carries read or write data to and from memory. During write operations to 8-bit wide memory regions, the PBI drives unused bus pins to determinate values.
POE#	1	O Rst(PB) ActLow	Peripheral Output Enable: indicates whether bus access is write or read with respect to I/O processor and is valid during entire bus access. This pin can be used to control output enable on a peripheral device. 0 = Read 1 = Write
PWE#	1	O Rst(PB) ActLow	Peripheral Write Enable: indicates to the peripheral device whether or not to write data to the addressed space. This pin can be used to control the write enable on the peripheral device. 0 = Write 1 = Read
PCE[1:0]#	2	O Rst(PB) ActLow	Peripheral Chip Enable: Specifies which of the two memory address ranges are associated with the current bus access. The pin remains valid during the entire bus access. ***Note:*** These pins must be pulled up to V_{CC3P3} with external 8.2K ohm 5%, 1/16W resistors for proper operation.
PB_RSTOUT#	1	O ActLow	Peripheral Bus Reset Out: can be used to reset the peripheral device. It has the same timing as the internal bus reset.
Total	46		

Table 3. Compact PCI Hot Swap Signals

Name	Count	Type	Description
HS_ENUM#	1	OD Rst(P) ActLow	Hot Swap Event: Conditionally asserted to notify system host that either a board has been freshly inserted or is about to be extracted. This signal informs the system host that the configuration of the system has changed. The system host then performs any necessary maintenance such as installing or quiesing a device driver.
HS_LSTAT	1	I Rst(P)	Hot Swap Latch Status: Input indicating state of the ejector switch. 0 = Indicates the ejector switch is closed. 1 = Indicates the ejector switch is open. If Compact PCI Hot Swap not supported, tie this signal low.
HS_LED_OUT	1	O Rst(P)	Hot Swap LED Output: outputs a logic one to illuminate the Hot Swap blue LED.
HS_FREQ[1:0]	2	I/O Rst(P)	Hot Swap Frequency: In Hot Swap mode, these pins are inputs, determining the bus frequency and mode during a PCI-X hot swap event. These are valid only when **PCIX_EP#** = 0 and **HS_SM#** = 0. 00 = 133 MHz PCI-X 01 = 100 MHz PCI-X 10 = 66 MHz PCI-X 11 = 33 or 66 MHz. PCI (frequency depends on **P_M66EN**) • These pins have internal pull-ups.
Total	5		

Table 4. PCI Bus Signals (Sheet 1 of 3)

Name	Count	Type	Description
P_AD[63:32]	32	I/O Sync(P) Rst(P)	PCI Address/Data: is the upper 32 bits of the PCI data bus driven during the data phase.
P_AD[31:0]	32	I/O Sync(P) Rst(P)	PCI Address/Data: is the multiplexed PCI address and lower 32 bits of the data bus.
P_CBE[7]#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_CBE[6]#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_CBE[5]#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_CBE[4]#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_CBE[3]#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_CBE[2]#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_CBE[1]#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_CBE[0]#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_PAR64	1	I/O Sync(P) Rst(P)	PCI Bus Upper DWORD Parity is even parity across **P_AD[63:32]** and P_CBE_N[7:4].
P_REQ64#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Request 64-Bit Transfer indicates the attempt of a 64-bit transaction on the PCI bus. When the target is 64-bit capable, the target acknowledges the attempt with the assertion of P_ACK64_N.
P_ACK64#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Acknowledge 64-Bit Transfer indicates that the device has positively decoded its address as the target of the current access and the target is willing to transfer data using the full 64-bit data bus.
P_PAR	1	I/O Sync(P) Rst(P)	PCI Bus Parity is even parity across **P_AD[31:0]** and P_CBE_N[3:0].
P_FRAME#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Cycle Frame is asserted to indicate the beginning and duration of an access.

Table 4. PCI Bus Signals (Sheet 2 of 3)

Name	Count	Type	Description
P_IRDY#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Initiator Ready indicates the initiating agent's ability to complete the current data phase of the transaction. During a write, it indicates that valid data is present on the address/data bus. During a read, it indicates that the processor is ready to accept the data.
P_TRDY#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Target Ready indicates the target agent's ability to complete the current data phase of the transaction. During a read, it indicates that valid data is present on the address/data bus. During a write, it indicates that the target is ready to accept the data.
P_STOP#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Stop indicates a request to stop the current transaction on the PCI bus.
P_DEVSEL#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Device Select is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected.
P_SERR#	1	I/O OD Sync(P) Rst(P) ActLow	PCI Bus System Error is driven for address parity errors on the PCI bus.
P_RSTOUT#	1	O Async ActLow	PCI Reset Out is based on **P_RST#** and **WARM_RST#**. It brings PCI-specific registers, sequencers, and signals to a consistent state. When either **P_RST#** or **WARM_RST#** is asserted, it causes **P_RSTOUT#** to assert and: • PCI output signals are driven to a known consistent state. • PCI bus interface output signals are three-stated. • Open-drain signals such as P_SERR_N are floated. **P_RSTOUT#** can be asynchronous to P_CLK when asserted or deasserted.
P_PERR#	1	I/O Sync(P) Rst(P) ActLow	PCI Bus Parity Error is asserted when a data parity error occurs during a PCI bus transaction.
P_M66EN	1	I	PCI Bus 66 MHz Enable indicates the speed of the PCI bus. When this signal is sampled high, the PCI bus speed is 66 MHz; when low, the bus speed is 33 MHz.
P_IDSEL	1	I Sync(P)	PCI Bus Initialization Device Select is used to select the Intel® 413808 and Intel® 413812 SAS/SATA I/O Controllers during a configuration read or write.
P_REQ#	1	O Sync(P) ActLow	PCI Bus Request: • External arbiter mode: This is the output request signal for the ATU.
P_GNT#	1	I Sync(P) Rst(P) ActLow	PCI Bus Grant: • External arbiter mode: This is the input grant signal to the ATU.
P_PCIXCAP	1	I	PCI-X Capability: Refer to the Intel® 413808 and Intel® 413812 SAS/SATA I/O Controllers *Specification Update* for more details.

Table 4. PCI Bus Signals (Sheet 3 of 3)

Name	Count	Type	Description
P_BMI	1	O Sync(P) Rst(P)	PCI Bus Master Indicator indicates that the I/O processor is mastering a transaction on the PCI bus.
P_CAL[0]	1	O	PCI Calibration is connected to an external calibration resistor. The V_{CCVIO} PCI output drivers reference the resistor to dynamically adjust the drive strength to compensate for voltage and temperature variations. This pin is connected through a 22.1 ohm 1% resistor to ground.
P_CAL[1]	1	O	PCI Calibration is connected to an external calibration resistor. The PCI output drivers reference the resistor to dynamically adjust the ODT resistance to compensate for voltage and temperature variations. This pin is connected through a 121 ohm 1% resistor to ground.
P_CAL[2]	1	O	PCI Calibration is connected to an external calibration resistor. The V_{CC3P3} PCI output drivers reference the resistor to dynamically adjust the drive strength to compensate for voltage and temperature variations. This pin is connected through a 22.1 ohm 1% resistor to ground.
P_CLKIN	1	I	PCI Bus Input Clock provides the AC timing reference for all PCI transactions.
Total	94		

Table 5. PCI Express* Signals

Name	Count	Type	Description
REFCLKP, **REFCLKN**	2	I Diff	PCI Express* Clock is the 100 MHz differential input reference clock for the PCI Express* interface.
PETP[7:0], **PETN[7:0]**	16	O Diff	PCI Express* Transmit carries the differential output serial data and embedded clock for the PCI Express* interface.
PERP[7:0], **PERN[7:0]**	16	I Diff	PCI Express* Receive carries the differential input serial data and embedded clock for the PCI Express* interface.
PE_CALP, **PE_CALN**	2	I/O	PCI Express* Calibration pins are connected to an external calibration resistor. The PCI Express* output drivers can reference the resistor to dynamically adjust their slew rate and drive strength to compensate for voltage and temperature variations. A 1.4K ohm 1% resistor is connected between these two pins.
Total	36		

Table 6. Storage Interface Signals (Sheet 1 of 3)

Name	Count	Type	Description
S_CLKN0, **S_CLKP0**	2	I Diff	Storage Clock is the 150 MHz or 125 MHz ±100 ppm differential input reference clock for the SAS/SATA interface. ***Note:*** Should be AC coupled with a 100nF capacitor.
S_TXP[7:0], **S_TXN[7:0]**	16	O Diff	Storage Transmit carries the differential output serial data and embedded clock for the SAS/SATA interface. ***Note:*** Should be AC coupled with a 10nF capacitor.
S_RXP[7:0], **S_RXN[7:0]**	16	I Diff	Storage Receive carries the differential input serial data and embedded clock for the SAS/SATA interface. ***Note:*** Should be AC coupled with a 10nF capacitor.
RBIAS[1:0]	2	O	Resistor Bias: A 6.49K ohm 1% 1/8W external resistor must be connected between this pin and ground for proper operation. This resistor generates internal bias currents.
RBIAS_SENSE[1:0]	2	I/O	Resistor Bias Sense is used internally to sense ground. This ball must be connected to the same physical ground point as the **RBIAS[1:0]** resistor is connected to on the PCB.
S_ACT0 / **SCLOCK0**	1	OD	Storage Activity: When SGPIO[0] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[0]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC. Serial Clock: (default) When SGPIO[0] is enabled, this pin is the serial output clock running at 99.8 KHz. The falling edge of **SCLOCK0** is used to latch **SLOAD0**, **SDATAOUT0**, and **SDATAIN0**.
S_STAT0 / **SLOAD0**	1	OD	Storage Status: When SGPIO[0] is disabled this pin can be used to drive an LED to indicate status of the link for storage engine[0]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC. Serial Load: (default) When SGPIO[0] is enabled, this pin is the serial load clock. It is driven high to indicate the start of the bit stream.
S_ACT1	1	OD	Storage Activity: When SGPIO[0] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[1]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC.
S_STAT1	1	OD	Storage Status: When SGPIO[0] is disabled, this pin can be used to drive an LED to indicate status of the link for storage engine[1]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC.
S_ACT2 / **SDATAIN0**	1	OD	Storage Activity: When SGPIO[0] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[2]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC. Serial Data In: (default) When SGPIO[0] is enabled, this pin is the serial input data. There are three bits of data per device and up to eight devices are supported.
S_STAT2 / **SDATAOUT0**	1	OD	Storage Status: When SGPIO[0] is disabled, this pin can be used to drive an LED to indicate status of the link for storage engine[2]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC. Serial Data Out: (default) When SGPIO[0] is enabled, this pin is the serial output data. There are three bits of data per device and up to eight devices are supported.

Table 6. Storage Interface Signals (Sheet 2 of 3)

Name	Count	Type	Description
S_ACT3	1	OD	Storage Activity: When SGPIO[0] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[3]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC.
S_STAT3	1	OD	Storage Status: When SGPIO[0] is disabled, this pin can be used to drive an LED to indicate status of the link for storage engine[3]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC.
S_ACT4 / SCLOCK1	1	OD	Storage Activity: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[4]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC. Serial Clock: (default) When SGPIO[1] is enabled this pin is the serial output clock running at 99.8 KHz. The falling edge of **SCLOCK1** is used to latch **SLOAD1**, **SDATAOUT1** and **SDATAIN1**.
S_STAT4 / SLOAD1	1	OD	Storage Status: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate status of the link for storage engine[4]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC. Serial Load: (default) When SGPIO[1] is enabled, this pin is the serial load clock. It is driven high to indicate the start of the bit stream.
S_ACT5	1	OD	Storage Activity: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[5]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC.
S_STAT5	1	OD	Storage Status: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate status of the link for storage engine[5]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC.
S_ACT6 / SDATAIN1	1	OD	Storage Activity: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[6]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC. Serial Data In: (default) When SGPIO[1] is enabled, this pin is the serial input data. There are three bits of data per device and up to eight devices are supported.
S_STAT6 / SDATAOUT1	1	OD	Storage Status: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate status of the link for storage engine[6]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC. Serial Data Out: (default) When SGPIO[1] is enabled, this pin is the serial output data. There are three bits of data per device and up to eight devices are supported.

Table 6. Storage Interface Signals (Sheet 3 of 3)

Name	Count	Type	Description
S_ACT7	1	OD	Storage Activity: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[7]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC.
S_STAT7	1	OD	Storage Status: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate status of the link for storage engine[7]. The pin can be direct driven by the storage engine or driven from an SGPIO. ***Note:*** Connect the LED to a series resistor pulled up to VCC.
Total	54		

Table 7. Interrupt Signals

Name	Count	Type	Description
P_INT[D:A]# / XINT[3:0]# / GPIO[11:8]	4	OD I I/O Async Rst(P) ActLow	PCI Interrupt requests an interrupt from the central resource. The assertion and deassertion is asynchronous. A device asserts its **XINT[3:0]# / P_INT[D:A]#** line when requesting attention from its device driver. As soon as the **XINT[3:0]# / P_INT[D:A]#** signal is asserted, it remains asserted until the device driver clears the pending request. ***Note:*** General Purpose I/O pins **GPIO[11:8]** not supported on Intel® 413808 and Intel® 413812 SAS/SATA I/O Controllers.
XINT[7:4]# / GPIO[15:12]	4	I I/O Async ActLow	External Interrupt Requests are used by external devices to request interrupt service. These pins are level-detect and are internally synchronized. These pins go to the **XINT[7:4]#** inputs of the interrupt controller. The interrupt controller can steer the interrupt to either the FIQ or the IRQ internal interrupt input of the Intel XScale® processor. ***Note:*** General Purpose I/O pins **GPIO[11:8]** not supported on Intel® 413808 and Intel® 413812 SAS/SATA I/O Controllers.
GPIO[7:0] / XINT[15:8]#	8	I/O I O Async Rst(p)	General Purpose I/O pins can be selected on a per-pin basis as general-purpose inputs or outputs. The default mode is a general-purpose input. External Interrupts are used by external devices to request interrupt service. These pins are level-detect and are internally synchronized. These pins go to the **XINT[15:8]#** inputs of the interrupt controller. These interrupts are dedicated to the Intel XScale® processor. To enable a given pin as an interrupt, it needs to be unmasked in the INTCTL[3:0] register.
HPI#	1	I Async ActLow	High-Priority Interrupt causes a high-priority interrupt to the I/O processor. This pin is level-detect only and is internally synchronized.
NMI0#	1	I Async ActLow	Non-Maskable Interrupt causes a non-maskable data abort to the Intel XScale® processor 0 in the I/O processor. This pin is falling edge-detect only and is internally synchronized.
NMI1#	1	I Async ActLow	Non-Maskable Interrupt causes a non-maskable data abort to the Intel XScale® processor 1 in the I/O processor. This pin is falling edge-detect only and is internally synchronized. ***Note:*** Pin not valid on Intel® 413808 I/O Controller
Total	19		

Table 8. I²C and SM Bus Signals

Name	Count	Type	Description
SCL0	1	I/O OD	I²C 0 Clock provides synchronous operation of the I²C bus.
SDA0	1	I/O OD	I²C 0 Data is used for data transfer and arbitration of the I²C bus.
SCL1	1	I/O OD	I²C 1 Clock provides synchronous operation of the I²C bus. ***Note:*** I²C 1 is not supported and this pin must be tied low.
SDA1	1	I/O OD	I²C 1 Data is used for data transfer and arbitration of the I²C bus. ***Note:*** I²C 1 is not supported and this pin must be tied low.
SCL2	1	I/O OD	I²C 2 Clock provides synchronous operation of the I²C bus. ***Note:*** I²C 2 is not supported and this pin must be tied low.
SDA2	1	I/O OD	I²C 2 Data is used for data transfer and arbitration of the I²C bus. ***Note:*** I²C 2 is not supported and this pin must be tied low.
SMBCLK	1	I/O OD	SM Bus Clock provides synchronous operation of the SM bus.
SMBDAT	1	I/O OD	SM Bus Data is used for data transfer and arbitration of the bus.
Total	8		

Note: Open drain outputs require an external pull-up resistor to pull up the signal to 3.3 V. The value of the pull-up resistor depends on the bus loading.

Table 9. UART Signals (Sheet 1 of 2)

Name	Count	Type	Description
U0_RXD	1	I Async	UART 0 Serial Input: Serial data input from device pin to the receive shift register.
U0_TXD	1	O Async	UART 0 Serial Output: Composite serial data output to the communications link-peripheral, modem, or data set. The TXD signal is set to the MARKING (logic 1) state upon a reset operation.
U0_CTS#	1	I ActLow Async	UART 0 Clear to Send: When low, this pin indicates that the receiving UART is ready to receive data. When the receiving UART deasserts CTS# high, the transmitting UART must stop transmission to prevent overflow of the receiving UART buffer. The CTS# signal is a modem-status input whose condition can be tested by the host processor or by the UART when in Autoflow Mode as described below: • Non-Autoflow Mode: When not in Autoflow Mode, bit[4] (CTS) of the Modem Status Register (MSR) indicates the state of CTS#. Bit[4] is the complement of the CTS# signal. Bit[0] (DCTS) of the Modem Status Register indicates whether the CTS# input has changed state since the previous reading of the Modem Status Register. CTS# has no effect on the transmitter. The user can program the UART to interrupt the processor when DCTS changes state. The programmer can then stall the outgoing data stream by starving the transmit FIFO or disabling the UART with the IER register. ***Note:*** When UART transmission is stalled by disabling the UART, the user does not receive an MSR interrupt when CTS# reasserts. This is because disabling the UART also disables interrupts. To work around this, the user can use Auto CTS in Autoflow Mode, or program the CTS# pin to interrupt. • Autoflow Mode: In Autoflow Mode, the UART transmit circuity checks the state of CTS# before transmitting each byte. When CTS# is high, no data is transmitted.
U0_RTS#	1	O ActLow Async	UART 0 Request to Send: This bit indicates to the remote device whether the UART is ready to receive data. When this bit is low, the UART is ready to receive data. A reset operation sets this signal to its inactive (high) state. LOOP Mode operation holds this signal in its inactive state. • Non-Autoflow Mode: The RTS# output signal can be asserted by setting bit[1] (RTS) of the Modem Control Register to 1. The RTS bit is the complement of the RTS# signal. • Autoflow Mode: RTS# is automatically asserted by the autoflow circuitry when the receive buffer exceeds its programmed threshold. It is deasserted when enough bytes are removed from the buffer to lower the data level back to the threshold.
U1_RXD	1	I Async	UART 1 Serial Input: Serial data input from the device pin to the receive shift register. **NOTE:** UART 1 is not supported and this pin must be tied low.

Table 9. UART Signals (Sheet 2 of 2)

Name	Count	Type	Description
U1_TXD	1	O Async	UART 1 Serial Output: Composite serial data output to the communications link-peripheral, modem, or data set. The TXD signal is set to the MARKING (logic 1) state upon a reset operation. **NOTE:** UART 1 is not supported and this pin must be unconnected.
U1_CTS#	1	I ActLow Async	UART 1 Clear to Send: When low, this pin indicates that the receiving UART is ready to receive data. When the receiving UART deasserts CTS# high, the transmitting UART must stop transmission to prevent overflow of the receiving UART buffer. The CTS# signal is a modem-status input whose condition can be tested by the host processor or by the UART when in Autoflow Mode as described below: Non-Autoflow Mode: When not in Autoflow Mode, bit[4] (CTS) of the Modem Status Register (MSR) indicates the state of CTS#. Bit[4] is the complement of the CTS# signal. Bit[0] (DCTS) of the Modem Status Register indicates whether the CTS# input has changed state since the previous reading of the Modem Status Register. CTS# has no effect on the transmitter. The user can program the UART to interrupt the processor when DCTS changes state. The programmer can then stall the outgoing datastream by starving the transmit FIFO or disabling the UART with the IER register. **NOTE:** When UART transmission is stalled by disabling the UART, the user does not receive an MSR interrupt when CTS# reasserts. This is because disabling the UART also disables interrupts. To get around this, the user can use Auto CTS in Autoflow Mode, or program the CTS# pin to interrupt. Autoflow Mode: **NOTE:** In Autoflow Mode, the UART transmit circuity checks the state of CTS# before transmitting each byte. When CTS# is high, no data is transmitted. **NOTE:** UART 1 is not supported and this pin must be tied low.
U1_RTS#	1	O ActLow Async	UART 1 Request to Send: This bit indicates to the remote device whether the UART is ready to receive data. When low, the UART is ready to receive data. A reset operation sets this signal to its inactive (high) state. LOOP Mode operation holds this signal in its inactive state. Non-Autoflow Mode: The RTS# output signal can be asserted by setting bit[1] (RTS) of the Modem Control Register to 1. The RTS bit is the complement of the RTS# signal. Autoflow Mode: RTS# is automatically asserted by the autoflow circuitry when the receive buffer exceeds its programmed threshold. It is deasserted when enough bytes are removed from the buffer to lower the data level back to the threshold. **NOTE:** UART 1 is not supported and this pin must be unconnected.
Total	8		

Table 10. Miscellaneous Signals

Name	Count	Type	Description
TCK	1	I	Test Clock provides clock input for IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the device on the rising clock edge, and data is clocked out on the falling clock edge.
TDI	1	I Sync(T)	Test Data Input is the JTAG serial input pin. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR states of the Test Access Port. This signal has a weak internal pull-up to ensure proper operation when this pin is not being driven.
TDO	1	O Sync(T) Rst(T)	Test Data Output is the serial output pin for the JTAG feature. TDO is driven on the falling edge of **TCK** during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, **TDO** floats. The behavior of **TDO** is independent of other resets.
TRST#	1	I Async ActLow	Test Reset asynchronously resets the Test Access Port controller function of IEEE 1149 Boundary Scan Testing (JTAG). This pin has a weak internal pull-up. ***Note:*** This pin must be tied low when not used.
TMS	1	I Sync(T)	Test Mode Select is sampled on the rising edge of **TCK** to select the operation of the test logic for IEEE 1149 Boundary Scan testing. This pin has a weak internal pull-up.
NC	199	I/O	No Connect: Pins have no usable function and must not be connected to any signal, power, or ground.
P_RST#	1	I Async ActLow	Cold Reset is used to asynchronously reset the I/O processor when it is low. This signal must be asserted whenever the power supplies are outside of the specified ranges. • Registers are reset to default values. • Pins are driven to known states. • Sticky configuration bits are reset.
WARM_RST#	1	I Async ActLow	Warm Reset is the same as a cold reset, except sticky configuration bits are not reset. This pin should only be used when the sticky bit functionality is required. In this scenario, the WARM_RST# pin must be tied to the system reset PCI_RST# signal while the P_RST# pin can be tied to the system power good signal. If the sticky bit functionality is not required, the WARM_RST# pin should not be used and must be tied to Vcc. When the PCI Express interface is used as an endpoint, the PCI Express inband Hot Reset Mechanism can also be used to provide the sticky bit functionality. ***Note:*** Driving WARM_RST# using any other methods than suggested above may result in unpredictable behavior of the device.
THERMDA	1	I	Thermal Diode Anode is the anode of the thermal diode.
THERMDC	1	O	Thermal Diode Cathode is the cathode of the thermal diode.
PUR1	1	I	Pull-Up Required 1: This pin must be pulled up to $\mathbf{V_{CC3P3}}$ with an external 8.2K ohm 5%, 1/16W resistor for proper operation.
Total	209		

Table 11. Power and Ground Signals

Name	Count	Type	Description
$V_{CC1P2PLLS0}$	1	PWR	V_{CC} PLL Storage: Ball connected to a 1.2 V filtered board supply. Provides power to one of two PLLs that control Storage interface.
$V_{CC1P2PLLS1}$	1	PWR	V_{CC} PLL Storage: Ball connected to a 1.2 V filtered board supply. Provides power to one of two PLLs that control Storage interface.
$V_{CC1P2PLLP}$	1	PWR	V_{CC} PLL PCI-X: Ball connected to a 1.2 V filtered board supply. Provides power to PLL that controls the PCI-X logic and interface.
$V_{CC1P2PLLD}$	1	PWR	V_{CC} PLL Digital: Ball connected to a 1.2 V filtered board supply. Provides power to the PLL that controls the processor digital logic.
$V_{CC3P3PLLX}$	1	PWR	V_{CC} PLL X: Ball to be connected to a 3.3 V filtered board supply. This pin provides power to a voltage regulator, which supplies power to the PLL that controls the Intel XScale® processor and XSI processor logic.
VSSPLLS0	1	GND	V_{SS} PLL Storage: Ball to be connected to a board ground plane at the location of the $V_{CC1P2PLLS0}$ filter.
VSSPLLS1	1	GND	V_{SS} PLL Storage: Ball to be connected to a board ground plane at the location of the $V_{CC1P2PLLS1}$ filter.
VSSPLLP	1	GND	V_{SS} PLL PCI-X: Ball connected to capacitor of the $V_{CC1P2PLLP}$ filter.
VSSPLLD	1	GND	V_{SS} PLLDigital: Ball connected to capacitor of $V_{CC1P2PLLD}$ filter.
VSSPLLX	1	GND	V_{SS} PLL X: Ball connected to capacitor of $V_{CC3P3PLLX}$ filter.
V_{CC1P2}	187	PWR	1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the processor logic.
$V_{CC1P2AE}$	8	PWR	1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the PCI Express* analog logic.
V_{CC1P2E}	6	PWR	1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the PCI Express* digital logic.
$V_{CC1P2DS}$	6	PWR	1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the storage interface digital logic.
$V_{CC1P2AS}$	9	PWR	1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the storage interface analog logic.
V_{CC1P2X}	119	PWR	1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the Intel XScale® processors.
V_{CCVIO}	21	PWR	VIO Power: Balls to be connected to a 3.3 V board power plane. These pins provide 3.3 V power to the PCI-X I/Os.
V_{CC1P8}	30	PWR	1.8 V Power: Balls to be connected to a 1.8 V board power plane. These pins provide power to the I/Os.
V_{CC1P8E}	14	PWR	1.8 V Power: Balls to be connected to a 1.8 V board power plane. These pins provide power to the PCI Express* interface I/Os.
V_{CC1P8S}	6	PWR	1.8 V Power: Balls to be connected to a 1.8 V board power plane. These pins provide power to the storage interface I/Os.
V_{CC3P3}	42	PWR	3.3 V Power: Balls to be connected to a 3.3 V board power plane. These pins provide power to the PBI, miscellaneous pins, and PCI-X I/Os in Mode 1.
V_{SS}	374	GND	Ground: Balls to be connected to a board ground plane.
V_{SSE}	20	GND	PCI Express* Ground: Balls connected to a board ground plane.
V_{SSAS}	20	GND	Analog Storage Ground: Balls connected to a board ground plane.
V_{SSDS}	6	GND	Digital Storage Ground: Balls connected to a board ground plane.
Total	879		

Table 12. Reset Strap Signals (Sheet 1 of 2)

Name	Count	Type	Description
BOOT_WIDTH_8#	1	Reset Strap	PBI Boot Bus Width: Sets the default bus width for the PBI Memory Boot window. 0 = 8 bits wide 1 = 16 bits wide (default mode) ***Note:*** Muxed onto signal **A[0]**.
DF_SEL[2:0]	3	Reset Strap	Device Function Select: These straps select the number of storage ports assigned to each function within Intel® 413808 and Intel® 413812 SAS/SATA I/O Controllers. ***Note:*** DF_SEL[2] muxed onto signal A[9] DF_SEL[1] muxed onto signal A[8] DF_SEL[0] muxed onto signal A[7] 0 = 4.7K ohms resistor pull down. 1 = Internal pull up. See Section 23.4, "Device Function Select", of the Developer's Manual for additional details.
CFG_CYCLE_EN#	1	Reset Strap	Configuration Cycle Enable: Determines whether PCI interface retries configuration cycles until Host Lockout Bit is cleared. 0 = Configuration cycles enabled 1 = Configuration retry enabled (default mode) • PCI-X Interface: Configuration cycles are claimed and terminated with a retry status. • PCI Express* Interface: Configuration requests result in a completion TLP with Configuration Retry Status (CRS). ***Note:*** Muxed onto signal **A[1]**
HOLD_X0_IN_RST#	1	Reset Strap	Hold Intel XScale® Microprocessor 0 in Reset: Determines whether the Intel XScale® microprocessor number 0 is held in reset until the reset bit is cleared in the PCI Configuration and Status Register. 0 = Hold in reset 1 = Do not hold in reset (default mode) ***Note:*** Muxed onto signal **A[2]**
HOLD_X1_IN_RST#	1	Reset Strap	Hold Intel XScale® Microprocessor 1 in Reset: Determines whether the Intel XScale® microprocessor number 1 is held in reset until the reset bit is cleared in the PCI Configuration and Status Register. 0 = Hold in reset 1 = Do not hold in reset (default mode) ***Note:*** Muxed onto signal **A[3]** ***Note:*** Pin not valid on Intel® 413808 I/O Controller
EXT_ARB#	1	Reset Strap	External Arbiter: Determines whether the PCI interface enables the integrated arbiter, or use an external arbiter. 0 = External arbiter 1 = Internal arbiter (default mode) ***Note:*** Internal Arbiter is not supported. This pin must be pulled low. ***Note:*** Muxed onto signal **A[6]**
INTERFACE_SEL_PCIX#	1	Reset Strap	***Note:*** Muxed onto signal **A[10]**
PCIX_EP#	1	Reset Strap	PCI-X End Point: Determines whether the PCI-X interface operates as an endpoint or a central resource. 0 = Endpoint 1 = Central resource (default mode) ***Note:*** Central resource mode is not supported. This pin must be pulled down to V_{SS} with an external 4.7K ohm 5%, $^1/_{16}$W resistor for proper operation. ***Note:*** Muxed onto signal **A[11]** ***Note:*** Setting both **PCIX_EP#** and PCIE_RC# to endpoint is unsupported.

Table 12. Reset Strap Signals (Sheet 2 of 2)

Name	Count	Type	Description
PCIE_RC#	1	Reset Strap	PCI-E Root Complex: Determines whether PCI Express* interface operates as an endpoint or a root complex. 0 = Root complex 1 = Endpoint (default mode) ***Note:*** Root Complex is not supported. ***Note:*** Muxed onto signal **A[12]** Setting both **PCIX_EP#** and **PCIE_RC#** to endpoint is unsupported.
SMB_A5, **SMB_A3**, **SMB_A2**, **SMB_A1**	4	Reset Strap	SM Bus Address: Maps to address bit[5], bit[3], bit[2], and bit[1] where bits[7:0] represent address SMBus slave port responds to when access is attempted. 0 = Address bit is low 1 = Address bit is high (default mode) ***Note:*** **SMB_A5** muxed onto signal **A[16]** ***Note:*** **SMB_A3** muxed onto signal **A[15]** ***Note:*** **SMB_A2** muxed onto signal **A[14]** ***Note:*** **SMB_A1** muxed onto signal **A[13]**
PCIX_PULLUP#	1	Reset Strap	0 = PCI-X Pull Up: Determines whether PCI interface has on-die pull-ups enabled. Enable PCI pull-up resistors 1 = Disable PCI pull-up resistors (default mode) ***Note:*** Muxed onto signal **A[17]**
PCIX_32BIT#	1	Reset Strap	32-Bit PCI-X Bus: Indicates width of the PCI-X bus to PCI-X Status Register. Enables pull-ups for upper half of bus when in 32-bit mode. 0 = 32-bit wide PCI-X bus 1 = 64-bit wide PCI-X bus (default mode) ***Note:*** Muxed onto signal **A[18]**
PCIXM1_100#	1	Reset Strap	PCI-X Mode 1 100 MHz Enable: this bit limits PCI-X bus to 100 MHz while in mode 1: 0 = Limit PCI-X mode 1 to 100 MHz 1 = 133 MHz enabled (default mode) ***Note:*** Muxed onto signal **A[19]**
HS_SM#	1	Reset Strap	Hot Swap Startup Mode: In End Point Mode, this bit determines whether Hot Swap mode is enabled. 0 = Hot Swap Mode enabled 1 = Hot Swap Mode disabled (default mode) ***Note:*** Muxed onto signal **A[21]**
FW_TIMER_OFF#	1	Reset Strap	Firmware Timer Off: Disables 400 mS firmware timer for development and debug. When enabled, timer automatically clears Configuration Cycle Retry (CCR) bit in PCSR after 400 mS regardless of processor state. When disabled, CCR bit functions as normal based on state of CFG_CYCLE_EN# pin at rising edge of P_RST#. 0 = Firmware timer disabled 1 = Firmware timer enabled (default mode) ***Note:*** Muxed onto signal **A[22]**
LK_DN_RST_BYPASS#	1	Reset Strap	Link Down Reset Bypass: Disables the full chip reset that would normally be caused by a Link Down or hot reset. 0 = Do not reset on Link Down 1 = Reset on Link Down (default mode) ***Note:*** Muxed onto signal **A[24]**
CLK_SRC_PCIE#	1	Reset Strap	Clock Source PCI-E: Selects PCI Express* Refclk pair as the input clock to the PLLs that control most internal logic. 0 = Source clock is **REFCLKP**/**REFCLKN** 1 = Source clock is **P_CLKIN** (default mode) ***Note:*** When **P_CLKO[3:0]** are used this pin must be pulled low. ***Note:*** Muxed onto signal **PWE#**
Total	24		

Reset strap signals are latched on the rising edge of **P_RST#**. All reset strap signals are internally pulled to logic 1 by default. An external 4.7KW 5%, 1/16W pull-down resistor is required to force a logic 0 on these pins.

Table 13. Functional Pin Mode Behavior (Sheet 1 of 3)

Pin	Boundary Scan High Z	Reset (End Point)	(Central Resource) Not supported	Normal	32-Bit SDRAM	PCIX_32BIT#	PCIX_PULLUP#	When only PCI-X Interface Active	When only PCI Express* Interface Active
A[24:0]	Z	H	H	VO	–	–	–	–	–
D[15:0]	Z	H	H	VB	–	–	–	–	–
POE#	Z	H	H	VO	–	–	–	–	–
PWE#	Z	H	H	VO	–	–	–	–	–
PB_RSTOUT#	Z	0	0	VO	–	–	–	–	–
PCE[1:0]#	Z	H	H	VO	–	–	–	–	–
HS_ENUM#	Z	Z	Z	VO	–	–	–	–	–
HS_LSTAT	–	VI	VI	VI	–	–	–	–	–
HS_LED_OUT	Z	1	1	VO	–	–	–	–	–
HS_FREQ[1:0]	Z	H	H	H	–	–	–	–	–
P_AD[63:32]	Z	Z	Z	VB	–	H	H	–	H
P_AD[31:0]	Z	Z	0	VB	–	–	–	–	H
P_CBE[7:4]#	Z	Z	Z	VB	–	H	H	–	H
P_CBE[3:0]#	Z	Z	0	VB	–	–	–	–	H
P_PAR64	Z	Z	Z	VB	–	H	H	–	H
P_REQ64#	Z	VI	0	VB	–	–	H	–	H
P_ACK64#	Z	Z	Z	VB	–	–	H	–	H
P_PAR	Z	Z	0	VB	–	–	–	–	H
P_FRAME#	Z	VI	VO	VB	–	–	H	–	H
P_IRDY#	Z	VI	VO	VB	–	–	H	–	H
P_TRDY#	Z	VI	VO	VB	–	–	H	–	H
P_STOP#	Z	VI	VO	VB	–	–	H	–	H
P_DEVSEL#	Z	VI	VO	VB	–	–	H	–	H
P_SERR#	Z	Z	Z	VB	–	–	H	–	H
P_RSTOUT#	Z	0	0	VO	–	–	–	–	VO
P_PERR#	Z	VI	VO	VB	–	–	H	–	H
P_M66EN	–	VI	VI	VI	–	–	–	–	H
P_IDSEL	–	VI	VI	VI	–	–	–	–	H
P_REQ#	Z	$Z_{(EA)}$	$Z_{(EA)}$	VO	–	–	–	–	H
P_GNT#	–	$VI_{(EA)}$	$VI_{(EA)}$	$VI_{(EA)}$	–	–	–	–	H
P_CLKIN	–	VI	VI	VI	–	–	–	–	GND
P_PCIXCAP	–	AI	AI	AI	–	–	–	–	GND
P_BMI	Z	VO	VO	VO	–	–	–	–	VO

1 = driven to V_{CC}
0 = driven to V_{SS}
X = driven to unknown state
ID = The input is disabled.
H = pulled up to V_{CC}
PD = pull-up disabled
L = pulled down to V_{SS}
ODT = On Die Termination
GND = Tie to Ground.
EA = External Arbiter mode
IA = Internal Arbiter mode
Z = output, pull-up/down disabled
VB = acts like a Valid Bidirectional pin
VO = a Valid Output level is driven.
VI = need to drive a Valid Input level.
AO = Analog Output level
AI = Analog Input level
* = after power fail sequence completes
"-" = unaffected by this mode

Table 13. Functional Pin Mode Behavior (Sheet 2 of 3)

Pin	Boundary Scan High Z	Reset (End Point)	(Central Resource) Not supported	Normal	32-Bit SDRAM	PCIX_32BIT#	PCIX_PULLUP#	When only PCI-X Interface Active	When only PCI Express* Interface Active
P_CAL[2:0]	Z	AO	AO	AO	–	–	–	–	VO
S_CLKP0, S_CLKN0	–	VI	VI	VI	–	–	–	–	–
S_TXP[7:0], S_TXN[7:0]	–	1	1	VO	–	–	–	–	–
S_RXP[7:0], S_RXN[7:0]	–	ID	ID	VI	–	–	–	–	–
RBIAS[1:0]	–	AO	AO	AO	–	–	–	–	–
RBIAS_SENSE[1:0]	–	AI	AI	AI	–	–	–	–	–
S_ACT0 / SCLOCK0	Z	Z	Z	VO	–	–	–	–	–
S_STAT0 / SLOAD0	Z	Z	Z	VO	–	–	–	–	–
S_ACT1	Z	Z	Z	VO	–	–	–	–	–
S_STAT1	Z	Z	Z	VO	–	–	–	–	–
S_ACT2 / SDATAIN0	Z	Z	Z	VO	–	–	–	–	–
S_STAT2 / SDATAOUT0	Z	Z	Z	VO	–	–	–	–	–
S_ACT3	Z	Z	Z	VO	–	–	–	–	–
S_STAT3	Z	Z	Z	VO	–	–	–	–	–
S_ACT4 / SCLOCK1	Z	Z	Z	VO	–	–	–	–	–
S_STAT4 / SLOAD1	Z	Z	Z	VO	–	–	–	–	–
S_ACT5	Z	Z	Z	VO	–	–	–	–	–
S_STAT5	Z	Z	Z	VO	–	–	–	–	–
S_ACT6 / SDATAIN1	Z	Z	Z	VO	–	–	–	–	–
S_STAT6 / SDATAOUT1	Z	Z	Z	VO	–	–	–	–	–
S_ACT7	Z	Z	Z	VO	–	–	–	–	–
S_STAT7	Z	Z	Z	VO	–	–	–	–	–
REFCLKP, REFCLKN	–	VI	VI	VI	–	–	–	GND/ VI	–
PETP[7:0], PETN[7:0]	–	Z	Z	VO	–	–	–	Z	–
PERP[7:0], PERN[7:0]	–	ID	ID	VI	–	–	–	Z	–
PE_CALP	–	AO	AO	AO	–	–	–	Z	–
PE_CALN	–	AO	AO	AO	–	–	–	Z	–
P_INT[D:A]# / XINT[3:0]#	Z	Z/VI	Z/VI	VB	–	–	H	–	–
XINT[7:4]#	–	VI	VI	VI	–	–	–	–	–
GPIO[7:0] / XINT[15:8]#	Z	VI	VI	VB	–	–	–	–	–

1 = driven to V_{CC}
0 = driven to V_{SS}
X = driven to unknown state
ID = The input is disabled.
H = pulled up to V_{CC}
PD = pull-up disabled
L = pulled down to V_{SS}
ODT = On Die Termination
GND = Tie to Ground.
EA = External Arbiter mode
IA = Internal Arbiter mode
Z = output, pull-up/down disabled
VB = acts like a Valid Bidirectional pin
VO = a Valid Output level is driven.
VI = need to drive a Valid Input level.
AO = Analog Output level
AI = Analog Input level
* = after power fail sequence completes
"-" = unaffected by this mode

Table 13. Functional Pin Mode Behavior (Sheet 3 of 3)

Pin	Boundary Scan High Z	Reset (End Point)	(Central Resource) Not supported	Normal	32-Bit SDRAM	PCIX_32BIT#	PCIX_PULLUP#	When only PCI-X Interface Active	When only PCI Express* Interface Active
HPI#	–	VI	VI	VI	–	–	–	–	–
NMI0#	–	VI	VI	VI	–	–	–	–	–
NMI1#	–	VI	VI	VI	–	–	–	–	–
SCL0	Z	Z	Z	VB	–	–	–	–	–
SDA0	Z	Z	Z	VB	–	–	–	–	–
SCL1	Z	Z	Z	VB	–	–	–	–	–
SDA1	Z	Z	Z	VB	–	–	–	–	–
SCL2	Z	Z	Z	VB	–	–	–	–	–
SDA2	Z	Z	Z	VB	–	–	–	–	–
SMBCLK	Z	Z	Z	VB	–	–	–	–	–
SMBDAT	Z	Z	Z	VB	–	–	–	–	–
U0_RXD	–	VI	VI	VI	–	–	–	–	–
U0_TXD	Z	1	1	VO	–	–	–	–	–
U0_CTS#	–	VI	VI	VI	–	–	–	–	–
U0_RTS#	Z	1	1	VO	–	–	–	–	–
U1_RXD	–	VI	VI	VI	–	–	–	–	–
U1_TXD	Z	1	1	VO	–	–	–	–	–
U1_CTS#	–	VI	VI	VI	–	–	–	–	–
U1_RTS#	Z	1	1	VO	–	–	–	–	–
TCK	–	VI	VI	VI	–	–	–	–	–
TDI	–	H	H	H	–	–	–	–	–
TDO	–	Z	Z	VO	–	–	–	–	–
TRST#	–	H	H	H	–	–	–	–	–
TMS	–	H	H	H	–	–	–	–	–
P_RST#	–	VI	VI	VI	–	–	–	–	–
WARM_RST#	–	VI	VI	VI	–	–	–	–	–
NC	-/Z	Z/H	Z/H	Z/H	–	–	–	–	–
THERMDA	–	AI	AI	AI	–	–	–	–	–
THERMDC	–	AO	AO	AO	–	–	–	–	–

1 = driven to V_{CC}
0 = driven to V_{SS}
X = driven to unknown state
ID = The input is disabled.
H = pulled up to V_{CC}
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ODT = On Die Termination
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EA = External Arbiter mode
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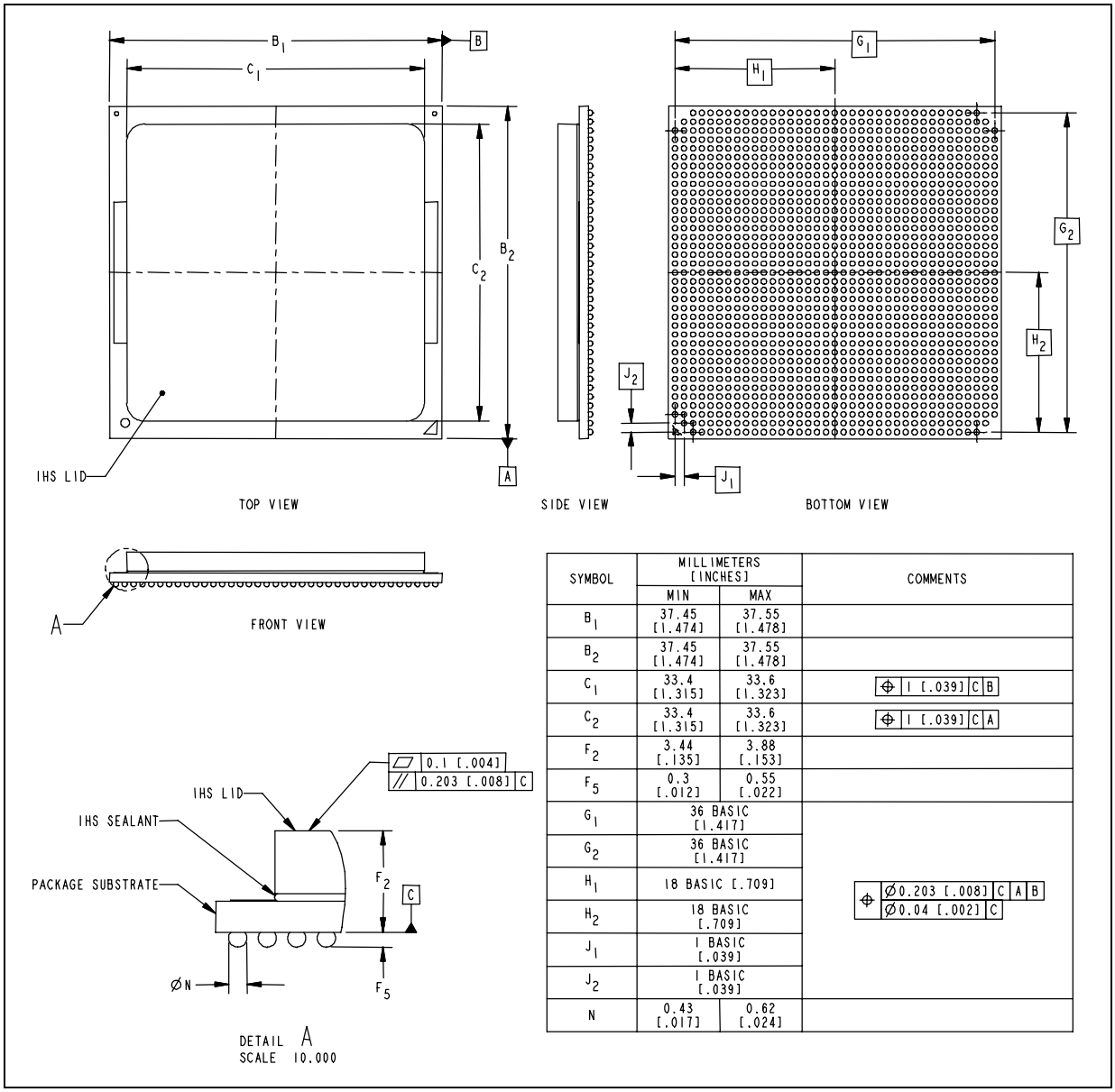
Z = output, pull-up/down disabled
VB = acts like a Valid Bidirectional pin
VO = a Valid Output level is driven.
VI = need to drive a Valid Input level.
AO = Analog Output level
AI = Analog Input level
* = after power fail sequence completes
"-" = unaffected by this mode

Figure 2. 1357-Lead FCBGA Package (Top and Bottom Views)



SYMBOL	MILLIMETERS [INCHES]		COMMENTS
	MIN	MAX	
B_1	37.45 [1.474]	37.55 [1.478]	
B_2	37.45 [1.474]	37.55 [1.478]	
C_1	33.4 [1.315]	33.6 [1.323]	⌖ | 1 [.039] | C | B
C_2	33.4 [1.315]	33.6 [1.323]	⌖ | 1 [.039] | C | A
F_2	3.44 [.135]	3.88 [.153]	
F_5	0.3 [.012]	0.55 [.022]	
G_1	36 BASIC [1.417]		
G_2	36 BASIC [1.417]		
H_1	18 BASIC [.709]		⌖ | Ø0.203 [.008] | C | A | B Ø0.04 [.002] | C
H_2	18 BASIC [.709]		
J_1	1 BASIC [.039]		
J_2	1 BASIC [.039]		
N	0.43 [.017]	0.62 [.024]	

The following figures show the 413808 and 413812 ballout diagrams:

The following tables show the 413808 and 413812 ball and signal listings:

Figure 3. 413808 and 413812 Ballout—Package Top (Left Side)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W
37			vss	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
36		vss	nc	nc	nc	vss	nc	nc	vss	vss	nc	nc	vss	nc	nc	vss	nc	nc	nc
35	vss	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	vss	nc
34	nc	nc	vss	nc	nc	vss	nc	nc	vss	vss	nc	nc	vss	nc	nc	vss	nc	nc	nc
33	nc	nc	nc	nc	vss	nc	nc	nc	nc	nc	nc	vss	nc	nc	nc	nc	nc	nc	vss
32	nc	nc	nc	nc	nc	vcc3 p3	vcc3 p3	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8
31	nc	nc	nc	nc	nc	nc	vcc3 p3	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss
30	nc	vss	nc	vss	nc	nc	vcc3 p3	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x
29	nc	nc	nc	nc	nc	nc	vcc3 p3	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss pllx	therm da	nc
28	nc	nc	nc	nc	nc	nc	vcc3 p3	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	therm dc	vcc1 p2x
27	s_a ct1	vss	s_ stat5	vss	s_ act4	s_ stat3	vcc3 p3	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss
26	s_ act5	s_ stat2	s_ act0	s_ stat7	s_ stat6	s_ stat4	vcc3 p3	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x
25	s_ stat0	s_ act2	s_ act3	s_ act7	s_ stat1	s_ act6	vcc3 p3	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss
24	vssas	vssas	vssas	vssas	vcc1 p2as	vcc1 p2as	vcc1 p2as	vss	vcc1 p2	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x
23	s_ rxp[3]	s_ rxn[3]	s_ txp[3]	s_ txn[3]	vcc1 p2as	vcc1 p2as	vcc1 p2as	vcc1 p2	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss
22	s_ rxp [1]	s_ rxn [1]	s_ txp [1]	s_ txn [1]	vcc1 p2as	vcc1 p2as	vcc1 p2as	vss	vcc1 p2	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x
21	vssas	vssas	vssas	vssas	rbias_ sense [0]	nc	nc	s_ clkp0	vss plls0	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss
20	s_ rxp [0]	s_ rxn [0]	s_ txp [0]	s_ txn [0]	rbias [0]	nc	nc	s_ clkn0	vcc1 p2plls0	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2
19	s_ rxp [2]	s_ rxn [2]	s_ txp [2]	s_ txn [2]	vcc1 p8s	vcc1 p8s	vcc1 p8s	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss
18	vssas	vssas	vssas	vssas	vcc1 p8s	vcc1 p8s	vcc1 p8s	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2
17	s_ rxp [7]	s_ xn [7]	s_ txp [7]	s_ txn [7]	vcc1 p2ds	vssds	vssds	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss
16	s_ rxp [5]	s_ rxn [5]	s_ txp [5]	s_ txn [5]	rbias_ sense [1]	nc	nc	vss	vss plls1	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2
15	vssas	vssas	vssas	vssas	rbias [1]	nc	nc	vss	vcc1 p2plls1	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss
14	s_ rxp [4]	s_ rxn [4]	s_ txp [4]	s_ txn [4]	vssds	vcc1 p2ds	vssds	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2
13	s_ rxp [6]	s_r xn [6]	s_ txp [6]	s_ txn [6]	vcc1 p2ds	vssds	vcc1 p2ds	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss
12	vssas	vssas	vssas	vssas	vssds	vcc1 p2ds	vcc1 p2ds	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2
11	gpio [1]	gpio [3]	gpio [7]	gpio [5]	gpio [6]	vcc3 p3	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vsspllp	vcc1 p2pllp	vss	vcc1 p2	vss	vcc1 p2	vss
10	gpio [0]	vss	gpio [2]	vss	gpio [4]	vcc3 p3	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2
9	xint# [1]	xint# [3]	xint# [5]	xint# [4]	xint# [7]	vcc3 p3	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss
8	xint# [2]	xint# [0]	xint# [6]	nmi0#	hs_ led_ out	vcc3 p3	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2
7	hs_ enum#	vss	hpi#	vss	nmi1#	vcc3 p3	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss
6	u0_ rts#	u0_ rxd	hs_ lstat	hs_ freq [1]	hs_ freq [0]	vcc3 p3	vcc3 p3	vcc vio	vcc3 p3	vcc3 p3	vcc vio	vcc vio	vcc3 p3	vcc vio	vcc3 p3	vcc3 p3	vcc vio	vcc3 p3	vcc3 p3
5	u0_ cts#	u0_ txd	u1_ rxd	nc	vcc3 p3	p_ cal [0]	nc	vcc vio	p_ req#	p_ ad [31]	vcc vio	p_ ad [26]	p_ idsel	vcc vio	p_ ad[16]	p_ trdy#	vcc vio	p_ad [13]	p_ad [9]
4	u1_ cts#	u1_ txd	u1_ rts#	vss	warm_ rst#	p_ bmi	vss	nc	nc	vss	p_ ad [30]	p_ ad [24]	vss	p_ ad [20]	p_ frame#	vss	p_ par	p_a d[11]	vss
3	vss	nc	nc	p_ cal[2]	nc	p_ cal[1]	nc	nc	nc	p_ ad[27]	p_ ad[28]	p_ ad[23]	p_ ad[22]	p_ ad[18]	p_ devsel #	p_ stop#	p_ ad[15]	p_ ad[12]	p_ cbe# [0]
2		vss	nc	nc	vss	p_ rst#	vss	nc	nc	vss	p_ ad[25]	p_ ad[21]	vss	p_ cbe# [2]	p_ pcixca p	vss	p_ cbe# [1]	p_ ad[10]	vss
1			vss	p_ clkin	nc	p_ rstout#	nc	nc	p_ gnt#	p_ ad[29]	p_ cbe# [3]	p_ ad[19]	p_ ad[17]	p_ irdy#	p_ perr#	p_ serr#	p_ ad[14]	p_ m66en	vss

Figure 4. 413808 and 413812 Ballout—Package Top (Right Side)

Y	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	AP	AR	AT	AU	
nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	vss			37
nc	nc	vss	nc	nc	vss	nc	nc	vss	vss	nc	nc	vss	nc	nc	nc	vss		36
vss	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	vss	35
nc	nc	vss	nc	nc	vss	nc	nc	vss	vss	nc	nc	vss	nc	nc	vss	nc	vss	34
nc	nc	nc	nc	vss	nc	nc	nc	nc	nc	nc	vss	nc	nc	nc	nc	vss	vss	33
vcc 1p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	32
vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc3 p3	vcc3 p3	vss	tck	vss	trst#	31
vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vcc3 p3	vcc3 p3	vcc3 p3	tdo	tms	tdi	30
vcc3 p3pllx	vss	vcc1 p2x	vss plld	vcc1 p2plld	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc3 p3	scl1	sda2	sda1	scl0	smbclk	29
vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vcc3p3	scl2	vss	sda0	vss	smbdat	28
vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vcc1 p2x	vcc1 p2x	vcc1 p2x	vcc1 p2x	vcc1 p2x	vcc1 p2x	vcc1 p2x	vcc1 p2x	vcc1 p2x	27
vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vcc1 p8e	vcc1 p8e	vcc1 p8e	vcc1 p8e	vcc1 p8e	vcc1 p8e	26
vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p8e	vcc1 p8e	vsse	vsse	vsse	vsse	25
vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vcc1 p2ae	vcc1 p8e	petn [7]	petp [7]	pern [7]	perp [7]	24
vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2	vss	vcc1 p2ae	vcc1 p8e	petn [6]	petp [6]	pern [6]	perp [6]	23
vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2	vss	vcc1 p2	vcc1 p2ae	vcc1 p8e	vsse	vsse	vsse	vsse	22
vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2ae	vcc1 p8e	petn [5]	petp [5]	pern [5]	perp [5]	21
vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	refclkp	nc	nc	pe_ calp	petn [4]	petp [4]	pern [4]	perp [4]	20
vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	refclkn	nc	nc	pe_ caln	vsse	vsse	vsse	vsse	19
vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vcc1 p2ae	vcc1 p8e	petn [3]	petp [3]	pern [3]	perp [3]	18
vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2ae	vcc1 p8e	petn [2]	petp [2]	pern [2]	perp [2]	17
vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vcc1 p2ae	vcc1 p2e	vsse	vsse	vsse	vsse	16
vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2ae	vcc1 p2e	petn [1]	petp [1]	pern [1]	perp [1]	15
vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vcc1 p2e	vcc1 p2e	petn [0]	petp [0]	pern [0]	perp [0]	14
vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2e	vcc1 p2e	vsse	vsse	vsse	vsse	13
vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vcc1 p2	vcc1 p2	vcc1 p2	vcc1 p2	vcc1 p2	vcc1 p2	12
vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc3 p3	poe# [1]	a[21]	a[19]	a[18]	a[22]	11
vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vcc3p3	a[20]	vss	pce# [0]	vss	a[13]	10
vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc3 p3	nc	a[9]	a[12]	a[8]	a[14]	9
vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vcc3 p3	PUR1	a[10]	pb_ rstout#	a[1]	a[6]	8
vcc 1p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc 3p3	a[11]	vss	a[15]	vss	a[2]	7
vcc vio	vcc vio	vcc3 p3	vcc vio	vcc vio	vcc3 p3	vcc vio	vcc vio	vcc3 p3	vcc vio	vcc vio	vcc3 p3	vcc3 p3	d[15]	a[16]	a[17]	a[3]	a[7]	6
p_ ad [4]	vcc vio	p_ cbe# [7]	p_ par 64	vcc vio	p_ ad [56]	p_ ad [52]	vcc vio	p_ ad [44]	p_ ad [40]	vcc vio	p_ ad [32]	d[10]	vcc3 p3	d[9]	d[4]	a[4]	a[5]	5
p_ad [6]	p_ad [0]	vss	p_ cbe# [5]	p_ad [60]	vss	p_ad [54]	p_ad [48]	vss	p_ad [42]	p_ad [36]	vss	poe#	d[2]	vss	d[3]	d[8]	d[1]	4
p_ad [5]	p_ad [2]	p_ req 64#	p_ad [63]	p_ad [62]	p_ad [58]	p_ad [51]	p_ad [50]	p_ad [46]	p_ad [39]	p_ad [38]	p_ad [34]	pwe#	d[12]	d[11]	a[23]	d[0]	vss	3
p_ad [7]	p_ad [1]	vss	p_ cbe# [4]	p_ad [59]	vss	p_ad [53]	p_ad [47]	vss	p_ad [41]	p_ad [35]	vss	d[14]	d[6]	d[5]	a[0]	vss		2
p_ad [8]	p_ad [3]	p_ ack 64#	p_ cbe# [6]	p_ad [61]	p_ad [57]	p_ad [55]	p_ad [49]	p_ad [45]	p_ad [43]	p_ad [37]	p_ad [33]	a[24]	d[7]	d[13]	vss			1

Figure 5. 413808 and 413812 Ballout—Package Bottom (Left Side)

	AU	AT	AR	AP	AN	AM	AL	AK	AJ	AH	AG	AF	AE	AD	AC	AB	AA	Y	W
37			vss	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
36		vss	nc	nc	nc	vss	nc	nc	vss	vss	nc	nc	vss	nc	nc	vss	nc	nc	nc
35	vss	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	vss	nc
34	vss	nc	vss	nc	nc	vss	nc	nc	vss	vss	nc	nc	vss	nc	nc	vss	nc	nc	nc
33	vss	vss	nc	nc	nc	nc	vss	nc	nc	nc	nc	nc	nc	vss	nc	nc	nc	nc	vss
32	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8
31	trst#	vss	tck	vss	vcc3p3	vcc3p3	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss
30	tdi	tms	tdo	vcc3p3	vcc3p3	vcc3p3	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x
29	smbclk	scl0	sda1	sda2	scl1	vcc3p3	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1 p2plld	vsspllld	vcc1p2x	vss	vcc3 p3pllx	nc
28	smbdat	vss	sda0	vss	scl2	vcc3p3	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x
27	vcc1p2x	vcc1p2x	vcc1p2x	vcc1p2x	vcc1p2x	vcc1p2x	vcc1p2x	vcc1p2x	vcc1p2x	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss
26	vcc1p8e	vcc1p8e	vcc1p8e	vcc1p8e	vcc1p8e	vcc1p8e	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x
25	vsse	vsse	vsse	vsse	vcc1p8e	vcc1p8e	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss
24	perp[7]	pern[7]	petp[7]	petn[7]	vcc1p8e	vcc1 p2ae	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x
23	perp[6]	pern[6]	petp[6]	petn[6]	vcc1p8e	vcc1 p2ae	vss	vcc1p2	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss
22	vsse	vsse	vsse	vsse	vcc1p8e	vcc1 p2ae	vcc1p2	vss	vcc1p2	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x
21	perp[5]	pern[5]	petp[5]	petn[5]	vcc1p8e	vcc1 p2ae	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
20	perp[4]	pern[4]	petp[4]	petn[4]	pe_calp	nc	nc	refclkp	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
19	vsse	vsse	vsse	vsse	pe_caln	nc	nc	refclkn	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
18	perp[3]	pern[3]	petp[3]	petn[3]	vcc1p8e	vcc1 p2ae	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
17	perp[2]	pern[2]	petp[2]	petn[2]	vcc1p8e	vcc1 p2ae	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
16	vsse	vsse	vsse	vsse	vcc1p2e	vcc1 p2ae	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
15	perp[1]	pern[1]	petp[1]	petn[1]	vcc1p2e	vcc1 p2ae	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
14	perp[0]	pern[0]	petp[0]	petn[0]	vcc1p2e	vcc1p2e	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
13	vsse	vsse	vsse	vsse	vcc1p2e	vcc1p2e	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
12	vcc1p2	vcc1p2	vcc1p2	vcc1p2	vcc1p2	vcc1p2	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
11	a[22]	a[18]	a[19]	a[21]	pce#[1]	vcc3p3	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
10	a[13]	vss	pce#[0]	vss	a[20]	vcc3p3	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
9	a[14]	a[8]	a[12]	a[9]	nc	vcc3p3	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
8	a[6]	a[1]	pb_ rstout#	a[10]	PUR1	vcc3p3	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
7	a[2]	vss	a[15]	vss	a[11]	vcc3p3	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
6	a[7]	a[3]	a[17]	a[16]	d[15]	vcc3p3	vcc3p3	vccvio	vccvio	vcc3p3	vccvio	vccvio	vcc3p3	vccvio	vccvio	vcc3p3	vccvio	vccvio	vcc3p3
5	a[5]	a[4]	d[4]	d[9]	vcc3p3	d[10]	p_ad[32]	vccvio	p_ad[40]	p_ad[44]	vccvio	p_ad[52]	p_ad[56]	vccvio	p_par64	p_cbe#[7]	vccvio	p_ad[4]	p_ad[9]
4	d[1]	d[8]	d[3]	vss	d[2]	poe#	vss	p_ad[36]	p_ad[42]	vss	p_ad[48]	p_ad[54]	vss	p_ad[60]	p_cbe#[5]	vss	p_ad[0]	p_ad[6]	vss
3	vss	d[0]	a[23]	d[11]	d[12]	pwe#	p_ad[34]	p_ad[38]	p_ad[39]	p_ad[46]	p_ad[50]	p_ad[51]	p_ad[58]	p_ad[62]	p_ad[63]	p_req64#	p_ad[2]	p_ad[5]	p_cbe#[0]
2		vss	a[0]	d[5]	d[6]	d[14]	vss	p_ad[35]	p_ad[41]	vss	p_ad[47]	p_ad[53]	vss	p_ad[59]	p_cbe#[4]	vss	p_ad[1]	p_ad[7]	vss
1			vss	d[13]	d[7]	a[24]	p_ad[33]	p_ad[37]	p_ad[43]	p_ad[45]	p_ad[49]	p_ad[55]	p_ad[57]	p_ad[61]	p_cbe#[6]	p_ack64#	p_ad[3]	p_ad[8]	vss

Figure 6. 413808 and 413812 Ballout—Package Bottom (Right Side)

V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	vss			37
nc	nc	vss	nc	nc	vss	nc	nc	vss	vss	nc	nc	vss	nc	nc	nc	vss		36
vss	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc	vss	35
nc	nc	vss	nc	nc	vss	nc	nc	vss	vss	nc	nc	vss	nc	nc	vss	nc	nc	34
nc	nc	nc	nc	nc	nc	vss	nc	nc	nc	nc	nc	nc	vss	nc	nc	nc	nc	33
vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc3p3	vcc3p3	nc	nc	nc	nc	nc	32
vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vcc3p3	nc	nc	nc	nc	nc	nc	31
vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc3p3	nc	nc	vss	nc	vss	nc	30
thermda	vsspllx	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vcc3p3	nc	nc	nc	nc	nc	nc	29
thermdc	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc3p3	nc	nc	nc	nc	nc	nc	28
vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vcc3p3	s_stat3	s_act4	vss	s_stat5	vss	s_act1	27
vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc3p3	s_stat4	s_stat6	s_stat7	s_act0	s_stat2	s_act5	26
vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vcc3p3	s_act6	s_stat1	s_act7	s_act3	s_act2	s_stat0	25
vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2	vss	vcc1p2as	vcc1p2as	vcc1p2as	vssas	vssas	vssas	vssas	24
vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2	vcc1p2as	vcc1p2as	vcc1p2as	s_txn[3]	s_txp[3]	s_rxn[3]	s_rxp[3]	23
vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2	vss	vcc1p2as	vcc1p2as	vcc1p2as	s_txn[1]	s_txp[1]	s_rxn[1]	s_rxp[1]	22
vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vsspllso	s_clkp0	nc	nc	rbias_sense[0]	vssas	vssas	vssas	vssas	21
vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2pllso	s_clkn0	nc	nc	rbias[0]	s_txn[0]	s_txp[0]	s_rxn[0]	s_rxp[0]	20
vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vcc1p8s	vcc1p8s	vcc1p8s	s_txn[2]	s_txp[2]	s_rxn[2]	s_rxp[2]	19
vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p8s	vcc1p8s	vcc1p8s	vssas	vssas	vssas	vssas	18
vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vssds	vssds	vcc1p2ds	s_txn[7]	s_txp[7]	s_rxn[7]	s_rxp[7]	17
vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vsspllsl	vss	nc	nc	rbias_sense[1]	s_txn[5]	s_txp[5]	s_rxn[5]	s_rxp[5]	16
vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vcc1p2pllsl	vss	nc	nc	rbias[1]	vssas	vssas	vssas	vssas	15
vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vssds	vcc1p2ds	vssds	s_txn[4]	s_txp[4]	s_rxn[4]	s_rxp[4]	14
vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vcc1p2ds	vssds	vcc1p2ds	s_txn[6]	s_txp[6]	s_rxn[6]	s_rxp[6]	13
vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2ds	vcc1p2ds	vssds	vssas	vssas	vssas	vssas	12
vcc1p2	vss	vcc1p2	vss	vcc1p2pllp	vsspllp	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc3p3	gpio[6]	gpio[5]	gpio[7]	gpio[3]	gpio[1]	11
vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vcc3p3	gpio[4]	vss	gpio[2]	vss	gpio[0]	10
vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc3p3	xint#[7]	xint#[4]	xint#[5]	xint#[3]	xint#[1]	9
vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vcc3p3	hs_led_out	nmi0#	xint#[6]	xint#[0]	xint#[2]	8
vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc3p3	nmi1#	vss	hpi#	vss	hs_enum#	7
vcc3p3	vccvio	vcc3p3	vcc3p3	vccvio	vcc3p3	vccvio	vccvio	vcc3p3	vcc3p3	vccvio	vcc3p3	vcc3p3	hs_freq[0]	hs_freq[1]	hs_lstat	u0_rxd	u0_rts#	6
p_ad[13]	vccvio	p_trdy#	p_ad[16]	vccvio	p_idsel	p_ad[26]	vccvio	p_ad[31]	p_req#	vccvio	nc	p_cal[0]	vcc3p3	nc	u1_rxd	u0_txd	u0_cts#	5
p_ad[11]	p_par	vss	p_frame#	p_ad[20]	vss	p_ad[24]	p_ad[30]	vss	nc	nc	vss	p_bmi	warm_rst#	vss	u1_rts#	u1_txd	u1_cts#	4
p_ad[12]	p_ad[15]	p_stop#	p_devsel#	p_ad[18]	p_ad[22]	p_ad[23]	p_ad[28]	p_ad[27]	nc	nc	nc	p_cal[1]	nc	p_cal[2]	nc	nc	vss	3
p_ad[10]	p_cbe#[1]	vss	p_pcixcap	p_cbe#[2]	vss	p_ad[21]	p_ad[25]	vss	nc	nc	vss	p_rst#	vss	nc	nc	vss		2
p_m66en	p_ad[14]	p_serr#	p_perr#	p_irdy#	p_ad[17]	p_ad[19]	p_cbe#[3]	p_ad[29]	p_gnt#	nc	nc	p_rstout#	nc	p_clkin	vss			1

Table 14. 413808 and 413812 1357-Lead Package - Alphabetical Ball Listings (Sheet 1 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
A1	-	B7	vss	C13	s_txp[6]
A2	-	B8	xint#[0]	C14	s_txp[4]
A3	vss	B9	xint#[3]	C15	vssas
A4	u1_cts#	B10	vss	C16	s_txp[5]
A5	u0_cts#	B11	gpio[3]	C17	s_txp[7]
A6	u0_rts#	B12	vssas	C18	vssas
A7	hs_enum#	B13	s_rxn[6]	C19	s_txp[2]
A8	xint#[2]	B14	s_rxn[4]	C20	s_txp[0]
A9	xint#[1]	B15	vssas	C21	vssas
A10	gpio[0]	B16	s_rxn[5]	C22	s_txp[1]
A11	gpio[1]	B17	s_rxn[7]	C23	s_txp[3]
A12	vssas	B18	vssas	C24	vssas
A13	s_rxp[6]	B19	s_rxn[2]	C25	s_act3
A14	s_rxp[4]	B20	s_rxn[0]	C26	s_act0
A15	vssas	B21	vssas	C27	s_stat5
A16	s_rxp[5]	B22	s_rxn[1]	C28	nc
A17	s_rxp[7]	B23	s_rxn[3]	C29	nc
A18	vssas	B24	vssas	C30	nc
A19	s_rxp[2]	B25	s_act2	C31	nc
A20	s_rxp[0]	B26	s_stat2	C32	nc
A21	vssas	B27	vss	C33	nc
A22	s_rxp[1]	B28	nc	C34	vss
A23	s_rxp[3]	B29	nc	C35	nc
A24	vssas	B30	vss	C36	nc
A25	s_stat0	B31	nc	C37	vss
A26	s_act5	B32	nc	D1	p_clkin
A27	s_act1	B33	nc	D2	nc
A28	nc	B34	nc	D3	p_cal[2]
A29	nc	B35	nc	D4	vss
A30	nc	B36	vss	D5	nc
A31	nc	B37	-	D6	hs_freq[1]
A32	nc	C1	vss	D7	vss
A33	nc	C2	nc	D8	nmi0#
A34	nc	C3	nc	D9	xint#[4]
A35	vss	C4	u1_rts#	D10	vss
A36	-	C5	u1_rxd	D11	gpio[5]
A37	-	C6	hs_lstat	D12	vssas
B1	-	C7	hpi#	D13	s_txn[6]
B2	vss	C8	xint#[6]	D14	s_txn[4]
B3	nc	C9	xint#[5]	D15	vssas
B4	u1_txd	C10	gpio[2]	D16	s_txn[5]
B5	u0_txd	C11	gpio[7]	D17	s_txn[7]
B6	u0_rxd	C12	vssas	D18	vssas
D19	s_txn[2]	E25	s_stat1	F31	nc

Table 14. 413808 and 413812 1357-Lead Package - Alphabetical Ball Listings (Sheet 2 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
D20	s_txn[0]	E26	s_stat6	F32	vcc3p3
D21	vssas	E27	s_act4	F33	nc
D22	s_txn[1]	E28	nc	F34	vss
D23	s_txn[3]	E29	nc	F35	nc
D24	vssas	E30	nc	F36	vss
D25	s_act7	E31	nc	F37	nc
D26	s_stat7	E32	nc	G1	nc
D27	vss	E33	vss	G2	vss
D28	nc	E34	nc	G3	nc
D29	nc	E35	nc	G4	vss
D30	vss	E36	nc	G5	nc
D31	nc	E37	nc	G6	vcc3p3
D32	nc	F1	p_rstout#	G7	vss
D33	nc	F2	p_rst#	G8	vcc1p2
D34	nc	F3	p_cal[1]	G9	vss
D35	nc	F4	p_bmi	G10	vcc1p2
D36	nc	F5	p_cal[0]	G11	vss
D37	nc	F6	vcc3p3	G12	vcc1p2ds
E1	nc	F7	vcc3p3	G13	vcc1p2ds
E2	vss	F8	vcc3p3	G14	vssds
E3	nc	F9	vcc3p3	G15	nc
E4	warm_rst#	F10	vcc3p3	G16	nc
E5	vcc3p3	F11	vcc3p3	G17	vssds
E6	hs_freq[0]	F12	vcc1p2ds	G18	vcc1p8s
E7	nmi1#	F13	vssds	G19	vcc1p8s
E8	hs_led_out	F14	vcc1p2ds	G20	nc
E9	xint#[7]	F15	nc	G21	nc
E10	gpio[4]	F16	nc	G22	vcc1p2as
E11	gpio[6]	F17	vssds	G23	vcc1p2as
E12	vssds	F18	vcc1p8s	G24	vcc1p2as
E13	vcc1p2ds	F19	vcc1p8s	G25	vcc3p3
E14	vssds	F20	nc	G26	vcc3p3
E15	rbias[1]	F21	nc	G27	vcc3p3
E16	rbias_sense[1]	F22	vcc1p2as	G28	vcc3p3
E17	vcc1p2ds	F23	vcc1p2as	G29	vcc3p3
E18	vcc1p8s	F24	vcc1p2as	G30	vcc3p3
E19	vcc1p8s	F25	s_act6	G31	vcc3p3
E20	rbias[0]	F26	s_stat4	G32	vcc3p3
E21	rbias_sense[0]	F27	s_stat3	G33	nc
E22	vcc1p2as	F28	nc	G34	nc
E23	vcc1p2as	F29	nc	G35	nc
E24	vcc1p2as	F30	nc	G36	nc
G37	nc	J6	vcc3p3	K12	vss

Table 14. 413808 and 413812 1357-Lead Package - Alphabetical Ball Listings (Sheet 3 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
H1	nc	J7	vss	K13	vcc1p2
H2	nc	J8	vcc1p2	K14	vss
H3	nc	J9	vss	K15	vcc1p2
H4	nc	J10	vcc1p2	K16	vss
H5	vccvio	J11	vss	K17	vcc1p2
H6	vccvio	J12	vcc1p2	K18	vss
H7	vcc1p2	J13	vss	K19	vcc1p2
H8	vss	J14	vcc1p2	K20	vss
H9	vcc1p2	J15	vcc1p2plls1	K21	vcc1p2
H10	vss	J16	vssplls1	K22	vss
H11	vcc1p2	J17	vss	K23	vcc1p2x
H12	vss	J18	vcc1p2	K24	vss
H13	vcc1p2	J19	vss	K25	vcc1p2x
H14	vss	J20	vcc1p2plls0	K26	vss
H15	vss	J21	vssplls0	K27	vcc1p2x
H16	vss	J22	vcc1p2	K28	vss
H17	vcc1p2	J23	vss	K29	vcc1p2x
H18	vss	J24	vcc1p2	K30	vss
H19	vcc1p2	J25	vss	K31	vcc1p2x
H20	s_clkn0	J26	vcc1p2x	K32	vcc1p8
H21	s_clkp0	J27	vss	K33	nc
H22	vss	J28	vcc1p2x	K34	vss
H23	vcc1p2	J29	vss	K35	nc
H24	vss	J30	vcc1p2x	K36	vss
H25	vcc1p2x	J31	vss	K37	nc
H26	vss	J32	vcc1p8	L1	p_cbe#[3]
H27	vcc1p2x	J33	nc	L2	p_ad[25]
H28	vss	J34	vss	L3	p_ad[28]
H29	vcc1p2x	J35	nc	L4	p_ad[30]
H30	vss	J36	vss	L5	vccvio
H31	vcc1p2x	J37	nc	L6	vccvio
H32	vcc1p8	K1	p_ad[29]	L7	vss
H33	nc	K2	vss	L8	vcc1p2
H34	nc	K3	p_ad[27]	L9	vss
H35	nc	K4	vss	L10	vcc1p2
H36	nc	K5	p_ad[31]	L11	vss
H37	nc	K6	vcc3p3	L12	vcc1p2
J1	p_gnt#	K7	vcc1p2	L13	vss
J2	nc	K8	vss	L14	vcc1p2
J3	nc	K9	vcc1p2	L15	vss
J4	nc	K10	vss	L16	vcc1p2
J5	p_req#	K11	vcc1p2	L17	vss
L18	vcc1p2	M24	vss	N30	vcc1p2x

Table 14. 413808 and 413812 1357-Lead Package - Alphabetical Ball Listings (Sheet 4 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
L19	vss	M25	vcc1p2x	N31	vss
L20	vcc1p2	M26	vss	N32	vcc1p8
L21	vss	M27	vcc1p2x	N33	nc
L22	vcc1p2x	M28	vss	N34	vss
L23	vss	M29	vcc1p2x	N35	nc
L24	vcc1p2x	M30	vss	N36	vss
L25	vss	M31	vcc1p2x	N37	nc
L26	vcc1p2x	M32	vcc1p8	P1	p_irdy#
L27	vss	M33	vss	P2	p_cbe#[2]
L28	vcc1p2x	M34	nc	P3	p_ad[18]
L29	vss	M35	nc	P4	p_ad[20]
L30	vcc1p2x	M36	nc	P5	vccvio
L31	vss	M37	nc	P6	vccvio
L32	vcc1p8	N1	p_ad[17]	P7	vcc1p2
L33	nc	N2	vss	P8	vss
L34	nc	N3	p_ad[22]	P9	vcc1p2
L35	nc	N4	vss	P10	vss
L36	nc	N5	p_idsel	P11	vcc1p2pllp
L37	nc	N6	vcc3p3	P12	vss
M1	p_ad[19]	N7	vss	P13	vcc1p2
M2	p_ad[21]	N8	vcc1p2	P14	vss
M3	p_ad[23]	N9	vss	P15	vcc1p2
M4	p_ad[24]	N10	vcc1p2	P16	vss
M5	p_ad[26]	N11	vsspllp	P17	vcc1p2
M6	vccvio	N12	vcc1p2	P18	vss
M7	vcc1p2	N13	vss	P19	vcc1p2
M8	vss	N14	vcc1p2	P20	vss
M9	vcc1p2	N15	vss	P21	vcc1p2
M10	vss	N16	vcc1p2	P22	vss
M11	vcc1p2	N17	vss	P23	vcc1p2x
M12	vss	N18	vcc1p2	P24	vss
M13	vcc1p2	N19	vss	P25	vcc1p2x
M14	vss	N20	vcc1p2	P26	vss
M15	vcc1p2	N21	vss	P27	vcc1p2x
M16	vss	N22	vcc1p2x	P28	vss
M17	vcc1p2	N23	vss	P29	vcc1p2x
M18	vss	N24	vcc1p2x	P30	vss
M19	vcc1p2	N25	vss	P31	vcc1p2x
M20	vss	N26	vcc1p2x	P32	vcc1p8
M21	vcc1p2	N27	vss	P33	nc
M22	vss	N28	vcc1p2x	P34	nc
M23	vcc1p2x	N29	vss	P35	nc
P36	nc	T5	p_trdy#	U11	vss

Table 14. 413808 and 413812 1357-Lead Package - Alphabetical Ball Listings (Sheet 5 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
P37	nc	T6	vcc3p3	U12	vcc1p2
R1	p_perr#	T7	vcc1p2	U13	vss
R2	p_pcixcap	T8	vss	U14	vcc1p2
R3	p_devsel#	T9	vcc1p2	U15	vss
R4	p_frame#	T10	vss	U16	vcc1p2
R5	p_ad[16]	T11	vcc1p2	U17	vss
R6	vcc3p3	T12	vss	U18	vcc1p2
R7	vss	T13	vcc1p2	U19	vss
R8	vcc1p2	T14	vss	U20	vcc1p2
R9	vss	T15	vcc1p2	U21	vss
R10	vcc1p2	T16	vss	U22	vcc1p2x
R11	vss	T17	vcc1p2	U23	vss
R12	vcc1p2	T18	vss	U24	vcc1p2x
R13	vss	T19	vcc1p2	U25	vss
R14	vcc1p2	T20	vss	U26	vcc1p2x
R15	vss	T21	vcc1p2	U27	vss
R16	vcc1p2	T22	vss	U28	vcc1p2x
R17	vss	T23	vcc1p2x	U29	vsspllx
R18	vcc1p2	T24	vss	U30	vcc1p2x
R19	vss	T25	vcc1p2x	U31	vss
R20	vcc1p2	T26	vss	U32	vcc1p8
R21	vss	T27	vcc1p2x	U33	nc
R22	vcc1p2x	T28	vss	U34	nc
R23	vss	T29	vcc1p2x	U35	nc
R24	vcc1p2x	T30	vss	U36	nc
R25	vss	T31	vcc1p2x	U37	nc
R26	vcc1p2x	T32	vcc1p8	V1	p_m66en
R27	vss	T33	nc	V2	p_ad[10]
R28	vcc1p2x	T34	vss	V3	p_ad[12]
R29	vss	T35	nc	V4	p_ad[11]
R30	vcc1p2x	T36	vss	V5	p_ad[13]
R31	vss	T37	nc	V6	vcc3p3
R32	vcc1p8	U1	p_ad[14]	V7	vcc1p2
R33	nc	U2	p_cbe#[1]	V8	vss
R34	nc	U3	p_ad[15]	V9	vcc1p2
R35	nc	U4	p_par	V10	vss
R36	nc	U5	vccvio	V11	vcc1p2
R37	nc	U6	vccvio	V12	vss
T1	p_serr#	U7	vss	V13	vcc1p2
T2	vss	U8	vcc1p2	V14	vss
T3	p_stop#	U9	vss	V15	vcc1p2
T4	vss	U10	vcc1p2	V16	vss
V17	vcc1p2	W23	vss	Y29	vcc3p3pllx

Table 14. 413808 and 413812 1357-Lead Package - Alphabetical Ball Listings (Sheet 6 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
V18	vss	W24	vcc1p2x	Y30	vss
V19	vcc1p2	W25	vss	Y31	vcc1p2x
V20	vss	W26	vcc1p2x	Y32	vcc1p8
V21	vcc1p2	W27	vss	Y33	nc
V22	vss	W28	vcc1p2x	Y34	nc
V23	vcc1p2x	W29	nc	Y35	vss
V24	vss	W30	vcc1p2x	Y36	nc
V25	vcc1p2x	W31	vss	Y37	nc
V26	vss	W32	vcc1p8	AA1	p_ad[3]
V27	vcc1p2x	W33	vss	AA2	p_ad[1]
V28	thermdc	W34	nc	AA3	p_ad[2]
V29	thermda	W35	nc	AA4	p_ad[0]
V30	vss	W36	nc	AA5	vccvio
V31	vcc1p2x	W37	nc	AA6	vccvio
V32	vcc1p8	Y1	p_ad[8]	AA7	vss
V33	nc	Y2	p_ad[7]	AA8	vcc1p2
V34	nc	Y3	p_ad[5]	AA9	vss
V35	vss	Y4	p_ad[6]	AA10	vcc1p2
V36	nc	Y5	p_ad[4]	AA11	vss
V37	nc	Y6	vccvio	AA12	vcc1p2
W1	vss	Y7	vcc1p2	AA13	vss
W2	vss	Y8	vss	AA14	vcc1p2
W3	p_cbe#[0]	Y9	vcc1p2	AA15	vss
W4	vss	Y10	vss	AA16	vcc1p2
W5	p_ad[9]	Y11	vcc1p2	AA17	vss
W6	vcc3p3	Y12	vss	AA18	vcc1p2
W7	vss	Y13	vcc1p2	AA19	vss
W8	vcc1p2	Y14	vss	AA20	vcc1p2
W9	vss	Y15	vcc1p2	AA21	vss
W10	vcc1p2	Y16	vss	AA22	vcc1p2x
W11	vss	Y17	vcc1p2	AA23	vss
W12	vcc1p2	Y18	vss	AA24	vcc1p2x
W13	vss	Y19	vcc1p2	AA25	vss
W14	vcc1p2	Y20	vss	AA26	vcc1p2x
W15	vss	Y21	vcc1p2	AA27	vss
W16	vcc1p2	Y22	vss	AA28	vcc1p2x
W17	vss	Y23	vcc1p2x	AA29	vss
W18	vcc1p2	Y24	vss	AA30	vcc1p2x
W19	vss	Y25	vcc1p2x	AA31	vss
W20	vcc1p2	Y26	vss	AA32	vcc1p8
W21	vss	Y27	vcc1p2x	AA33	nc
W22	vcc1p2x	Y28	vss	AA34	nc
AA35	nc	AC4	p_cbe#[5]	AD10	vss

Table 14. 413808 and 413812 1357-Lead Package - Alphabetical Ball Listings (Sheet 7 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
AA36	nc	AC5	p_par64	AD11	vcc1p2
AA37	nc	AC6	vccvio	AD12	vss
AB1	p_ack64#	AC7	vss	AD13	vcc1p2
AB2	vss	AC8	vcc1p2	AD14	vss
AB3	p_req64#	AC9	vss	AD15	vcc1p2
AB4	vss	AC10	vcc1p2	AD16	vss
AB5	p_cbe#[7]	AC11	vss	AD17	vcc1p2
AB6	vcc3p3	AC12	vcc1p2	AD18	vss
AB7	vcc1p2	AC13	vss	AD19	vcc1p2
AB8	vss	AC14	vcc1p2	AD20	vss
AB9	vcc1p2	AC15	vss	AD21	vcc1p2
AB10	vss	AC16	vcc1p2	AD22	vss
AB11	vcc1p2	AC17	vss	AD23	vcc1p2x
AB12	vss	AC18	vcc1p2	AD24	vss
AB13	vcc1p2	AC19	vss	AD25	vcc1p2x
AB14	vss	AC20	vcc1p2	AD26	vss
AB15	vcc1p2	AC21	vss	AD27	vcc1p2x
AB16	vss	AC22	vcc1p2x	AD28	vss
AB17	vcc1p2	AC23	vss	AD29	vcc1p2plld
AB18	vss	AC24	vcc1p2x	AD30	vss
AB19	vcc1p2	AC25	vss	AD31	vcc1p2x
AB20	vss	AC26	vcc1p2x	AD32	vcc1p8
AB21	vcc1p2	AC27	vss	AD33	vss
AB22	vss	AC28	vcc1p2x	AD34	nc
AB23	vcc1p2x	AC29	vssplld	AD35	nc
AB24	vss	AC30	vcc1p2x	AD36	nc
AB25	vcc1p2x	AC31	vss	AD37	nc
AB26	vss	AC32	vcc1p8	AE1	p_ad[57]
AB27	vcc1p2x	AC33	nc	AE2	vss
AB28	vss	AC34	nc	AE3	p_ad[58]
AB29	vcc1p2x	AC35	nc	AE4	vss
AB30	vss	AC36	nc	AE5	p_ad[56]
AB31	vcc1p2x	AC37	nc	AE6	vcc3p3
AB32	vcc1p8	AD1	p_ad[61]	AE7	vss
AB33	nc	AD2	p_ad[59]	AE8	vcc1p2
AB34	vss	AD3	p_ad[62]	AE9	vss
AB35	nc	AD4	p_ad[60]	AE10	vcc1p2
AB36	vss	AD5	vccvio	AE11	vss
AB37	nc	AD6	vccvio	AE12	vcc1p2
AC1	p_cbe#[6]	AD7	vcc1p2	AE13	vss
AC2	p_cbe#[4]	AD8	vss	AE14	vcc1p2
AC3	p_ad[63]	AD9	vcc1p2	AE15	vss
AE16	vcc1p2	AF22	vss	AG28	vcc1p2x

Table 14. 413808 and 413812 1357-Lead Package - Alphabetical Ball Listings (Sheet 8 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
AE17	vss	AF23	vcc1p2x	AG29	vss
AE18	vcc1p2	AF24	vss	AG30	vcc1p2x
AE19	vss	AF25	vcc1p2x	AG31	vss
AE20	vcc1p2	AF26	vss	AG32	vcc1p8
AE21	vss	AF27	vcc1p2x	AG33	nc
AE22	vcc1p2x	AF28	vss	AG34	nc
AE23	vss	AF29	vcc1p2x	AG35	nc
AE24	vcc1p2x	AF30	vss	AG36	nc
AE25	vss	AF31	vcc1p2x	AG37	nc
AE26	vcc1p2x	AF32	vcc1p8	AH1	p_ad[45]
AE27	vss	AF33	nc	AH2	vss
AE28	vcc1p2x	AF34	nc	AH3	p_ad[46]
AE29	vss	AF35	nc	AH4	vss
AE30	vcc1p2x	AF36	nc	AH5	p_ad[44]
AE31	vss	AF37	nc	AH6	vcc3p3
AE32	vcc1p8	AG1	p_ad[49]	AH7	vcc1p2
AE33	nc	AG2	p_ad[47]	AH8	vss
AE34	vss	AG3	p_ad[50]	AH9	vcc1p2
AE35	nc	AG4	p_ad[48]	AH10	vss
AE36	vss	AG5	vccvio	AH11	vcc1p2
AE37	nc	AG6	vccvio	AH12	vss
AF1	p_ad[55]	AG7	vss	AH13	vcc1p2
AF2	p_ad[53]	AG8	vcc1p2	AH14	vss
AF3	p_ad[51]	AG9	vss	AH15	vcc1p2
AF4	p_ad[54]	AG10	vcc1p2	AH16	vss
AF5	p_ad[52]	AG11	vss	AH17	vcc1p2
AF6	vccvio	AG12	vcc1p2	AH18	vss
AF7	vcc1p2	AG13	vss	AH19	vcc1p2
AF8	vss	AG14	vcc1p2	AH20	vss
AF9	vcc1p2	AG15	vss	AH21	vcc1p2
AF10	vss	AG16	vcc1p2	AH22	vss
AF11	vcc1p2	AG17	vss	AH23	vcc1p2x
AF12	vss	AG18	vcc1p2	AH24	vss
AF13	vcc1p2	AG19	vss	AH25	vcc1p2x
AF14	vss	AG20	vcc1p2	AH26	vss
AF15	vcc1p2	AG21	vss	AH27	vcc1p2x
AF16	vss	AG22	vcc1p2x	AH28	vss
AF17	vcc1p2	AG23	vss	AH29	vcc1p2x
AF18	vss	AG24	vcc1p2x	AH30	vss
AF19	vcc1p2	AG25	vss	AH31	vcc1p2x
AF20	vss	AG26	vcc1p2x	AH32	vcc1p8
AF21	vcc1p2	AG27	vss	AH33	nc
AH34	vss	AK3	p_ad[38]	AL9	vss

Table 14. 413808 and 413812 1357-Lead Package - Alphabetical Ball Listings (Sheet 9 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
AH35	nc	AK4	p_ad[36]	AL10	vcc1p2
AH36	vss	AK5	vccvio	AL11	vss
AH37	nc	AK6	vccvio	AL12	vcc1p2
AJ1	p_ad[43]	AK7	vcc1p2	AL13	vss
AJ2	p_ad[41]	AK8	vss	AL14	vcc1p2
AJ3	p_ad[39]	AK9	vcc1p2	AL15	vss
AJ4	p_ad[42]	AK10	vss	AL16	vcc1p2
AJ5	p_ad[40]	AK11	vcc1p2	AL17	vss
AJ6	vccvio	AK12	vss	AL18	vcc1p2
AJ7	vss	AK13	vcc1p2	AL19	nc
AJ8	vcc1p2	AK14	vss	AL20	nc
AJ9	vss	AK15	vcc1p2	AL21	vss
AJ10	vcc1p2	AK16	vss	AL22	vcc1p2
AJ11	vss	AK17	vcc1p2	AL23	vss
AJ12	vcc1p2	AK18	vss	AL24	vcc1p2x
AJ13	vss	AK19	refclkn	AL25	vss
AJ14	vcc1p2	AK20	refclkp	AL26	vcc1p2x
AJ15	vss	AK21	vcc1p2	AL27	vcc1p2x
AJ16	vcc1p2	AK22	vss	AL28	vcc1p2x
AJ17	vss	AK23	vcc1p2	AL29	vss
AJ18	vcc1p2	AK24	vss	AL30	vcc1p2x
AJ19	vss	AK25	vcc1p2x	AL31	vss
AJ20	vcc1p2	AK26	vss	AL32	vcc1p8
AJ21	vss	AK27	vcc1p2x	AL33	vss
AJ22	vcc1p2	AK28	vss	AL34	nc
AJ23	vss	AK29	vcc1p2x	AL35	nc
AJ24	vcc1p2x	AK30	vss	AL36	nc
AJ25	vss	AK31	vcc1p2x	AL37	nc
AJ26	vcc1p2x	AK32	vcc1p8	AM1	a[24]
AJ27	vcc1p2x	AK33	nc	AM2	d[14]
AJ28	vcc1p2x	AK34	nc	AM3	pwe#
AJ29	vss	AK35	nc	AM4	poe#
AJ30	vcc1p2x	AK36	nc	AM5	d[10]
AJ31	vss	AK37	nc	AM6	vcc3p3
AJ32	vcc1p8	AL1	p_ad[33]	AM7	vcc3p3
AJ33	nc	AL2	vss	AM8	vcc3p3
AJ34	vss	AL3	p_ad[34]	AM9	vcc3p3
AJ35	nc	AL4	vss	AM10	vcc3p3
AJ36	vss	AL5	p_ad[32]	AM11	vcc3p3
AJ37	nc	AL6	vcc3p3	AM12	vcc1p2
AK1	p_ad[37]	AL7	vss	AM13	vcc1p2e
AK2	p_ad[35]	AL8	vcc1p2	AM14	vcc1p2e
AM15	vcc1p2ae	AN21	vcc1p8e	AP27	vcc1p2x

Table 14. 413808 and 413812 1357-Lead Package - Alphabetical Ball Listings (Sheet 10 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
AM16	vcc1p2ae	AN22	vcc1p8e	AP28	vss
AM17	vcc1p2ae	AN23	vcc1p8e	AP29	sda2
AM18	vcc1p2ae	AN24	vcc1p8e	AP30	vcc3p3
AM19	nc	AN25	vcc1p8e	AP31	vss
AM20	nc	AN26	vcc1p8e	AP32	vcc1p8
AM21	vcc1p2ae	AN27	vcc1p2x	AP33	nc
AM22	vcc1p2ae	AN28	scl2	AP34	nc
AM23	vcc1p2ae	AN29	scl1	AP35	nc
AM24	vcc1p2ae	AN30	vcc3p3	AP36	nc
AM25	vcc1p8e	AN31	vcc3p3	AP37	nc
AM26	vcc1p8e	AN32	vcc1p8	AR1	vss
AM27	vcc1p2x	AN33	nc	AR2	a[0]
AM28	vcc3p3	AN34	nc	AR3	a[23]
AM29	vcc3p3	AN35	nc	AR4	d[3]
AM30	vcc3p3	AN36	nc	AR5	d[4]
AM31	vcc3p3	AN37	nc	AR6	a[17]
AM32	vcc1p8	AP1	d[13]	AR7	a[15]
AM33	nc	AP2	d[5]	AR8	pb_rstout#
AM34	vss	AP3	d[11]	AR9	a[12]
AM35	nc	AP4	vss	AR10	pce#[0]
AM36	vss	AP5	d[9]	AR11	a[19]
AM37	nc	AP6	a[16]	AR12	vcc1p2
AN1	d[7]	AP7	vss	AR13	vsse
AN2	d[6]	AP8	a[10]	AR14	petp[0]
AN3	d[12]	AP9	a[9]	AR15	petp[1]
AN4	d[2]	AP10	vss	AR16	vsse
AN5	vcc3p3	AP11	a[21]	AR17	petp[2]
AN6	d[15]	AP12	vcc1p2	AR18	petp[3]
AN7	a[11]	AP13	vsse	AR19	vsse
AN8	PUR1	AP14	petn[0]	AR20	petp[4]
AN9	nc	AP15	petn[1]	AR21	petp[5]
AN10	a[20]	AP16	vsse	AR22	vsse
AN11	pce#[1]	AP17	petn[2]	AR23	petp[6]
AN12	vcc1p2	AP18	petn[3]	AR24	petp[7]
AN13	vcc1p2e	AP19	vsse	AR25	vsse
AN14	vcc1p2e	AP20	petn[4]	AR26	vcc1p8e
AN15	vcc1p2e	AP21	petn[5]	AR27	vcc1p2x
AN16	vcc1p2e	AP22	vsse	AR28	sda0
AN17	vcc1p8e	AP23	petn[6]	AR29	sda1
AN18	vcc1p8e	AP24	petn[7]	AR30	tdo
AN19	pe_caln	AP25	vsse	AR31	tck
AN20	pe_calp	AP26	vcc1p8e	AR32	vcc1p8
AR33	nc	AT23	pern[6]	AU12	vcc1p2

Table 14. 413808 and 413812 1357-Lead Package - Alphabetical Ball Listings (Sheet 11 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
AR34	vss	AT24	pern[7]	AU13	vsse
AR35	nc	AT25	vsse	AU14	perp[0]
AR36	nc	AT26	vcc1p8e	AU15	perp[1]
AR37	vss	AT27	vcc1p2x	AU16	vsse
AT1	-	AT28	vss	AU17	perp[2]
AT2	vss	AT29	scl0	AU18	perp[3]
AT3	d[0]	AT30	tms	AU19	vsse
AT4	d[8]	AT31	vss	AU20	perp[4]
AT5	a[4]	AT32	vcc1p8	AU21	perp[5]
AT6	a[3]	AT33	vss	AU22	vsse
AT7	vss	AT34	nc	AU23	perp[6]
AT8	a[1]	AT35	nc	AU24	perp[7]
AT9	a[8]	AT36	vss	AU25	vsse
AT10	vss	AT37	-	AU26	vcc1p8e
AT11	a[18]	AU1	-	AU27	vcc1p2x
AT12	vcc1p2	AU2	-	AU28	smbdat
AT13	vsse	AU3	vss	AU29	smbclk
AT14	pern[0]	AU4	d[1]	AU30	tdi
AT15	pern[1]	AU5	a[5]	AU31	trst#
AT16	vsse	AU6	a[7]	AU32	vcc1p8
AT17	pern[2]	AU7	a[2]	AU33	vss
AT18	pern[3]	AU8	a[6]	AU34	vss
AT19	vsse	AU9	a[14]	AU35	vss
AT20	pern[4]	AU10	a[13]	AU36	-
AT21	pern[5]	AU11	a[22]	AU37	-
AT22	vsse				

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Table 15. 413808 and 413812 1357-Lead Package - Alphabetical Signal Listings (Sheet 1 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
-	A1	d[6]	AN2	nc	C30
-	A2	d[7]	AN1	nc	C31
-	A36	d[8]	AT4	nc	C32
-	A37	d[9]	AP5	nc	C33
-	B1	d[10]	AM5	nc	C35
-	B37	d[11]	AP3	nc	C36
-	AT1	d[12]	AN3	nc	D2
-	AT37	d[13]	AP1	nc	D5
-	AU1	d[14]	AM2	nc	D28
-	AU2	d[15]	AN6	nc	D29
-	AU36	gpio[0]	A10	nc	D31
-	AU37	gpio[1]	A11	nc	D32
a[0]	AR2	gpio[2]	C10	nc	D33
a[1]	AT8	gpio[3]	B11	nc	D34
a[2]	AU7	gpio[4]	E10	nc	D35
a[3]	AT6	gpio[5]	D11	nc	D36
a[4]	AT5	gpio[6]	E11	nc	D37
a[5]	AU5	gpio[7]	C11	nc	E1
a[6]	AU8	hpi#	C7	nc	E3
a[7]	AU6	hs_enum#	A7	nc	E28
a[8]	AT9	hs_freq[0]	E6	nc	E29
a[9]	AP9	hs_freq[1]	D6	nc	E30
a[10]	AP8	hs_led_out	E8	nc	E31
a[11]	AN7	hs_lstat	C6	nc	E32
a[12]	AR9	nc	A28	nc	E34
a[13]	AU10	nc	A29	nc	E35
a[14]	AU9	nc	A30	nc	E36
a[15]	AR7	nc	A31	nc	E37
a[16]	AP6	nc	A32	nc	F15
a[17]	AR6	nc	A33	nc	F16
a[18]	AT11	nc	A34	nc	F20
a[19]	AR11	nc	B3	nc	F21
a[20]	AN10	nc	B28	nc	F28
a[21]	AP11	nc	B29	nc	F29
a[22]	AU11	nc	B31	nc	F30
a[23]	AR3	nc	B32	nc	F31
a[24]	AM1	nc	B33	nc	F33
d[0]	AT3	nc	B34	nc	F35
d[1]	AU4	nc	B35	nc	F37
d[2]	AN4	nc	C2	nc	G1
d[3]	AR4	nc	C3	nc	G3
d[4]	AR5	nc	C28	nc	G5
d[5]	AP2	nc	C29	nc	G15

Table 15. 413808 and 413812 1357-Lead Package - Alphabetical Signal Listings (Sheet 2 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
nc	G16	nc	R33	nc	AE33
nc	G20	nc	R34	nc	AE35
nc	G21	nc	R35	nc	AE37
nc	G33	nc	R36	nc	AF33
nc	G34	nc	R37	nc	AF34
nc	G35	nc	T33	nc	AF35
nc	G36	nc	T35	nc	AF36
nc	G37	nc	T37	nc	AF37
nc	H1	nc	U33	nc	AG33
nc	H2	nc	U34	nc	AG34
nc	H3	nc	U35	nc	AG35
nc	H4	nc	U36	nc	AG36
nc	H33	nc	U37	nc	AG37
nc	H34	nc	V33	nc	AH33
nc	H35	nc	V34	nc	AH35
nc	H36	nc	V36	nc	AH37
nc	H37	nc	V37	nc	AJ33
nc	J2	nc	W29	nc	AJ35
nc	J3	nc	W34	nc	AJ37
nc	J4	nc	W35	nc	AK33
nc	J33	nc	W36	nc	AK34
nc	J35	nc	W37	nc	AK35
nc	J37	nc	Y33	nc	AK36
nc	K33	nc	Y34	nc	AK37
nc	K35	nc	Y36	nc	AL19
nc	K37	nc	Y37	nc	AL20
nc	L33	nc	AA33	nc	AL34
nc	L34	nc	AA34	nc	AL35
nc	L35	nc	AA35	nc	AL36
nc	L36	nc	AA36	nc	AL37
nc	L37	nc	AA37	nc	AM19
nc	M34	nc	AB33	nc	AM20
nc	M35	nc	AB35	nc	AM33
nc	M36	nc	AB37	nc	AM35
nc	M37	nc	AC33	nc	AM37
nc	N33	nc	AC34	nc	AN9
nc	N35	nc	AC35	nc	AN33
nc	N37	nc	AC36	nc	AN34
nc	P33	nc	AC37	nc	AN35
nc	P34	nc	AD34	nc	AN36
nc	P35	nc	AD35	nc	AN37
nc	P36	nc	AD36	nc	AP33
nc	P37	nc	AD37	nc	AP34

Table 15. 413808 and 413812 1357-Lead Package - Alphabetical Signal Listings (Sheet 3 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
nc	AP35	p_ad[31]	K5	p_cbe#[6]	AC1
nc	AP36	p_ad[32]	AL5	p_cbe#[7]	AB5
nc	AP37	p_ad[33]	AL1	p_clkin	D1
nc	AR33	p_ad[34]	AL3	p_devsel#	R3
nc	AR35	p_ad[35]	AK2	p_frame#	R4
nc	AR36	p_ad[36]	AK4	p_gnt#	J1
-	-	p_ad[37]	AK1	p_idsel	N5
nc	AT34	p_ad[38]	AK3	p_irdy#	P1
nc	AT35	p_ad[39]	AJ3	p_m66en	V1
nmi0#	D8	p_ad[40]	AJ5	p_par	U4
nmi1#	E7	p_ad[41]	AJ2	p_par64	AC5
p_ack64#	AB1	p_ad[42]	AJ4	p_pcixcap	R2
p_ad[0]	AA4	p_ad[43]	AJ1	p_perr#	R1
p_ad[1]	AA2	p_ad[44]	AH5	p_req#	J5
p_ad[2]	AA3	p_ad[45]	AH1	p_req64#	AB3
p_ad[3]	AA1	p_ad[46]	AH3	p_rst#	F2
p_ad[4]	Y5	p_ad[47]	AG2	p_rstout#	F1
p_ad[5]	Y3	p_ad[48]	AG4	p_serr#	T1
p_ad[6]	Y4	p_ad[49]	AG1	p_stop#	T3
p_ad[7]	Y2	p_ad[50]	AG3	p_trdy#	T5
p_ad[8]	Y1	p_ad[51]	AF3	pb_rstout#	AR8
p_ad[9]	W5	p_ad[52]	AF5	pce#[0]	AR10
p_ad[10]	V2	p_ad[53]	AF2	pce#[1]	AN11
p_ad[11]	V4	p_ad[54]	AF4	pe_caln	AN19
p_ad[12]	V3	p_ad[55]	AF1	pe_calp	AN20
p_ad[13]	V5	p_ad[56]	AE5	pern[0]	AT14
p_ad[14]	U1	p_ad[57]	AE1	pern[1]	AT15
p_ad[15]	U3	p_ad[58]	AE3	pern[2]	AT17
p_ad[16]	R5	p_ad[59]	AD2	pern[3]	AT18
p_ad[17]	N1	p_ad[60]	AD4	pern[4]	AT20
p_ad[18]	P3	p_ad[61]	AD1	pern[5]	AT21
p_ad[19]	M1	p_ad[62]	AD3	pern[6]	AT23
p_ad[20]	P4	p_ad[63]	AC3	pern[7]	AT24
p_ad[21]	M2	p_bmi	F4	perp[0]	AU14
p_ad[22]	N3	p_cal[0]	F5	perp[1]	AU15
p_ad[23]	M3	p_cal[1]	F3	perp[2]	AU17
p_ad[24]	M4	p_cal[2]	D3	perp[3]	AU18
p_ad[25]	L2	p_cbe#[0]	W3	perp[4]	AU20
p_ad[26]	M5	p_cbe#[1]	U2	perp[5]	AU21
p_ad[27]	K3	p_cbe#[2]	P2	perp[6]	AU23
p_ad[28]	L3	p_cbe#[3]	L1	perp[7]	AU24
p_ad[29]	K1	p_cbe#[4]	AC2	petn[0]	AP14
p_ad[30]	L4	p_cbe#[5]	AC4	petn[1]	AP15

Table 15. 413808 and 413812 1357-Lead Package - Alphabetical Signal Listings (Sheet 4 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
petn[2]	AP17	s_rxp[2]	A19	tms	AT30
petn[3]	AP18	s_rxp[3]	A23	trst#	AU31
petn[4]	AP20	s_rxp[4]	A14	u0_cts#	A5
petn[5]	AP21	s_rxp[5]	A16	u0_rts#	A6
petn[6]	AP23	s_rxp[6]	A13	u0_rxd	B6
petn[7]	AP24	s_rxp[7]	A17	u0_txd	B5
petp[0]	AR14	s_stat0	A25	u1_cts#	A4
petp[1]	AR15	s_stat1	E25	u1_rts#	C4
petp[2]	AR17	s_stat2	B26	u1_rxd	C5
petp[3]	AR18	s_stat3	F27	u1_txd	B4
petp[4]	AR20	s_stat4	F26	vcc1p2	G8
petp[5]	AR21	s_stat5	C27	vcc1p2	G10
petp[6]	AR23	s_stat6	E26	vcc1p2	H7
petp[7]	AR24	s_stat7	D26	vcc1p2	H9
poe#	AM4	s_txn[0]	D20	vcc1p2	H11
PUR1	AN8	s_txn[1]	D22	vcc1p2	H13
pwe#	AM3	s_txn[2]	D19	vcc1p2	H17
rbias[0]	E20	s_txn[3]	D23	vcc1p2	H19
rbias[1]	E15	s_txn[4]	D14	vcc1p2	H23
rbias_sense[0]	E21	s_txn[5]	D16	vcc1p2	J8
rbias_sense[1]	E16	s_txn[6]	D13	vcc1p2	J10
refclkn	AK19	s_txn[7]	D17	vcc1p2	J12
refclkp	AK20	s_txp[0]	C20	vcc1p2	J14
s_act0	C26	s_txp[1]	C22	vcc1p2	J18
s_act1	A27	s_txp[2]	C19	vcc1p2	J22
s_act2	B25	s_txp[3]	C23	vcc1p2	J24
s_act3	C25	s_txp[4]	C14	vcc1p2	K7
s_act4	E27	s_txp[5]	C16	vcc1p2	K9
s_act5	A26	s_txp[6]	C13	vcc1p2	K11
s_act6	F25	s_txp[7]	C17	vcc1p2	K13
s_act7	D25	scl0	AT29	vcc1p2	K15
s_clkn0	H20	scl1	AN29	vcc1p2	K17
s_clkp0	H21	scl2	AN28	vcc1p2	K19
s_rxn[0]	B20	sda0	AR28	vcc1p2	K21
s_rxn[1]	B22	sda1	AR29	vcc1p2	L8
s_rxn[2]	B19	sda2	AP29	vcc1p2	L10
s_rxn[3]	B23	smbclk	AU29	vcc1p2	L12
s_rxn[4]	B14	smbdat	AU28	vcc1p2	L14
s_rxn[5]	B16	tck	AR31	vcc1p2	L16
s_rxn[6]	B13	tdi	AU30	vcc1p2	L18
s_rxn[7]	B17	tdo	AR30	vcc1p2	L20
s_rxp[0]	A20	thermda	V29	vcc1p2	M7
s_rxp[1]	A22	thermdc	V28	vcc1p2	M9

Table 15. 413808 and 413812 1357-Lead Package - Alphabetical Signal Listings (Sheet 5 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
vcc1p2	M11	vcc1p2	V9	vcc1p2	AC20
vcc1p2	M13	vcc1p2	V11	vcc1p2	AD7
vcc1p2	M15	vcc1p2	V13	vcc1p2	AD9
vcc1p2	M17	vcc1p2	V15	vcc1p2	AD11
vcc1p2	M19	vcc1p2	V17	vcc1p2	AD13
vcc1p2	M21	vcc1p2	V19	vcc1p2	AD15
vcc1p2	N8	vcc1p2	V21	vcc1p2	AD17
vcc1p2	N10	vcc1p2	W8	vcc1p2	AD19
vcc1p2	N12	vcc1p2	W10	vcc1p2	AD21
vcc1p2	N14	vcc1p2	W12	vcc1p2	AE8
vcc1p2	N16	vcc1p2	W14	vcc1p2	AE10
vcc1p2	N18	vcc1p2	W16	vcc1p2	AE12
vcc1p2	N20	vcc1p2	W18	vcc1p2	AE14
vcc1p2	P7	vcc1p2	W20	vcc1p2	AE16
vcc1p2	P9	vcc1p2	Y7	vcc1p2	AE18
vcc1p2	P13	vcc1p2	Y9	vcc1p2	AE20
vcc1p2	P15	vcc1p2	Y11	vcc1p2	AF7
vcc1p2	P17	vcc1p2	Y13	vcc1p2	AF9
vcc1p2	P19	vcc1p2	Y15	vcc1p2	AF11
vcc1p2	P21	vcc1p2	Y17	vcc1p2	AF13
vcc1p2	R8	vcc1p2	Y19	vcc1p2	AF15
vcc1p2	R10	vcc1p2	Y21	vcc1p2	AF17
vcc1p2	R12	vcc1p2	AA8	vcc1p2	AF19
vcc1p2	R14	vcc1p2	AA10	vcc1p2	AF21
vcc1p2	R16	vcc1p2	AA12	vcc1p2	AG8
vcc1p2	R18	vcc1p2	AA14	vcc1p2	AG10
vcc1p2	R20	vcc1p2	AA16	vcc1p2	AG12
vcc1p2	T7	vcc1p2	AA18	vcc1p2	AG14
vcc1p2	T9	vcc1p2	AA20	vcc1p2	AG16
vcc1p2	T11	vcc1p2	AB7	vcc1p2	AG18
vcc1p2	T13	vcc1p2	AB9	vcc1p2	AG20
vcc1p2	T15	vcc1p2	AB11	vcc1p2	AH7
vcc1p2	T17	vcc1p2	AB13	vcc1p2	AH9
vcc1p2	T19	vcc1p2	AB15	vcc1p2	AH11
vcc1p2	T21	vcc1p2	AB17	vcc1p2	AH13
vcc1p2	U8	vcc1p2	AB19	vcc1p2	AH15
vcc1p2	U10	vcc1p2	AB21	vcc1p2	AH17
vcc1p2	U12	vcc1p2	AC8	vcc1p2	AH19
vcc1p2	U14	vcc1p2	AC10	vcc1p2	AH21
vcc1p2	U16	vcc1p2	AC12	vcc1p2	AJ8
vcc1p2	U18	vcc1p2	AC14	vcc1p2	AJ10
vcc1p2	U20	vcc1p2	AC16	vcc1p2	AJ12
vcc1p2	V7	vcc1p2	AC18	vcc1p2	AJ14

Table 15. 413808 and 413812 1357-Lead Package - Alphabetical Signal Listings (Sheet 6 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
vcc1p2	AJ16	vcc1p2ds	E17	vcc1p2x	P25
vcc1p2	AJ18	vcc1p2ds	F12	vcc1p2x	P27
vcc1p2	AJ20	vcc1p2ds	F14	vcc1p2x	P29
vcc1p2	AJ22	vcc1p2ds	G12	vcc1p2x	P31
vcc1p2	AK7	vcc1p2ds	G13	vcc1p2x	R22
vcc1p2	AK9	vcc1p2e	AM13	vcc1p2x	R24
vcc1p2	AK11	vcc1p2e	AM14	vcc1p2x	R26
vcc1p2	AK13	vcc1p2e	AN13	vcc1p2x	R28
vcc1p2	AK15	vcc1p2e	AN14	vcc1p2x	R30
vcc1p2	AK17	vcc1p2e	AN15	vcc1p2x	T23
vcc1p2	AK21	vcc1p2e	AN16	vcc1p2x	T25
vcc1p2	AK23	vcc1p2plld	AD29	vcc1p2x	T27
vcc1p2	AL8	vcc1p2pllp	P11	vcc1p2x	T29
vcc1p2	AL10	vcc1p2plls0	J20	vcc1p2x	T31
vcc1p2	AL12	vcc1p2plls1	J15	vcc1p2x	U22
vcc1p2	AL14	vcc1p2x	H25	vcc1p2x	U24
vcc1p2	AL16	vcc1p2x	H27	vcc1p2x	U26
vcc1p2	AL18	vcc1p2x	H29	vcc1p2x	U28
vcc1p2	AL22	vcc1p2x	H31	vcc1p2x	U30
vcc1p2	AM12	vcc1p2x	J26	vcc1p2x	V23
vcc1p2	AN12	vcc1p2x	J28	vcc1p2x	V25
vcc1p2	AP12	vcc1p2x	J30	vcc1p2x	V27
vcc1p2	AR12	vcc1p2x	K23	vcc1p2x	V31
vcc1p2	AT12	vcc1p2x	K25	vcc1p2x	W22
vcc1p2	AU12	vcc1p2x	K27	vcc1p2x	W24
vcc1p2ae	AM15	vcc1p2x	K29	vcc1p2x	W26
vcc1p2ae	AM16	vcc1p2x	K31	vcc1p2x	W28
vcc1p2ae	AM17	vcc1p2x	L22	vcc1p2x	W30
vcc1p2ae	AM18	vcc1p2x	L24	vcc1p2x	Y23
vcc1p2ae	AM21	vcc1p2x	L26	vcc1p2x	Y25
vcc1p2ae	AM22	vcc1p2x	L28	vcc1p2x	Y27
vcc1p2ae	AM23	vcc1p2x	L30	vcc1p2x	Y31
vcc1p2ae	AM24	vcc1p2x	M23	vcc1p2x	AA22
vcc1p2as	E22	vcc1p2x	M25	vcc1p2x	AA24
vcc1p2as	E23	vcc1p2x	M27	vcc1p2x	AA26
vcc1p2as	E24	vcc1p2x	M29	vcc1p2x	AA28
vcc1p2as	F22	vcc1p2x	M31	vcc1p2x	AA30
vcc1p2as	F23	vcc1p2x	N22	vcc1p2x	AB23
vcc1p2as	F24	vcc1p2x	N24	vcc1p2x	AB25
vcc1p2as	G22	vcc1p2x	N26	vcc1p2x	AB27
vcc1p2as	G23	vcc1p2x	N28	vcc1p2x	AB29
vcc1p2as	G24	vcc1p2x	N30	vcc1p2x	AB31
vcc1p2ds	E13	vcc1p2x	P23	vcc1p2x	AC22

Table 15. 413808 and 413812 1357-Lead Package - Alphabetical Signal Listings (Sheet 7 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
vcc1p2x	AC24	vcc1p2x	AN27	vcc1p8e	AN25
vcc1p2x	AC26	vcc1p2x	AP27	vcc1p8e	AN26
vcc1p2x	AC28	vcc1p2x	AR27	vcc1p8e	AP26
vcc1p2x	AC30	vcc1p2x	AT27	vcc1p8e	AR26
vcc1p2x	AD23	vcc1p2x	AU27	vcc1p8e	AT26
vcc1p2x	AD25	vcc1p8	H32	vcc1p8e	AU26
vcc1p2x	AD27	vcc1p8	J32	vcc1p8s	E18
vcc1p2x	AD31	vcc1p8	K32	vcc1p8s	E19
vcc1p2x	AE22	vcc1p8	L32	vcc1p8s	F18
vcc1p2x	AE24	vcc1p8	M32	vcc1p8s	F19
vcc1p2x	AE26	vcc1p8	N32	vcc1p8s	G18
vcc1p2x	AE28	vcc1p8	P32	vcc1p8s	G19
vcc1p2x	AE30	vcc1p8	R32	vcc3p3	E5
vcc1p2x	AF23	vcc1p8	T32	vcc3p3	F6
vcc1p2x	AF25	vcc1p8	U32	vcc3p3	F7
vcc1p2x	AF27	vcc1p8	V32	vcc3p3	F8
vcc1p2x	AF29	vcc1p8	W32	vcc3p3	F9
vcc1p2x	AF31	vcc1p8	Y32	vcc3p3	F10
vcc1p2x	AG22	vcc1p8	AA32	vcc3p3	F11
vcc1p2x	AG24	vcc1p8	AB32	vcc3p3	F32
vcc1p2x	AG26	vcc1p8	AC32	vcc3p3	G6
vcc1p2x	AG28	vcc1p8	AD32	vcc3p3	G25
vcc1p2x	AG30	vcc1p8	AE32	vcc3p3	G26
vcc1p2x	AH23	vcc1p8	AF32	vcc3p3	G27
vcc1p2x	AH25	vcc1p8	AG32	vcc3p3	G28
vcc1p2x	AH27	vcc1p8	AH32	vcc3p3	G29
vcc1p2x	AH29	vcc1p8	AJ32	vcc3p3	G30
vcc1p2x	AH31	vcc1p8	AK32	vcc3p3	G31
vcc1p2x	AJ24	vcc1p8	AL32	vcc3p3	G32
vcc1p2x	AJ26	vcc1p8	AM32	vcc3p3	J6
vcc1p2x	AJ27	vcc1p8	AN32	vcc3p3	K6
vcc1p2x	AJ28	vcc1p8	AP32	vcc3p3	N6
vcc1p2x	AJ30	vcc1p8	AR32	vcc3p3	R6
vcc1p2x	AK25	vcc1p8	AT32	vcc3p3	T6
vcc1p2x	AK27	vcc1p8	AU32	vcc3p3	V6
vcc1p2x	AK29	vcc1p8e	AM25	vcc3p3	W6
vcc1p2x	AK31	vcc1p8e	AM26	vcc3p3	AB6
vcc1p2x	AL24	vcc1p8e	AN17	vcc3p3	AE6
vcc1p2x	AL26	vcc1p8e	AN18	vcc3p3	AH6
vcc1p2x	AL27	vcc1p8e	AN21	vcc3p3	AL6
vcc1p2x	AL28	vcc1p8e	AN22	vcc3p3	AM6
vcc1p2x	AL30	vcc1p8e	AN23	vcc3p3	AM7
vcc1p2x	AM27	vcc1p8e	AN24	vcc3p3	AM8

Table 15. 413808 and 413812 1357-Lead Package - Alphabetical Signal Listings (Sheet 8 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
vcc3p3	AM9	vss	C37	vss	K10
vcc3p3	AM10	vss	D4	vss	K12
vcc3p3	AM11	vss	D7	vss	K14
vcc3p3	AM28	vss	D10	vss	K16
vcc3p3	AM29	vss	D27	vss	K18
vcc3p3	AM30	vss	D30	vss	K20
vcc3p3	AM31	vss	E2	vss	K22
vcc3p3	AN5	vss	E33	vss	K24
vcc3p3	AN30	vss	F34	vss	K26
vcc3p3	AN31	vss	F36	vss	K28
vcc3p3	AP30	vss	G2	vss	K30
vcc3p3pllx	Y29	vss	G4	vss	K34
vccvio	H5	vss	G7	vss	K36
vccvio	H6	vss	G9	vss	L7
vccvio	L5	vss	G11	vss	L9
vccvio	L6	vss	H8	vss	L11
vccvio	M6	vss	H10	vss	L13
vccvio	P5	vss	H12	vss	L15
vccvio	P6	vss	H14	vss	L17
vccvio	U5	vss	H15	vss	L19
vccvio	U6	vss	H16	vss	L21
vccvio	Y6	vss	H18	vss	L23
vccvio	AA5	vss	H22	vss	L25
vccvio	AA6	vss	H24	vss	L27
vccvio	AC6	vss	H26	vss	L29
vccvio	AD5	vss	H28	vss	L31
vccvio	AD6	vss	H30	vss	M8
vccvio	AF6	vss	J7	vss	M10
vccvio	AG5	vss	J9	vss	M12
vccvio	AG6	vss	J11	vss	M14
vccvio	AJ6	vss	J13	vss	M16
vccvio	AK5	vss	J17	vss	M18
vccvio	AK6	vss	J19	vss	M20
vss	A3	vss	J23	vss	M22
vss	A35	vss	J25	vss	M24
vss	B2	vss	J27	vss	M26
vss	B7	vss	J29	vss	M28
vss	B10	vss	J31	vss	M30
vss	B27	vss	J34	vss	M33
vss	B30	vss	J36	vss	N2
vss	B36	vss	K2	vss	N4
vss	C1	vss	K4	vss	N7
vss	C34	vss	K8	vss	N9

Table 15. 413808 and 413812 1357-Lead Package - Alphabetical Signal Listings (Sheet 9 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
vss	N13	vss	T16	vss	W19
vss	N15	vss	T18	vss	W21
vss	N17	vss	T20	vss	W23
vss	N19	vss	T22	vss	W25
vss	N21	vss	T24	vss	W27
vss	N23	vss	T26	vss	W31
vss	N25	vss	T28	vss	W33
vss	N27	vss	T30	vss	Y8
vss	N29	vss	T34	vss	Y10
vss	N31	vss	T36	vss	Y12
vss	N34	vss	U7	vss	Y14
vss	N36	vss	U9	vss	Y16
vss	P8	vss	U11	vss	Y18
vss	P10	vss	U13	vss	Y20
vss	P12	vss	U15	vss	Y22
vss	P14	vss	U17	vss	Y24
vss	P16	vss	U19	vss	Y26
vss	P18	vss	U21	vss	Y28
vss	P20	vss	U23	vss	Y30
vss	P22	vss	U25	vss	Y35
vss	P24	vss	U27	vss	AA7
vss	P26	vss	U31	vss	AA9
vss	P28	vss	V8	vss	AA11
vss	P30	vss	V10	vss	AA13
vss	R7	vss	V12	vss	AA15
vss	R9	vss	V14	vss	AA17
vss	R11	vss	V16	vss	AA19
vss	R13	vss	V18	vss	AA21
vss	R15	vss	V20	vss	AA23
vss	R17	vss	V22	vss	AA25
vss	R19	vss	V24	vss	AA27
vss	R21	vss	V26	vss	AA29
vss	R23	vss	V30	vss	AA31
vss	R25	vss	V35	vss	AB2
vss	R27	vss	W1	vss	AB4
vss	R29	vss	W2	vss	AB8
vss	R31	vss	W4	vss	AB10
vss	T2	vss	W7	vss	AB12
vss	T4	vss	W9	vss	AB14
vss	T8	vss	W11	vss	AB16
vss	T10	vss	W13	vss	AB18
vss	T12	vss	W15	vss	AB20
vss	T14	vss	W17	vss	AB22

Table 15. 413808 and 413812 1357-Lead Package - Alphabetical Signal Listings (Sheet 10 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
vss	AB24	vss	AE27	vss	AH30
vss	AB26	vss	AE29	vss	AH34
vss	AB28	vss	AE31	vss	AH36
vss	AB30	vss	AE34	vss	AJ7
vss	AB34	vss	AE36	vss	AJ9
vss	AB36	vss	AF8	vss	AJ11
vss	AC7	vss	AF10	vss	AJ13
vss	AC9	vss	AF12	vss	AJ15
vss	AC11	vss	AF14	vss	AJ17
vss	AC13	vss	AF16	vss	AJ19
vss	AC15	vss	AF18	vss	AJ21
vss	AC17	vss	AF20	vss	AJ23
vss	AC19	vss	AF22	vss	AJ25
vss	AC21	vss	AF24	vss	AJ29
vss	AC23	vss	AF26	vss	AJ31
vss	AC25	vss	AF28	vss	AJ34
vss	AC27	vss	AF30	vss	AJ36
vss	AC31	vss	AG7	vss	AK8
vss	AD8	vss	AG9	vss	AK10
vss	AD10	vss	AG11	vss	AK12
vss	AD12	vss	AG13	vss	AK14
vss	AD14	vss	AG15	vss	AK16
vss	AD16	vss	AG17	vss	AK18
vss	AD18	vss	AG19	vss	AK22
vss	AD20	vss	AG21	vss	AK24
vss	AD22	vss	AG23	vss	AK26
vss	AD24	vss	AG25	vss	AK28
vss	AD26	vss	AG27	vss	AK30
vss	AD28	vss	AG29	vss	AL2
vss	AD30	vss	AG31	vss	AL4
vss	AD33	vss	AH2	vss	AL7
vss	AE2	vss	AH4	vss	AL9
vss	AE4	vss	AH8	vss	AL11
vss	AE7	vss	AH10	vss	AL13
vss	AE9	vss	AH12	vss	AL15
vss	AE11	vss	AH14	vss	AL17
vss	AE13	vss	AH16	vss	AL21
vss	AE15	vss	AH18	vss	AL23
vss	AE17	vss	AH20	vss	AL25
vss	AE19	vss	AH22	vss	AL29
vss	AE21	vss	AH24	vss	AL31
vss	AE23	vss	AH26	vss	AL33
vss	AE25	vss	AH28	vss	AM34

Table 15. 413808 and 413812 1357-Lead Package - Alphabetical Signal Listings (Sheet 11 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
vss	AM36	vssas	B18	vsse	AR22
vss	AP4	vssas	B21	vsse	AR25
vss	AP7	vssas	B24	vsse	AT13
vss	AP10	vssas	C12	vsse	AT16
vss	AP28	vssas	C15	vsse	AT19
vss	AP31	vssas	C18	vsse	AT22
vss	AR1	vssas	C21	vsse	AT25
vss	AR34	vssas	C24	vsse	AU13
vss	AR37	vssas	D12	vsse	AU16
vss	AT2	vssas	D15	vsse	AU19
vss	AT7	vssas	D18	vsse	AU22
vss	AT10	vssas	D21	vsse	AU25
vss	AT28	vssas	D24	vssplld	AC29
vss	AT31	vssds	E12	vssplp	N11
vss	AT33	vssds	E14	vsspllso	J21
vss	AT36	vssds	F13	vsspllso1	J16
vss	AU3	vssds	F17	vssplx	U29
vss	AU33	vssds	G14	warm_rst#	E4
vss	AU34	vssds	G17	xint#[0]	B8
vss	AU35	vsse	AP13	xint#[1]	A9
vssas	A12	vsse	AP16	xint#[2]	A8
vssas	A15	vsse	AP19	xint#[3]	B9
vssas	A18	vsse	AP22	xint#[4]	D9
vssas	A21	vsse	AP25	xint#[5]	C9
vssas	A24	vsse	AR13	xint#[6]	C8
vssas	B12	vsse	AR16	xint#[7]	E9
vssas	B15	vsse	AR19		

4.0 Electrical Specifications

Table 16. Absolute Maximum Ratings

Parameter	Maximum Rating
Storage temperature	−10°C to +45°C
Supply voltage V_{CC3P3} wrt. V_{SS}	−0.5 V to +4.1 V
Supply voltage V_{CC1P8S} wrt. V_{SSAS}	−0.5 V to +2.5 V
Supply voltage V_{CC1P8E} wrt. V_{SSE}	−0.5 V to +2.5 V
Supply voltage V_{CC1P8} wrt. V_{SS}	−0.5 V to +2.5 V
Supply voltage V_{CCVIO} wrt. V_{SS}	−0.5 V to +4.1 V
Supply voltage V_{CC1P2X} wrt. V_{SS}	−0.5 V to +1.8 V
Supply voltage V_{CC1P2} wrt. V_{SS}	−0.5 V to +1.8 V
Supply voltage $V_{CC1P2AE}$ wrt. V_{SSE}	−0.5 V to +1.8 V
Supply voltage V_{CC1P2E} wrt. V_{SSE}	−0.5 V to +1.8 V
Supply voltage $V_{CC1P2AS}$ wrt. V_{SSAS}	−0.5 V to +1.8 V
Supply voltage $V_{CC1P2DS}$ wrt. V_{SSDS}	−0.5 V to +1.8 V
Voltage on any ball wrt. V_{SS}	−0.5 V to V_{CCP} +0.5 V

Notice: This data sheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product becomes available. The specifications are subject to change without notice. Contact your local Intel representative before finalizing a design.

†**WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Table 17. Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{CC3P3}	3.3 V supply voltage for PCI-X category 2 signals and general purpose I/Os	3.0	3.6	V	
V_{CC1P8S}	1.8 V supply voltage for storage interface	1.71	1.89	V	
V_{CC1P8E}	1.8 V supply voltage for PCI Express* interface	1.71	1.89	V	
V_{CC1P8}	1.8 V supply voltage for I/Os	1.71	1.89	V	
V_{CCVIO}	3.3 V supply voltage for PCI-X category 1 signals	3.0	3.6	V	
V_{CC1P2X}	1.2 V supply voltage for Intel XScale® processors	1.164	1.236	V	
V_{CC1P2}	1.2 V supply voltage for most digital logic	1.164	1.236	V	
V_{CC1P2E}	1.2 V supply voltage for PCI Express* interface digital logic	1.164	1.236	V	
$V_{CC1P2AE}$	1.2 V supply voltage for PCI Express* interface analog logic	1.164	1.236	V	
$V_{CC1P2AS}$	1.2 V supply voltage for storage interface analog logic	1.164	1.236	V	
$V_{CC1P2DS}$	1.2 V supply voltage for storage interface digital logic	1.164	1.236	V	
$V_{CC1P2PLLS0}$	1.2 V supply voltage for storage PLL 0	1.164	1.236	V	
$V_{CC1P2PLLS1}$	1.2 V supply voltage for storage PLL 1	1.164	1.236	V	
$V_{CC1P2PLLP}$	1.2 V supply voltage for PCI-X PLL	1.164	1.236	V	
$V_{CC1P2PLLD}$	1.2 V supply voltage for processor logic PLL.	1.164	1.236	V	
$V_{CC3P3PLLX}$	3.3 V supply voltage for processor logic PLL	3.0	3.6	V	
T_C	Case temperature under bias	0	100	°C	

4.1 V_{CCPLL} Pin Requirements

To reduce clock jitter, the $V_{CC1P2PLLD}$, $V_{CC1P2PLLP}$, $V_{CC3P3PLLX}$, $V_{CC1P2PLLS0}$ and $V_{CC1P2PLLS1}$ balls for the phase-lock loop (PLL) circuits are isolated on the package. The low-pass filters, as shown in the following figures, reduce noise-induced clock jitter and its effects on timing relationships in system design.

This paragraph pertains to the $V_{CC1P2PLLD}$, $V_{CC1P2PLLP}$, $V_{CC3P3PLLX}$ filters. The filter components must be able to handle a DC current of 30 mA. Use a shielded type inductor to minimize magnetic pickup. The total series resistance from the board VCC plane (before the filter) to the VCCPLL ball must be less than 1.5 ohms (including component and trace resistance). The total series resistance from the board VCC plane (before the filter) to the top plate of the capacitor must be greater than 0.35 ohms (including component and trace resistance). The nodes connecting VCCPLL and VSSPLL to the capacitor must be as short as possible (less than 0.1 ohms). VCCPLL and VSSPLL must be routed close to each other to minimize loop area. The VSSPLL balls must be connected to the filter only and not to any other ground, as shown in Figure 7 and Figure 9. The inductor and capacitor must be placed close to each other. Any discrete resistor must be placed between the VCC board plane and the inductor. If the trace and component resistance is high enough, a discrete resistor might not be required.

This paragraph pertains to the $V_{CC1P2PLLS0}$, $V_{CC1P2PLLS1}$ filters. The recommended filter for the PLL supplies is shown in Figure 8. The purpose of this filter is to achieve at least 10 dB rejection of frequencies between 1 and 20 MHz. The current draw for the IC is less than 85 mA. The board's supply distribution system must ensure that the minimum voltage into the filter is equal to or greater than 1.14 V. The filter components are selected to achieve a corner frequency of 100 KHz. The series resistance keeps the Q of this resonant circuit safely below unity for all component variations.

The bypass capacitor must be placed as close to the supply pins as possible. The series impedances to both the supply pin and the PCB analog ground plane must be an order of magnitude lower than the ESR and ESL specified for the capacitor. The S0/S1 PLLs have dedicated internal supplies, so the VSSPLLS0/S1 pins must be soldered directly to the analog ground plane of the PCB.

Figure 7. $V_{CC3P3PLLX}$ Low-Pass Filter

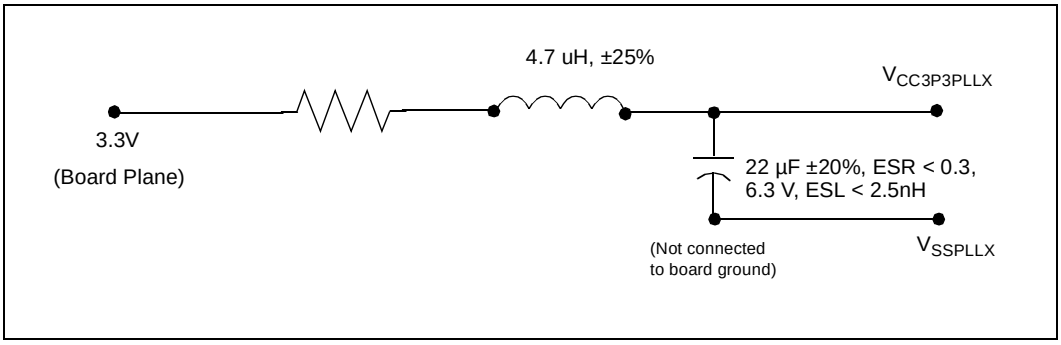


Figure 8. $V_{CC1P2PLLS0}$, $V_{CC1P2PLLS1}$ Low-Pass Filter

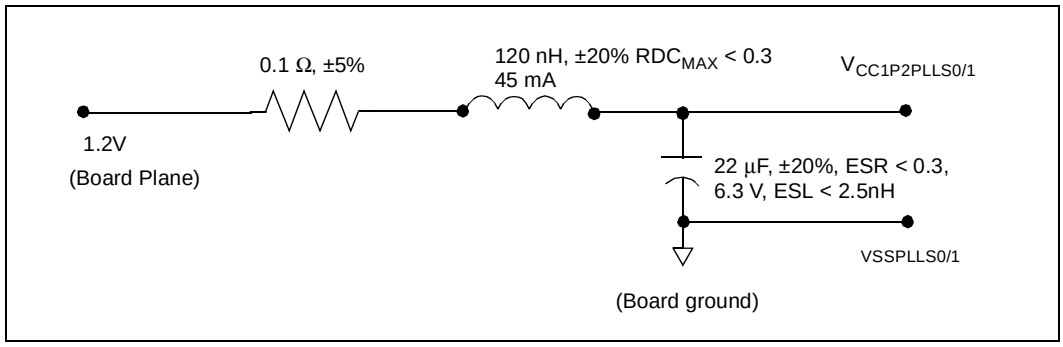
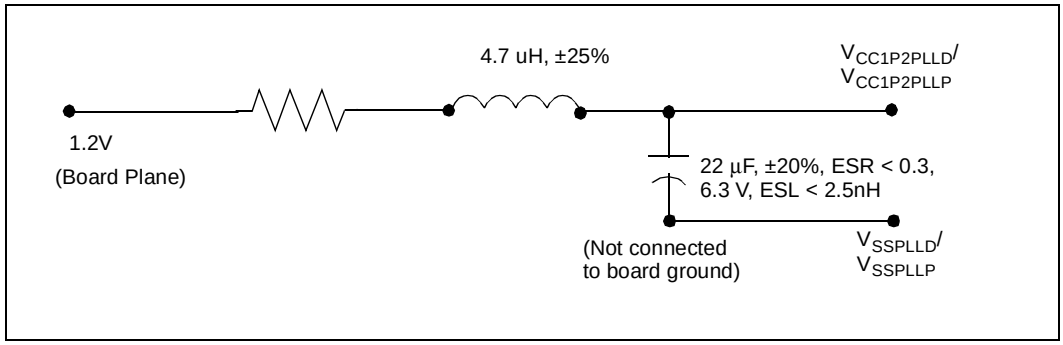


Figure 9. $V_{CC1P2PLLD}$, $V_{CC1P2PLLP}$ Low-Pass Filter



4.2 Targeted DC Specifications

Table 18. DC Characteristics

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{IL1}	Input Low Voltage (General Purpose).	-0.3	$0.3V_{CC3P3}$	V	a
V_{IH1}	Input High Voltage (General Purpose).	2.0	V_{CC3P3} + 0.3	V	a
V_{IL2}	Input Low Voltage (PCI).	-0.5	$0.3V_{CC3P3}$	V	
V_{IL3}	Input Low Voltage (PCI-X).	-0.5	$0.35V_{CC3P3}$	V	
V_{IH3}	Input High Voltage (PCI-X/PCI).	$0.5V_{CC3P3}$	V_{CC3P3} + 0.5	V	
V_{OL1}	Output Low Voltage (General Purpose).	–	0.4	V	I_{OL} = 10 mA a
V_{OH1}	Output High Voltage (General Purpose).	2.6	–	V	I_{OH} = -10 mA a
V_{OL2}	Output Low Voltage (PCI-X).	–	$0.1V_{CC3P3}$	V	I_{OL} = 1.50 mA
V_{OH2}	Output High Voltage (PCI-X).	$0.9V_{CC3P3}$	–	V	I_{OH} = -0.50 mA
I_{LI1}	Input Leakage Current for General Purpose pins when internal pull up resistors are not enabled.		±5	µA	$0 \le V_{IN} \le V_{CC3P3}$ b
I_{LI2}	Input Leakage Current for PCI-X pins when internal pull up resistors are not enabled.		±10	µA	$0 \le V_{IN} \le V_{CC3P3}$ (Cat. 2) $0 \le V_{IN} \le V_{CCVIO}$ (Cat. 1) b
R_{GP}	Internal pull up resistor value for General Purpose pins.	28.5	38.7	KΩ	c
R_{PCIX}	Internal pull up resistor value for PCI-X pins.	5.9	8.1	KΩ	c
C_{GP}	General Purpose pin Capacitance.	1	4.5	pF	c
C_{PCIX}	PCI-X pin Capacitance.	1	4.5	pF	c
L_{PIN}	Ball Inductance.	1	12	nH	c

a. General Purpose signals include all signals that are not part of the PCI-X and PCI-Express interfaces or the Storage Tx/Rx pairs and analog pins.
b. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs
c. Not tested, guaranteed by design.

Table 19. I_{CC} Characteristics for the Intel® 413808 and 413812 I/O Controllers

Symbol	Parameter	Typ	Max	Units	Notes
Icc12 Active (Power Supply)	Power Supply Current: • PCI Express A&D • Intel XScale® michroarchitecture: - 800 MHz - 1200 MHz		 7.43 7.96	A	1, 2, 4
Icc18 Active (Power Supply)	Power Supply Current: • Storage PHY I/O • PCI Express I/Os: - 800 MHz - 1200 MHz		1.00	A	1, 2, 4
Icc33 Active (Power Supply)	Power Supply Current: • PCI, PBI, GPIO • PCI-X I/Os: - 800 MHz - 1200 MHz		0.69	A	1, 2
Icc12 Active (Thermal)	Thermal Current: • PCI Express • Intel XScale® michroarchitecture: - 800 MHz - 1200 MHz	 5.31 6.42		A	1, 3, 4
Icc18 Active (Thermal)	Thermal Current: • Storage PHY I/Os • PCI Express I/Os:	0.92		A	1, 3, 4
Icc33 Active (Thermal)	Thermal Current: • PCI, PBI, GPIO • PCI-X I/Os	0.56		A	1, 3

Notes:

1. Measured with the device operating and outputs loaded to the test condition in Figure 14, "AC Test Load for all Signals Except PCI, PCI-Express and Storage PHY" on page 80.
2. Icc Active (Power Supply) value is provided for selecting the system power supply. This is based on the worst case data patterns and skew material at the following worst case voltages: Vcc33 = 3.63 V, Vcc18 = 1.89 V, Vcc12 = 1.24 V and ambient temperature = 55°C.
3. Icc Active (Thermal) value is provided for selecting the system thermal design power (TDP). This is based on the following typical voltages: Vcc33 = 3.3 V, Vcc18 = 1.8 V, Vcc12 = 1.2 V and ambient temperature = 55°C.
4. The Customer Reference Boards use a 1.2 V switching regulator for all the 1.2 V supplies (Vcc1p2, Vcc1p2x, Vcc1p2e, Vcc1p2ds, Vcc1p2ae, Vcc1p2as) and a 1.8 V switching regulator for all 1.8 V supplies: (Vcc1p8e, Vcc1p8s)

Note: The power numbers listed in Table 19 were measured with transport firmware running on a single core.

4.3 Targeted AC Specifications

4.3.1 Clock Signal Timings

Table 20. PCI Clock Timings

Symbol	Parameter	PCI-X 133		PCI-X 100		PCI-X 66		PCI 66		PCI 33		Units	Notes
		Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max		
T_{C1}	PCI Clock Cycle Time Jitter Class 1	7.5	11	10	15	15	22	15	25	30	50	ns	a
T_{C2}	PCI Clock Cycle Time Jitter Class 2	7.375	11	9.875	15	14.8	22	14.8	25	29.7	50		a
T_{CH1}	PCI clock High Time	2.5		3		5.5		5.5		10		ns	
TCL1	PCI clock Low Time	2.5		3		5.5		5.5		10		ns	
	PCI clock Period Jitter	125	-125	125	-125	200	-200	200	-200	300	-300	ps	b
TSR1	PCI clock Slew Rate	1.5	4	1.5	4	1.5	4	1.5	4	1	4	V/ns	c
PCI Spread Spectrum Requirements													
f_{mod}	PCI clock modulation frequency	30	33	30	33	30	33	30	33			KHz	
f_{spread}	PCI clock frequency spread	-1	0	-1	0	-1	0	-1	0			%	
PCI Output Clocks													
	PCI output clock skew		250		350		350		350		350	ps	
	PCI output clock period jitter	100	-100	150	-150	150	-150	150	-150	150	-150	ps	d, e

a. The clock frequency may not change beyond the spread-spectrum limits except while **P_RST#** or **WARM_RST#** is asserted.
b. Period jitter is the deviation between any single period of the clock and the average period of the clock.
c. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.
d. If a jitter class 2 input clock is used, output clocks can not support jitter class 1.
e. The deviation between any single period of the clock and the average period of the clock.

Table 21. PCI Express* Clock Timings

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
TF2	PCI Express* Clock Frequency		100		MHz	a
TC2	PCI Express* Clock Cycle Time	9.872			ns	
DF0	Frequency Variation	-300		300	ppm	
TCCJ	Cycle to Cycle Jitter			125	ps	
TPPJ	Peak to Peak Jitter (5–50 MHz)			50	ps	
Dc	Clock Duty Cycle	45		55	%	
Trise	REFCLK Rise Time	175		350	ps	b, c, d
Tfall	REFCLK Fall Time	175		350	ps	b, c, d
Tvrise	REFCLK Rise Time Variation			125	ps	
Tvfall	REFCLK Fall Time Variation			125	ps	
	Rise-Fall Matching			20	%	
Vca	Absolute Cross Point	0.25		0.55	V	b, e, f, g
Vcr	Relative Cross Point	Calc		Calc		h, i
Tvc	Total Variation of Vc over all edges			0.14	V	g
	Rising Edge Ringback	0.56			V	Absolute Min.
	Falling Edge Ringback			0.25	V	Absolute Max.
Vhi	High Level Voltage	0.66	0.71	0.85	V	f, j
Vli	Low Level Voltage	-0.15	0	0.15	V	f, k
Vrb	Ringback Voltage			0.10	V	f
Vovs	Maximum Overshoot			Vhi+0.3	V	f, l
Vuds	Minimum Undershoot			-0.30	V	f, m

a. The average period over any 1 µs period of time must be greater than the minimum specified period.
b. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK equals the falling edge of REFCLK#.
c. Measured from V_{OL} = 0.175 V to V_{OH} = 0.525 V. Valid only for rising REFCLK and falling REFCLK#. Signal must be monotonic through the V_{OL} to V_{OH} region for T_{RISE} and T_{FALL}.
d. Measurement taken from single-ended waveform.
e. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
f. Measurement taken from differential waveform.
g. ΔV_{CROSS} is defined as the total variation of all crossing voltages of Rising REFCLK and Falling REFCLK#. This is the maximum allowed variance in V_{CROSS} for any particular system.
h. V_{CROSS}(rel) Min and Max are derived using the following:

$V_{CROSS}(rel)\ Min = 0.5\ (V_{havg} - 0.710) + 0.250$
$V_{CROSS}(rel)\ Max = 0.5\ (V_{havg} - 0.710) + 0.550$

i. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
j. V_{HIGH} is defined as the statistical average High value as obtained by using the Oscilloscope V_{HIGH} Math function.
k. V_{LOW} is defined as the statistical average Low value as obtained by using the Oscilloscope V_{LOW} Math function.
l. Overshoot is defined as the absolute value of the maximum voltage.
m. Undershoot is defined as the absolute value of the minimum voltage.

Table 22. Peripheral Bus Interface Signal Timings

Symbol	Parameter	Min.	Nom.	Max.	Units
A2D	Address to Data wait-states	4	-	20	clks
D2D	Data to Data wait-states	4	-	20	clks
REC	Recovery wait-states	1	-	20	clks
N	Number of Data phases	1	-	4	phases
Tasc	Address setup to CE#	25	30	-	ns
Taso	Address setup to OE#	10	15	-	ns
Tasw	Address setup to WE#	25	30	-	ns
Tah	Address hold from CE#,OE#	Nom - 5	REC × 15	-	ns
Tahw	Address hold from WE#	Nom - 5	(REC+1) × 15	-	ns
Twce	CE# pulse width	Nom - 5	(A2D + 2 + ((N - 1)(D2D + 2))) × 15	-	ns
Twoe	OE# pulse width	Nom - 5	(A2D + 3 + ((N - 1)(D2D + 2))) × 15	-	ns
Twwe	WE# pulse width	Nom - 5	(A2D + 1) × 15	-	ns
Tdsw	Write Data setup to WE#	Nom - 5	(A2D + 1) × 15	-	ns
Tdhw	Write Data hold from WE#	10	15	20	ns
Tad1	1st Read Data access time from Address	-	(A2D + 4) × 15	Nom - 11	ns
TadN	Nth Read Data access time from Address	-	(D2D + 2) × 15	Nom - 11	ns
Tcd	Read Data access time from CE#	-	(A2D + 2) × 15	Nom - 11	ns
Toe	Read Data access time from OE#	0	(A2D + 3) × 15	Nom - 11	ns
Tdh	Read Data hold time from Address, CE#, OE#	0	(REC + 2) × 15	Nom - 5	ns

Note: See Figure 21, "PBI Output Timings" on page 83 and Figure 22, "PBI External Device Timings (Flash)" on page 84.

4.3.2 I²C/SMBus Interface Signal Timings

Table 23. I²C/SMBus Signal Timings

Symbol	Parameter	Std. Mode		Fast Mode		Units	Notes
		Min.	Max	Min.	Max		
FSCL	**SCL** Clock Frequency	0	100	0	400	KHz	
T_{BUF}	Bus Free Time Between STOP and START Condition	4.7		1.3		µs	a
T_{HDSTA}	Hold Time (repeated) START Condition	4		0.6		µs	a,b
T_{LOW}	**SCL** Clock Low Time	4.7		1.3		µs	a,c
THIGH	**SCL** Clock High Time	4		0.6		µs	a,c
TSUSTA	Setup Time for a Repeated START Condition	4.7		0.6		µs	a
THDDAT	Data Hold Time	0	3.45	0	0.9	µs	a
TSUDAT	Data Setup Time	250		100		ns	a
T_{SR}	**SCL** and **SDA** Rise Time		1000	$20 + 0.1C_b$	300	ns	a,d
T_{SF}	**SCL** and **SDA** Fall Time		300	$20 + 0.1C_b$	300	ns	a,d)
T_{SUSTO}	Setup Time for STOP Condition	4		0.6		µs	a

a. See Figure 13, "I²C Interface Signal Timings" on page 80.
b. After this period, the first clock pulse is generated.
c. Not tested.
d. C_b = the total capacitance of one bus line, in pF.

4.3.3 PCI Bus Interface Signal Timings

Table 24. PCI Signal Timings

Symbol	Parameter			PCI-X 133 PCI-X 100		PCI-X 66		PCI 66		PCI 33		Units	Notes
				Min.	Max	Min.	Max	Min.	Max	Min.	Max		
T_{OV1}	Clock to Output Valid Delay			0.7	3.7	0.7	3.7	1	6	2	11	ns	a, b
T_{OF}	Clock to Output Float Delay				7		7		14		28	ns	a, c
T_{IS1}	Input Setup to clock			1.2		1.7		3		7		ns	d
T_{IH1}	Input Hold time from clock			0.5		0.5		0		0		ns	d
T_{RST}	Reset Active Time			1		1		1		1		ms	
T_{RF}	Reset Active to output float delay				40		40		40		40	ns	
T_{IS3}	REQ64# to Reset setup time			10		10		10		10		clocks	
T_{IH2}	Reset to REQ64# hold time			0	50	0	50	0	50	0	50	ns	
T_{IS4}	PCI-X initialization pattern to Reset setup time			10		10						clocks	
T_{IH3}	Reset to PCI-X initialization pattern hold time			0	50	0	50					ns	

Notes:

1. See the timing measurement conditions in; Figure 11, "Output Timing Measurement Waveforms" on page 79.
2. See the timing measurement conditions in: Figure 12, "Input Timing Measurement Waveforms" on page 80.
3. See Figure 15, "PCI/PCI-X TOV(max) Rising Edge AC Test Load" on page 81,Figure 16, "PCI/PCI-X TOV(max) Falling Edge AC Test Load" on page 81, Figure 17, "PCI/PCI-X TOV(min) AC Test Load" on page 81.
4. For purposes of Active/Float timing measurements, the Hi-Z or "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

a. See the timing measurement conditions in; Figure 11, "Output Timing Measurement Waveforms" on page 79.
b. See Figure 15, "PCI/PCI-X TOV(max) Rising Edge AC Test Load" on page 81,Figure 16, "PCI/PCI-X TOV(max) Falling Edge AC Test Load" on page 81, Figure 17, "PCI/PCI-X TOV(min) AC Test Load" on page 81.
c. For purposes of Active/Float timing measurements, the Hi-Z or "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
d. See the timing measurement conditions in: Figure 12, "Input Timing Measurement Waveforms" on page 80.

4.3.4 PCI Express* Differential Transmitter (Tx) Output Specifications

Table 25. PCI Express* Rx Input Specifications

Symbol	Parameter	Min.	Nom	Max	Units	Notes
$V_{DIFFp-p}$	Differential input voltage	0.175		1.200	V	a
J_{TOTAL}	Total output jitter			0.65	UI	b
V_{CM-AC}	AC common mode			100	mV	c
T_{Reye}	Receiver eye opening	0.35			UI	d
$RL\text{-}Diff_{RX}$	Differential return loss	12			dB	e
$RL\text{-}CM_{TX}$	Common mode return loss	6			dB	e
$Z_{RX-OUT-DC}$	DC differential output impedance	90	100	110	Ohm	f
$Z_{RX-Match-DC}$	D+/D- impedance matching	-5		+5	%	g
$V_{RX-SQUELCH}$	Squelch detect threshold	75		175	mV	h
Cin_{RX}	AC coupled	75			nf	i
$L_{SKEW-RX}$	Lane to lane skew at Rx			20	UI	j

a. Peak-Peak differential voltage. $V_{DIFFp-p} = 2 \times V_{RMAx}$. Measured at the package pins of the receiver. See Figure 12.
b. Max Jitter tolerated by Rx. This is the nominal value tolerated at the package pin of the receiver device. A receiver must therefore tolerate any additional jitter generated by the package to the die.
c. Peak common mode value. $|V_{D+} + V_{D-}|/2 - V_{CM-DC(avg)}$
d. See Figure 20, "Receiver Eye Opening (Differential)" on page 82.
e. 50 MHz to 1.6 GHz. The driver output impedance shall result in a differential return loss greater than or equal to 15 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.8 GHz. This output impedance requirement applies to all valid output levels. The reference impedance for return loss measurements is 100 ohm for differential return loss and 25 ohm for common mode (i.e. as measured by a Vector Network Analyzer with 100 ohm differential probes). Note this is based on a nominal PCI Express* interconnect differential characteristic impedance of 100 ohm. Applicable during active (L0) and Align states only.
f. DC Differential Mode Impedance 100 ohm ±10% tolerance.
g. DC impedance matching between two lanes of a port.
h. Peak-to-Peak value. Measured at the pin of the receiver. Differential signal below this level will indicate a squelch condition.
i. All receivers shall be AC coupled to the media.
j. Lane skew at the Receiver that must be tolerated.

Table 26. PCI Express* Tx Output Specifications

Symbol	Parameter	Min.	Nom	Max	Units	Notes
UI	Unit Interval		400		ps	a
$V_{DIFFp-p}$	Differential output voltage	0.800		1.200	V	b
T_{rise}, T_{fall}	Driver Rise/Fall Time	0.2		0.4	UI	c
$V_{TX-CM-AC}$	AC Common Mode			20	mV	d
$V_{TX-CM-DC\ delta}$	Common Mode Active to Sleep mode delta	-50		+50	mV	
RL-$Diff_{TX}$	Differential Return Loss	15			dB	e
RL-CM_{TX}	Common Mode Return Loss	6			dB	e
$Z_{TX-OUT-DC}$	DC Differential Output Impedance	90	100	110	Ohm	f
$Z_{TX-Match-DC}$	D+/D- impedance matching	-5		+5	%	g
$L_{SKEW-TX}$	Lane to Lane Skew at Tx			500	ps	h
J_{TOTAL}	Total Output Jitter.			0.35	UI	i
T_{Deye}	Minimum Transmitter eye opening.	0.65			UI	j
$I_{TX-SHORT}$	Short circuit Current	-100		100	mA	k
$V_{TX-IDLE}$	Sleep mode Voltage Output	0	0	20	mV	l

a. ±300 ppm. UI does not account for SSC dictated variations. No test load is necessarily associated with this value. This UI spec is a "before transmission" specification and represents the nominal time of each bit transmission or width.
b. Peak-Peak differential voltage. $V_{DIFFp-p} = 2 \times V_{DMAx}$. Specified at the package pins into a 100 ohm test load as shown in Figure 18, "Transmitter Test Load (100 Ohm diff Load)" on page 81. Max level set by maximum single ended voltage after a reflection from an open. This value is for the first bit after a transition on the data lines. Subsequent bits of the same polarity shall have an amplitude of 6 dB (±0.5 db) less as measured differentially peak to peak than the specified value.
c. 20–80% at transmitter. Slower rise/fall times are better.
d. Peak common mode value. $|V_{D+} + V_{D-}|/2 - V_{CM-DC(avg)}$
e. 50 MHz to 1.6 GHz. The driver output impedance shall result in a differential return loss greater than or equal to 15 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.8 GHz. This output impedance requirement applies to all valid output levels. The reference impedance for return loss measurements is 100 ohm for differential return loss and 25 ohm for common mode (i.e. as measured by a Vector Network Analyzer with 100 ohm differential probes). Note this is based on a nominal PCI Express* interconnect differential characteristic impedance of 100 ohm. Applicable during active (L0) and Align states only.
f. DC Differential Mode Impedance 100 ohm ±10% tolerance. All devices shall employ on-chip adaptive impedance matching circuits to ensure the best possible termination/Zout for its Transmitters (as well as receivers).
g. DC impedance matching between two lanes of a port.
h. Between any two lanes within a single transmitter.
i. Clock source PPM mismatch is in addition to this value. Measured over 250 UI.
j. See Figure 19, "Transmitter Eye Diagram" on page 82.
k. Between any voltage from max supply to gnd with power on or off.
l. Squelch condition. Both signals brought to $V_{CM-DC-|VD+ - VD-|}$

4.3.5 PCI Express* Differential Receiver (Rx) Input Specifications

Table 27. PCI Express* Rx Input Specifications

Symbol	Parameter	Min.	Nom	Max	Units	Notes
$V_{DIFFp-p}$	Differential input voltage	0.175		1.200	V	a
J_{TOTAL}	Total Output Jitter.			0.65	UI	b
V_{CM-AC}	AC Common Mode			100	mV	c
T_{Reye}	Receiver eye opening.	0.35			UI	d
$RL\text{-}Diff_{RX}$	Differential Return Loss	15			dB	e
$RL\text{-}CM_{TX}$	Common Mode Return Loss	6			dB	e
$Z_{RX-OUT-DC}$	DC Differential Output Impedance	90	100	110	Ohm	f
$Z_{RX-Match-DC}$	D+/D- impedance matching	0-5		+5	%	g
$V_{RX-SQUELCH}$	Squelch detect threshold	75		175	mV	h
Cin_{RX}	AC coupled	400			pf	i
$L_{SKEW-RX}$	Lane to Lane Skew at Rx			20	UI	j

a. Peak-Peak differential voltage. $V_{DIFFp-p} = 2 * V_{RMAx}$. Measured at the package pins of the receiver. See Figure 12.
b. Max Jitter tolerated by Rx. This is the nominal value tolerated at the package pin of the receiver device. A receiver must therefore tolerate any additional jitter generated by the package to the die.
c. Peak common mode value. $|V_{D+} + V_{D-}|/2 - V_{CM-DC(avg)}$
d. See Figure 20, "Receiver Eye Opening (Differential)" on page 82.
e. 50 MHz to 1.6 GHz. The driver output impedance shall result in a differential return loss greater than or equal to 15 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.8 GHz. This output impedance requirement applies to all valid output levels. The reference impedance for return loss measurements is 100 ohm for differential return loss and 25 ohm for common mode (i.e. as measured by a Vector Network Analyzer with 100 ohm differential probes). Note this is based on a nominal PCI Express* interconnect differential characteristic impedance of 100 ohm. Applicable during active (L0) and Align states only.
f. DC Differential Mode Impedance 100 ohm ±10% tolerance.
g. DC impedance matching between two lanes of a port.
h. Peak to Peak value. Measured at the pin of the receiver. Differential signal below this level will indicate a squelch condition.
i. All receivers shall be AC coupled to the media.
j. Lane skew at the Receiver that must be tolerated.

4.3.6 Boundary Scan Test Signal Timings

Table 28. Boundary Scan Test Signal Timings

Symbol	Parameter	Min.	Max	Units	Notes
T_{JTF}	**TCK** Frequency	0	66	MHz	
T_{JTCH}	**TCK** High Time	7.0		ns	Measured at 1.5 V [a]
TJTCL	**TCK** Low Time	7.0		ns	Measured at 1.5 V [a]
T_{JTCR}	**TCK** Rise Time		5	ns	0.8 V to 2.0 V [a]
T_{JTCF}	**TCK** Fall Time		5	ns	2.0 V to 0.8 V [a]
T_{JTIS1}	Input Setup to **TCK**—**TDI**, **TMS**	3.0		ns	[b]
T_{JTIH1}	Input Hold from **TCK**—**TDI**, **TMS**	2.0		ns	[b]
T_{JTOV1}	**TDO** Output Valid Delay	4.25	13.25	ns	Relative to falling edge of **TCK** [c]
T_{OF1}	**TDO** Float Delay	4.25	13.25	ns	Relative to falling edge of **TCK** [d]

a. Not tested.
b. See Figure 12, "Input Timing Measurement Waveforms" on page 80.
c. See Figure 11, "Output Timing Measurement Waveforms" on page 79.
d. A float condition occurs when the output current becomes less than I_{LO}. Float delay is not tested. See Figure 11, "Output Timing Measurement Waveforms" on page 79.

4.4 AC Timing Waveforms

Figure 10. Clock Timing Measurement Waveforms

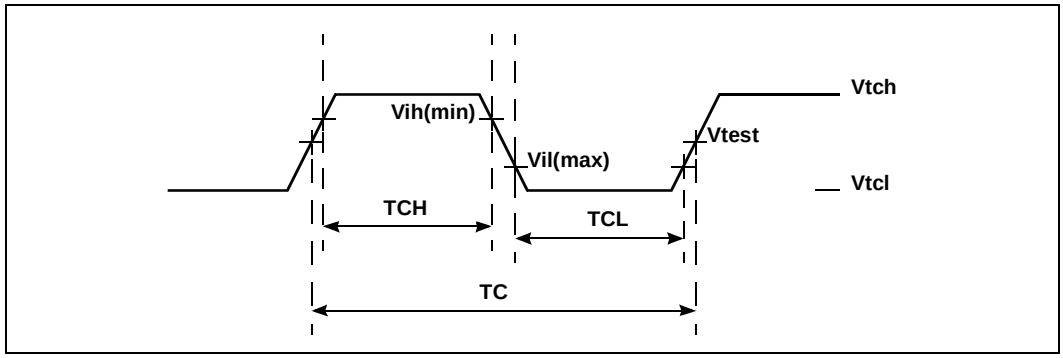


Figure 11. Output Timing Measurement Waveforms

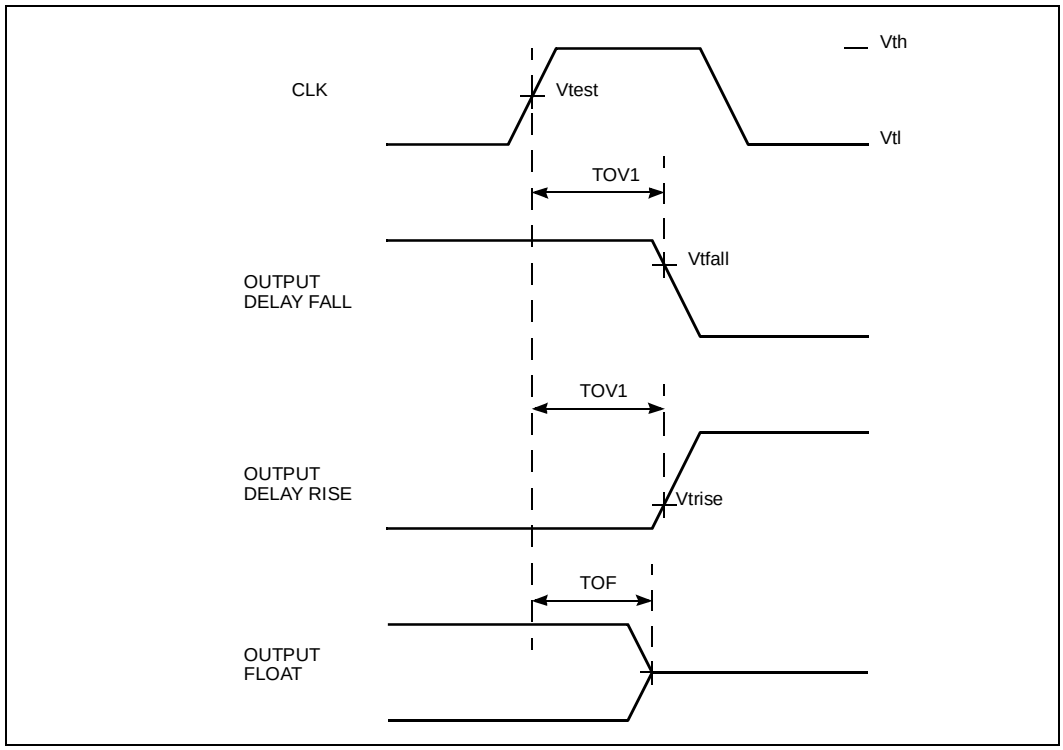


Figure 12. Input Timing Measurement Waveforms

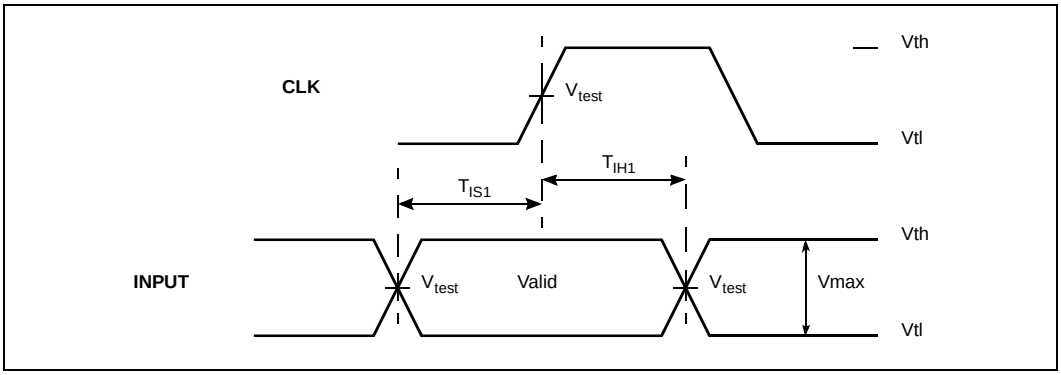


Figure 13. I²C Interface Signal Timings

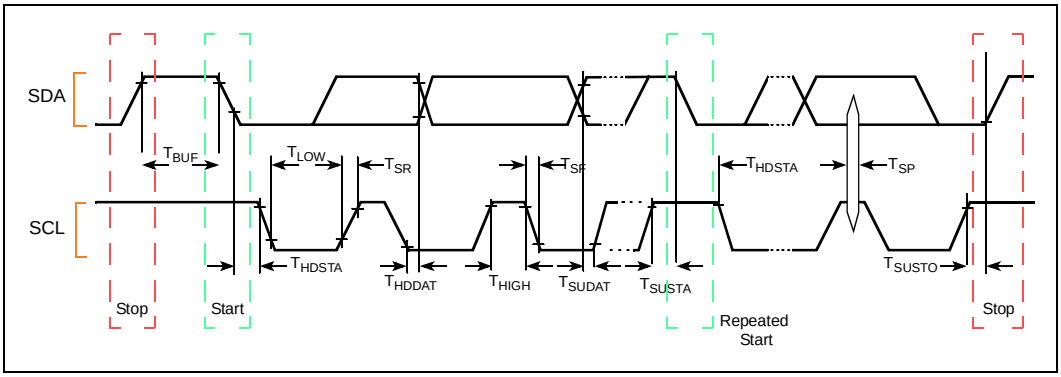


Table 29. AC Measurement Conditions

Symbol	PCI-X	PCI	PBI	Units	Notes
Vth	$0.6V_{CC3P3}$	$0.6V_{CC3P3}$	2.0	V	
V_{tl}	$0.25V_{CC3P3}$	$0.2V_{CC3P3}$	0.8	V	
V_{test}	$0.4V_{CC3P3}$	$0.4V_{CC3P3}$	1.5	V	
V_{trise}	$0.285V_{CC3P3}$	$0.285V_{CC3P3}$	1.5	V	
V_{tfall}	$0.615V_{CC3P3}$	$0.615V_{CC3P3}$	1.5	V	
V_{max}	$0.35V_{CC3P3}$	$0.4V_{CC3P3}$	1.2	V	
Slew Rate	1.5	1.5	1.0	V/nS	a

a. Input signal slew rate is measured between V_{il} and V_{ih}

Figure 14. AC Test Load for all Signals Except PCI, PCI-Express and Storage PHY

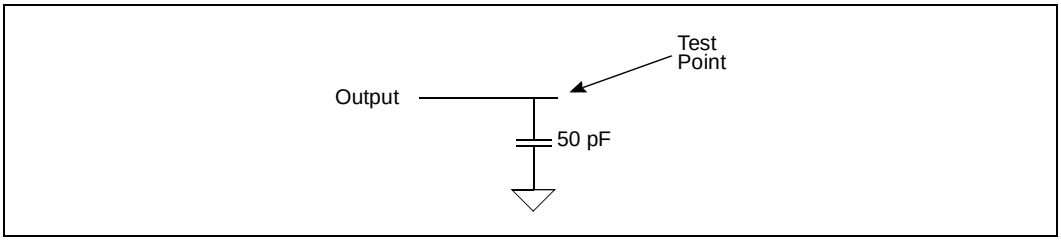


Figure 15. PCI/PCI-X $T_{OV(max)}$ Rising Edge AC Test Load

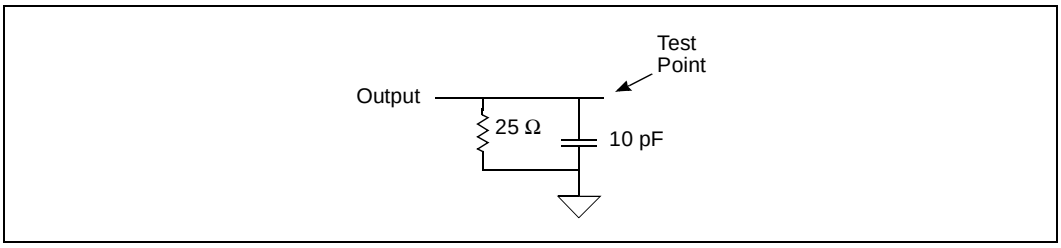


Figure 16. PCI/PCI-X $T_{OV(max)}$ Falling Edge AC Test Load

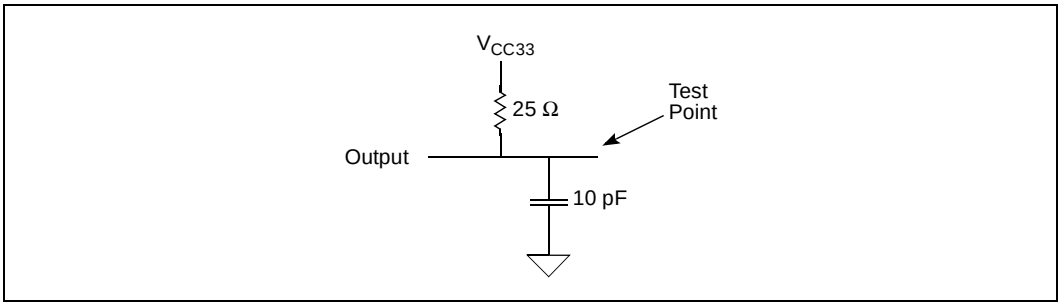


Figure 17. PCI/PCI-X $T_{OV(min)}$ AC Test Load

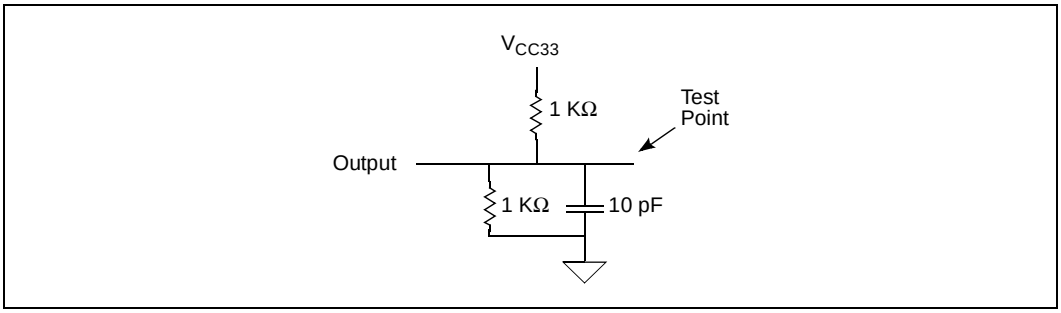


Figure 18. Transmitter Test Load (100 Ohm diff Load)

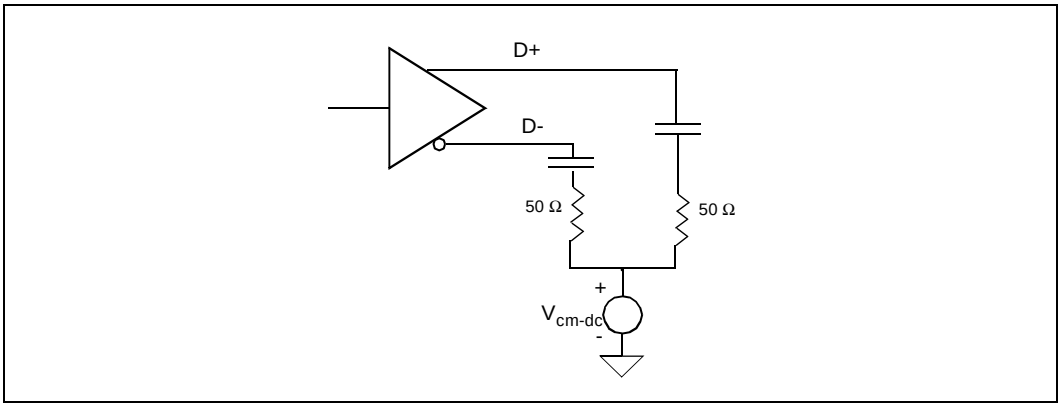


Figure 19. Transmitter Eye Diagram

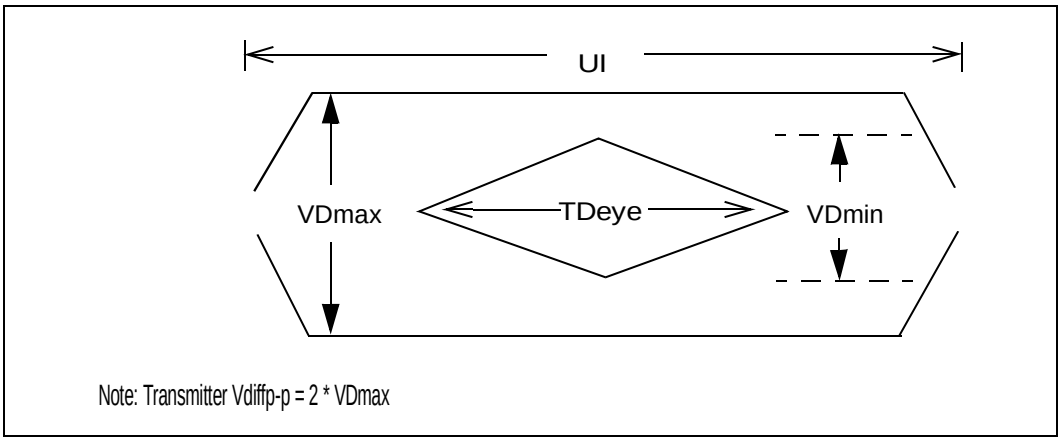


Figure 20. Receiver Eye Opening (Differential)

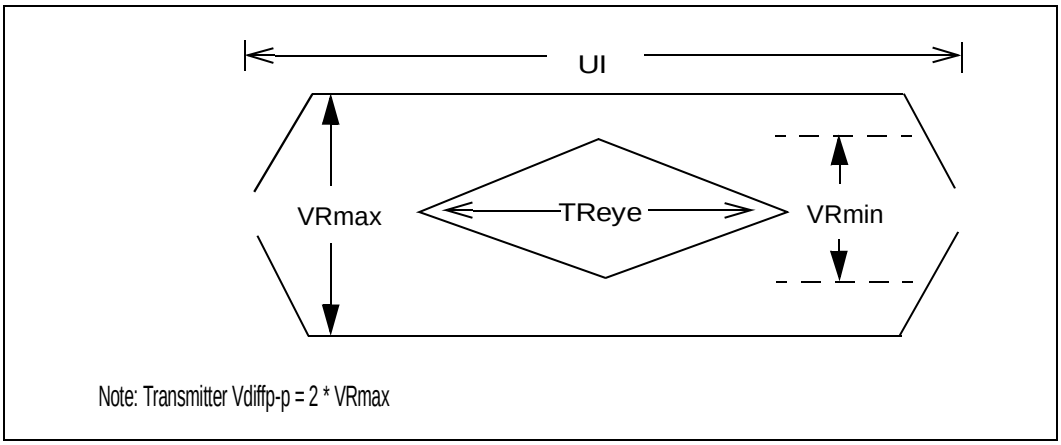
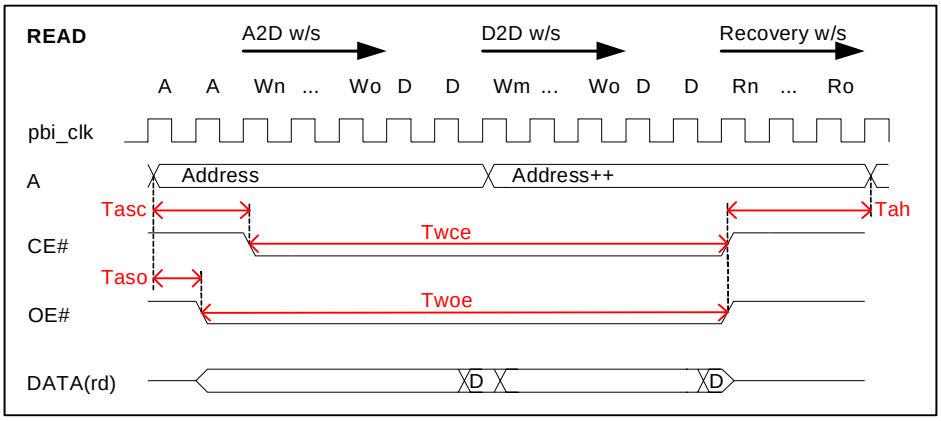
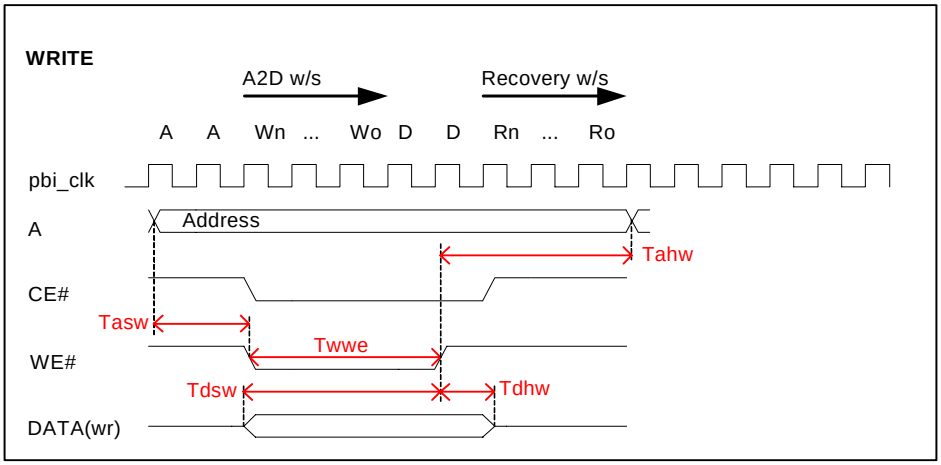


Figure 21. PBI Output Timings

PBI Output Timings - READ

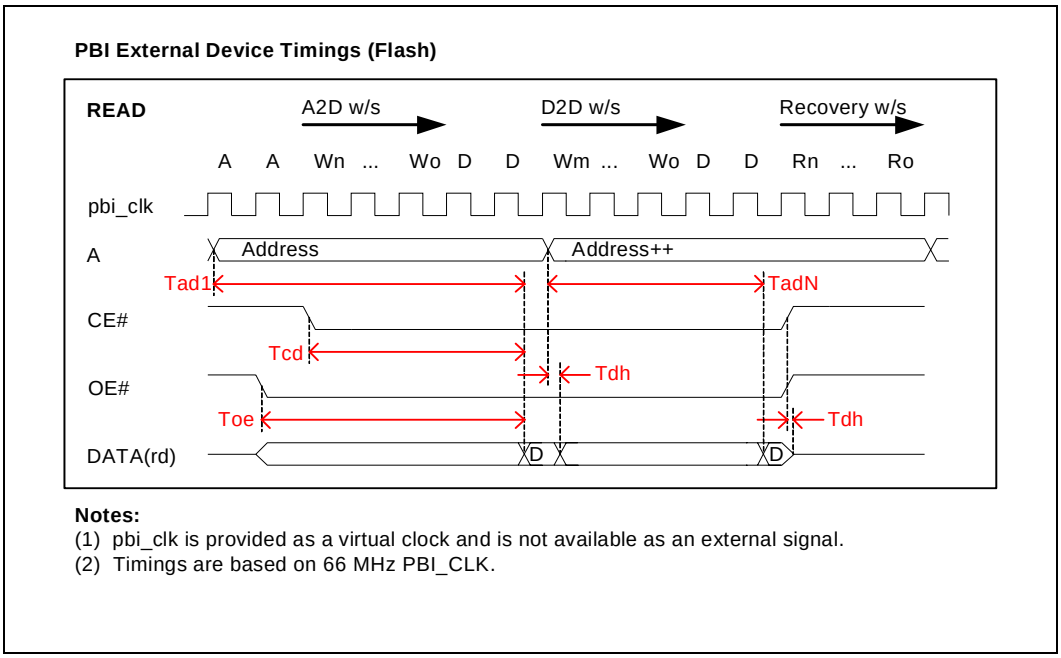


PBI Output Timings - WRITE



Notes:
(1) pbi_clk is provided as a virtual clock and is not available as an external signal.
(2) Timings are based on 66 MHz PBI_CLK.

Figure 22. PBI External Device Timings (Flash)



Notes:
(1) pbi_clk is provided as a virtual clock and is not available as an external signal.
(2) Timings are based on 66 MHz PBI_CLK.

4.5 Storage Interface Electrical Specifications

Table 30. Storage Interface Reference Clock Electrical Characteristics [S_CLKP0/ S_CLKN0]

Parameter	Limit			Unit	Condition
	Min.	Typ.	Max.		
S_CLKP0/S_CLKN0 Differential Input voltage	250	350	1000	mV diff-pk	
S_CLKP0/S_CLKN0 Input Common Mode Voltage	V_{CC1P8S} × 0.665	V_{CC1P8S} × 0.7	V_{CC1P8S} × 0.735	V	
S_CLKP0/S_CLKN0 Input Bias Voltage	V_{CC1P8S}/2 - 100 mV	V_{CC1P8S}/2	V_{CC1P8S}/2 + 100 mV	V	This is the voltage to which both S_CLKP0/ S_CLKN0 are internally biased.
S_CLKP0/S_CLKN0 Input Clock Frequency	150 - 100 ppm	150	150 + 100 ppm	MHz	1.5G, 3G
	125 - 100 ppm	125	125 + 100 ppm		1G, 1.5G, 2G, 3G, 4G
S_CLKP0/S_CLKN0 Duty Cycle	45		55	%	
S_CLKP0/S_CLKN0 Rise and Fall Ttime		0.35	0.55	nS	20% to 80%
S_CLKP0/S_CLKN0 Input Jitter			2	pS rms	10 KHz–20 MHz bandwidth
S_CLKP0/S_CLKN0 Differential Input Resistance	80	100	120	Ohm	
S_CLKP0/S_CLKN0 Differential Input Capacitance		1.5		pF	

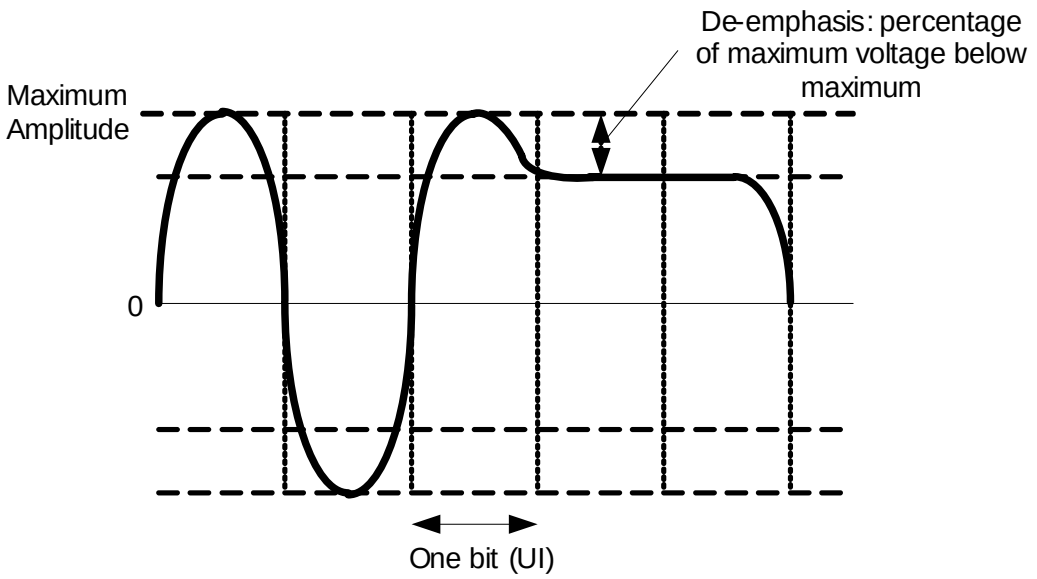
Notes:
1. S_CLKP0/S_CLKN0 are AC coupled with a 100 nF capacitor.
2. S_CLKP0/S_CLKN0 are driven from 100 ±5% Ω differential source

Table 31. Storage Interface Transmitter Output Electrical Characteristics [S_TXP[7:0] S_TXN[7:0]

Parameter	Limit			Unit	Condition
	Min.	Typ.	Max.		
S_TXP [7:0] S_TXN [7:0] Differential Output Voltage	400	500	600	mV pk-pk	SATA Gen 1i, Gen 1m
	800		1600		SATA Gen 1x, Gen 2x
	400		700		SATA Gen 2i, Gen 2m
	400		1600		SAS (including emphasis)
S_TXP [7:0] S_TXN [7:0] De-emphasis	0		44	%	See Figure 23 on page 86.
S_TXP [7:0] S_TXN [7:0] Differential Output Rise & Fall Time	47		130	pS	
S_TXP [7:0] S_TXN [7:0] Differential Output Impedance	85	100	115	Ohm	
S_TXP [7:0] S_TXN [7:0] Singled Ended Impedance		40		Ohm	

Notes:
1. Transmitter outputs are AC coupled with a 10 nF capacitor.

Figure 23. Maximum Amplitude



When emphasis is enabled, the de-emphasized output level is defined as a percentage of the maximum voltage below the maximum output level.

Table 32. Storage Interface Receiver Input Electrical Characteristics [S_RXP[7:0] S_RXN[7:0]

Parameter	Limit			Unit	Condition
	Min.	Typ.	Max.		
S_RXP [7:0] S_RXN [7:0] Differential Input Voltage	325		600	mV pk-pk	SATA Gen 1i
	240		600		SATA Gen 1m
	275		1600		SATA Gen 1x, 2x
	275		750		SATA Gen 2i
	240		750		SATA Gen 2m
	275		1600		SAS (including emphasis)
S_RXP [7:0] S_RXN [7:0] Differential Input Impedance	85	100	115	Ohm	
S_RXP [7:0] S_RXN [7:0] Common Mode Impedance	20	30	40	Ohm	

Notes:
1. Receiver inputs are AC coupled with a 10 nF capacitor.

Figure 24. Intel®413808 and Intel®413812 SAS/SATA I/O Controllers Storage PHY 1.2 V/1.8 V Power SequencingSystem Requirements

- Signal/ball names concerned: vcc1p8s, vcc1p2as and vcc1p2ds
- 1.8 V supply must never exceed the 1.2 V supply (analog or digital) when vcc1p2 < nominal