LP3907

LP3907 Dual High-Current Step-Down DC/DC and Dual Linear Regulator with I2C-Compatible Interface

Literature Number: SNVS511N

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LP3907

Dual High-Current Step-Down DC/DC and Dual Linear Regulator with I2C-Compatible Interface

General Description

The LP3907 is a multi-function, programmable Power Management Unit, optimized for low power FPGAs, microprocessors and DSPs. This device integrates two highly efficient 1A/600mA step-down DC/DC converters with dynamic voltage management (DVM), two 300mA linear regulators and a 400kHz I^{2}C compatible interface to allow a host controller access to the internal control registers of the LP3907. The LP3907 additionally features programmable power-on sequencing. Package options include a tiny 4 x 4 x 0.8mm LLP 24-pin package and an even smaller 2.5 x 2.5mm micro SMD 25-bump package.

Key Specifications

Step-Down DC/DC Converter (Buck)

- 1A/600mA output current
- Programmable V_{OUT} from:
  - Buck1 : 0.8V - 2.0V @ 1A
  - Buck2 : 1.0V - 3.5V @ 600mA
- Up to 96% efficiency
- 2.1MHz PWM switching frequency
- PWM - PFM automatic mode change under low loads
- ±3% output voltage accuracy
- Automatic soft start

Linear Regulators (LDO)

- Programmable V_{OUT} of 1.0V–3.5V (except “JJ11” and “FX6W” options)
- ±3% output voltage accuracy
- 300mA output current
- 30mV (typ) dropout

Features

- Compatible with advanced applications processors and FPGAs
- 2 LDOs for powering Internal processor functions and I/Os
- High-speed serial interface for independent control of device functions and settings
- Precision internal reference
- Thermal overload protection
- Current overload protection
- 24-lead 4 × 4 × 0.8mm LLP or 25-bump 2.5 x 2.5mm micro SMD package
- Software Programmable Regulators
- External Power-on-reset function for Buck1 and Buck2 (i.e., Power Good with delay function)
- Undervoltage lock out detector to monitor input supply voltage
- LP3907Q is an Automotive Grade product that is AECQ-100 Grade 1 qualified

Applications

- FPGA, DSP core power
- Applications processors
- Peripheral I/O power

Typical Application Circuit

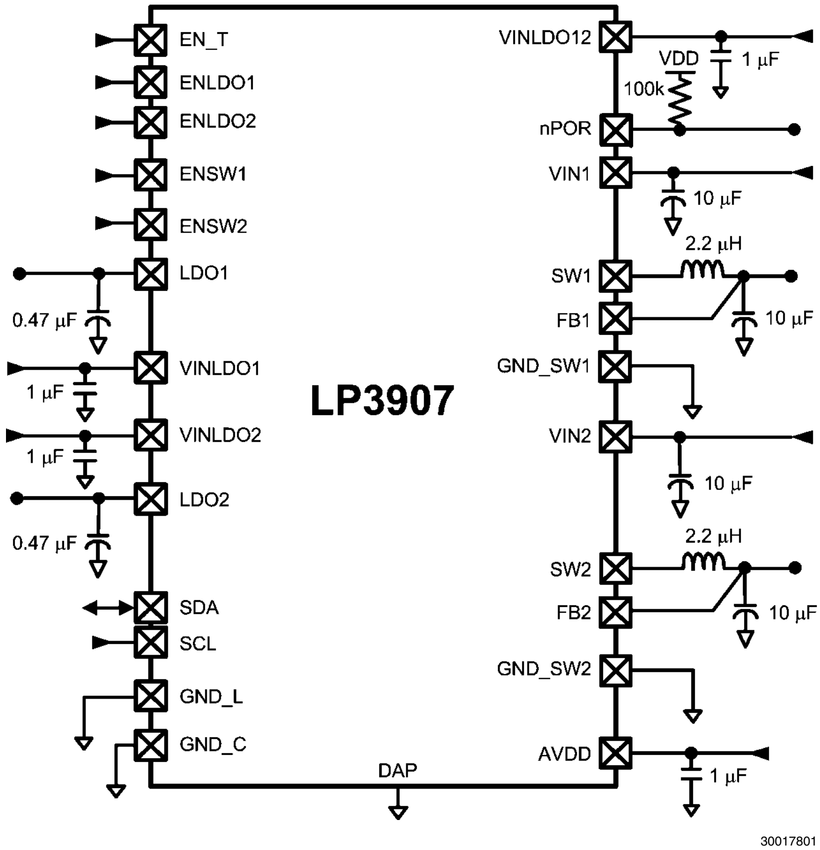


FIGURE 1. Application Circuit

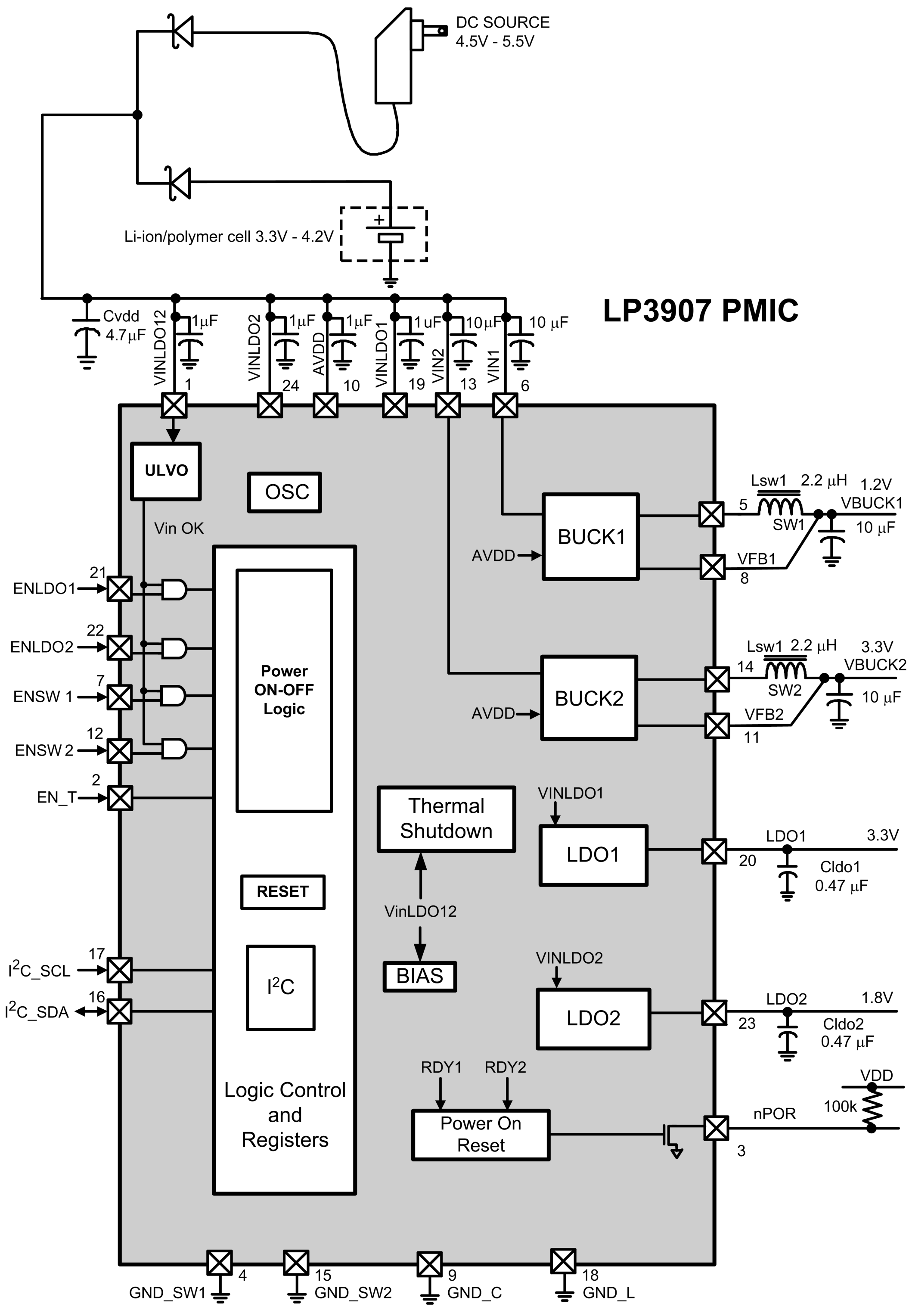
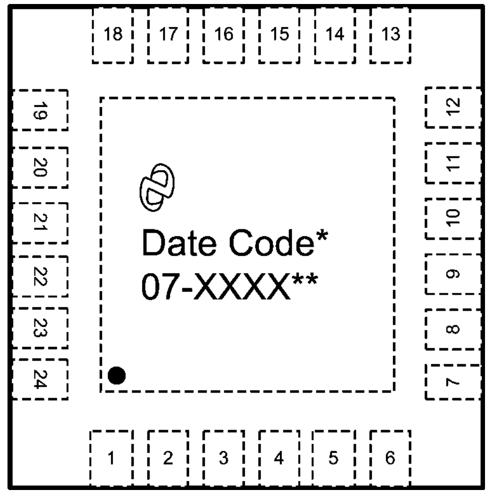


FIGURE 2. Application Circuit

Connection Diagrams and Package Mark Information



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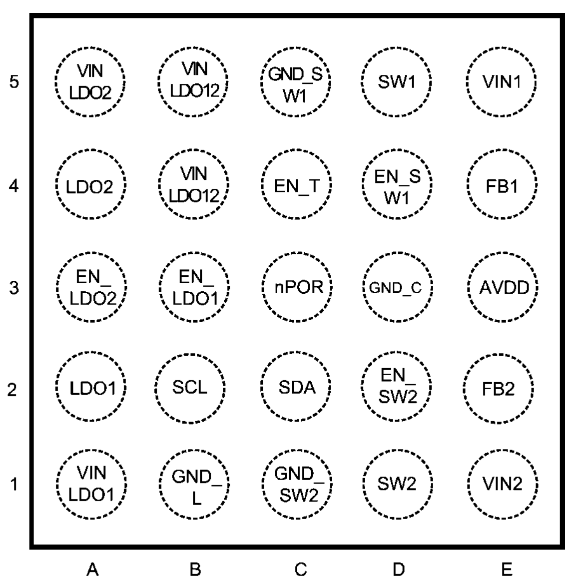
24-Lead LLP Package (top view)

Note: The physical placement of the package marking will vary from part to part.

(*) UZXYTT format: 'U' – wafer fab code; 'Z' – assembly code; 'XY' 2 digit date code; 'TT' – die run code. See http://www.national.com/quality/marking_conventions.html for more information on marking information.

(**) Package received will have XXXX replaced with the specific part version ordered.

25-Bump Thin Micro SMD Package, Large Bump National Package Number TLA25AAA



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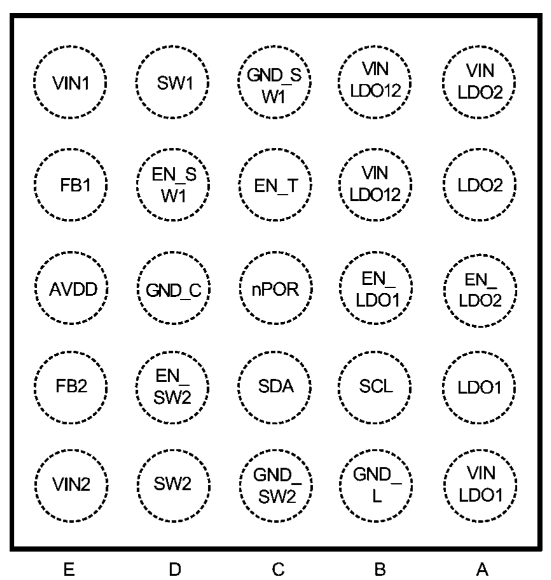
Top View



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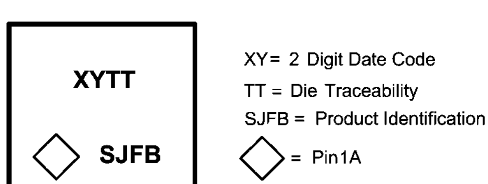
Bottom View



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Package Mark - Top View

Ordering Information

Voltage Option	Order Number	Package Type	NSC Pkg. Drawing	Package Marking	Supplied As
Voltage 'PXPP'	LP3907SQ-PXPP	24-lead LLP	SQA024AE	07-PXPP	1000 tape & reel
Voltage 'PXPP'	LP3907SQX-PXPP	24-lead LLP	SQA024AE	07-PXPP	4500 tape & reel
Voltage 'JXIP'	LP3907SQ-TJXIP	24-lead LLP	SQA024AE	07TJXIP	1000 tape & reel
Voltage 'JXIP'	LP3907SQX-TJXIP	24-lead LLP	SQA024AE	07TJXIP	4500 tape & reel
Voltage 'JXIP'	LP3907QSQ-JXIP	24-lead LLP	SQA024AE	07QJXIP	1000 tape & reel
Voltage 'JXIP'	LP3907QSQX-JXIP	24-lead LLP	SQA024AE	07QJXIP	4500 tape & reel
Voltage 'JXIP'	LP3907QSQ-JXI7	24-lead LLP	SQA024AE	07QJXI7	1000 tape & reel
Voltage 'JXIP'	LP3907QSQX-JXI7	24-lead LLP	SQA024AE	07QJXI7	4500 tape & reel
Voltage 'JXQX'	LP3907SQ-JXQX	24-lead LLP	SQA024AE	07-JXQX	1000 tape & reel
Voltage 'JXQX'	LP3907SQX-JXQX	24-lead LLP	SQA024AE	07-JXQX	4500 tape & reel
Voltage 'JYQX'	LP3907SQ-JYQX	24-lead LLP	SQA024AE	07-JYQX	1000 tape & reel
Voltage 'JYQX'	LP3907SQX-JYQX	24-lead LLP	SQA024AE	07-JYQX	4500 tape & reel
Voltage 'JXIX'	LP3907SQ-PJXIX	24-lead LLP	SQA024AE	07PJXIX	1000 tape & reel
Voltage 'JXIX'	LP3907SQX-PJXIX	24-lead LLP	SQA024AE	07PJXIX	4500 tape & reel
Voltage 'FX6W'	LP3907SQ-PFX6W	24-lead LLP	SQA024AE	7PFX6W	1000 tape & reel
Voltage 'FX6W'	LP3907SQX-PFX6W	24-lead LLP	SQA024AE	7PFX6W	4500 tape & reel
Voltage 'JX6X'	LP3907SQ-BJX6X	24-lead LLP	SQA024AE	07BJX6X	1000 tape & reel
Voltage 'JX6X'	LP3907SQX-BJX6X	24-lead LLP	SQA024AE	07BJX6X	4500 tape & reel
Voltage 'BJXQX'	LP3907SQ-BJXQX	24-lead LLP	SQA024AE	07BJXQX	1000 tape & reel
Voltage 'BJXQX'	LP3907SQX-BJXQX	24-lead LLP	SQA024AE	07BJXQX	4500 tape & reel
Voltage 'BJYQX'	LP3907SQ-BJYQX	24-lead LLP	SQA024AE	07BJYQX	1000 tape & reel
Voltage 'BJYQX'	LP3907SQX-BJYQX	24-lead LLP	SQA024AE	07BJYQX	4500 tape & reel
Voltage 'BJXIX'	LP3907SQ-BJXIX	24-lead LLP	SQA024AE	07BJXIX	1000 tape & reel
Voltage 'BJXIX'	LP3907SQX-BJXIX	24-lead LLP	SQA024AE	07BJXIX	4500 tape & reel
Voltage 'BFX6W'	LP3907SQ-BFX6W	24-lead LLP	SQA024AE	7BFX6W	1000 tape & reel
Voltage 'BFX6W'	LP3907SQX-BFX6W	24-lead LLP	SQA024AE	7BFX6W	4500 tape & reel
Voltage 'JJXP'	LP3907QSQ-JJXP	24-lead LLP	SQA024AE	07QJJXP	1000 tape & reel
Voltage 'JJXP'	LP3907QSQX-JJXP	24-lead LLP	SQA024AE	07QJJXP	4500 tape & reel
Voltage 'VRZX'	LP3907SQ-VRZX	24-lead LLP	SQA024AE	07-VRZX	1000 tape & reel
Voltage 'VRZX'	LP3907SQX-VRZX	24-lead LLP	SQA024AE	07-VRZX	4500 tape & reel
Voltage 'JJ11'	LP3907TL-JJ11	25-bump micro SMD	TLA25AAA	V013	250 tape & reel
Voltage 'JJ11'	LP3907TLX-JJ11	25-bump micro SMD	TLA25AAA	V013	3000 tape & reel
Voltage 'JSXS'	LP3907TL-JSXS	25-bump micro SMD	TLA25AAA	V012	250 tape & reel
Voltage 'JSXS'	LP3907TLX-JSXS	25-bump micro SMD	TLA25AAA	V012	3000 tape & reel
Voltage 'JJCP'	LP3907TL-JJCP	25-bump micro SMD	TLA25AAA	V016	250 tape & reel
Voltage 'JJCP'	LP3907TLX-JJCP	25-bump micro SMD	TLA25AAA	V016	3000 tape & reel
Voltage 'VXSS'	LP3907QTL-VXSS	25-bump micro SMD	TLA25AAA	V025	250 tape & reel
Voltage 'VXSS'	LP3907QTLX-VXSS	25-bump micro SMD	TLA25AAA	V025	3000 tape & reel
Voltage 'LNTO'	LP3907TL-PLNTO	25-bump micro SMD	TLA25AAA	V027	250 tape & reel
Voltage 'LNTO'	LP3907TLX-PLNTO	25-bump micro SMD	TLA25AAA	V027	3000 tape & reel

Default Voltage Options

Version	Default SW1 Voltage	Default SW2 Voltage	Default LDO1 Voltage	Default LDO2 Voltage
JXIP	1.2	3.3	1.8	2.5
JXQX	1.2	3.3	2.6	3.3
FX6W	1	3.3	2.65*	3.2
JXIX	1.2	3.3	1.8	3.3
PXPP	1.5	3.3	2.5	2.5
JXIP	1.2	3.3	1.8	2.5
JJ11	1.2	1.8	2.85*	2.85*
JJCP	1.2	1.8	1.2	2.5
JSXS	1.2	2.8	3.3	2.8
LNTO	1.3	2.2	2.9	2.4
VXSS	1.8	3.3	2.8	2.8
JX6X	1.2	3.3	2.65*	3.3
JYQX	1.2	3.4	2.6	3.3
JJXP	1.2	1.8	3.3	2.5
VRZX	1.8	2.7	3.5	3.3

* Voltage is fixed and not programmable.

Default Options

Order Suffix	Spec	Version	Buck Modes	Default EN_T Delay	Default UVLO	AECQ
QSQ-JXI7	NOPB	JXIP	Forced PWM	001	Disabled	Grade 1
QSQ-JXIP	NOPB	JXIP	Forced PWM	001	Enabled	Grade 1
SQ-JXQX	NOPB	JXQX	Auto-Mode	010	Enabled	No
SQ-JXQX	S7001874	JXQX	Forced PWM	010	Enabled	No
SQX-JXQX	S7001997	JXQX	Forced PWM	010	Enabled	No
SQ-JYQX	NOPB	JYQX	Auto-Mode	010	Enabled	No
SQ-JYQX	S7001934	JYQX	Forced PWM	010	Enabled	No
SQX-JYQX	S7002030	JYQX	Forced PWM	010	Enabled	No
SQ-PFX6W	NOPB	FX6W	Forced PWM	010	Enabled	No
SQ-PJXIX	NOPB	JXIX	Forced PWM	010	Enabled	No
SQ-PXPP	NOPB	PXPP	Auto-Mode	010	Enabled	No
TJXIP	NOPB	JXIP	Forced PWM	001	Enabled	No
TL-JJ11	NOPB	JJ11	Auto-Mode	010	Enabled	No
TL-JJCP	NOPB	JJCP	Auto-Mode	010	Enabled	No
TL-JSXS	NOPB	JSXS	Auto-Mode	010	Enabled	No
TL-PLNTO	NOPB	LNTO	Forced PWM	010	Enabled	No
QTL-VXSS	NOPB	VXSS	Forced PWM	010	Enabled	Grade 1
BJXQX	NOPB	JXQX	Forced PWM	010	Disabled	No
BJYQX	NOPB	JYQX	Forced PWM	010	Disabled	No
BJXIX	NOPB	JXIX	Forced PWM	010	Disabled	No
BJX6X	NOPB	JX6X	Forced PWM	010	Disabled	No
BFX6W	NOPB	FX6W	Forced PWM	010	Disabled	No
QSQ-JJXP	NOPB	JJXP	Forced PWM	010	Disabled	Grade 1
SQ-VRZX	NOPB	VRZX	Auto Mode	010	Enabled	No

Package Type	Default I²C Address
24-lead LLP	60
25-bump micro SMD	61

Pin Descriptions

LLP Pin No.	micro SMD pin no.	Name	I/O	Type	Description
1	B4, B5	VINLDO12	I	PWR	Analog Power for Internal Functions (VREF, BIAS, I²C, Logic)
2	C4	EN_T	I	D	Enable for preset power on sequence. (See page 22.)
3	C3	nPOR	O	D	nPOR Power on reset pin for both Buck1 and Buck 2. Open drain logic output 100K pullup resistor. nPOR is pulled to ground when the voltages on these supplies are not good. See nPOR section for more info.
4	C5	GND_SW1	G	G	Buck1 NMOS Power Ground
5	D5	SW1	O	PWR	Buck1 switcher output pin
6	E5	VIN1	I	PWR	Power in from either DC source or Battery to Buck1
7	D4	ENSW1	I	D	Enable Pin for Buck1 switcher, a logic HIGH enables Buck1
8	E4	FB1	I	A	Buck1 input feedback terminal
9	D3	GND_C	G	G	Non switching core ground pin
10	E3	AVDD	I	PWR	Analog Power for Buck converters
11	E2	FB2	I	A	Buck2 input feedback terminal
12	D2	ENSW2	I	D	Enable Pin for Buck2 switcher, a logic HIGH enables Buck2
13	E1	VIN2	I	PWR	Power in from either DC source or Battery to Buck2
14	D1	SW2	O	PWR	Buck2 switcher output pin
15	C1	GND_SW2	G	G	Buck2 NMOS Power ground
16	C2	SDA	I/O	D	I²C Data (bidirectional)
17	B2	SCL	I	D	I²C Clock
18	B1	GND_L	G	G	LDO ground
19	A1	VINLDO1	I	PWR	Power in from either DC source or battery to input terminal to LDO1
20	A2	LDO1	O	PWR	LDO1 Output
21	B3	ENLDO1	I	D	LDO1 enable pin, a logic HIGH enables the LDO1
22	A3	ENLDO2	I	D	LDO2 enable pin, a logic HIGH enables the LDO2
23	A4	LDO2	O	PWR	LDO2 Output
24	A5	VINLDO2	I	PWR	Power in from either DC source or battery to input terminal to LDO2.
DAP		DAP	GND	GND	Connection isn't necessary for electrical performance, but it is recommended for better thermal dissipation.

A: Analog Pin **D:** Digital Pin **G:** Ground Pin **PWR:** Power Pin **I:** Input Pin **I/O:** Input/Output Pin **O:** Output Pin.

	Power Block Operation		Note
Power Block Input	Enabled	Disabled	
VINLDO12	VIN+	VIN+	Always Powered
AVDD	VIN+	VIN+	Always Powered
VIN1	VIN+	VIN+ or 0V	
VIN2	VIN+	VIN+ or 0V	
LDO 1	≤ VIN+	≤ VIN+	If Enabled, Min Vin is 1.74V
LDO 2	≤ VIN+	≤ VIN+	If Enabled, Min Vin is 1.74V

VIN+ is the largest potential voltage on the device.

Absolute Maximum Ratings (Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}, SDA, SCL	−0.3V to +6V
GND to GND SLUG	±0.3V
Power Dissipation (P_{D_MAX}) (T_A=85°C, T_{MAX}=125°C,) (Note 5)	1.43W
Junction Temperature ($T_{J\text{-}MAX}$)	150°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering)	260°C
ESD Ratings Human Body Model (Note 4)	2kV

Operating Ratings: Bucks

(Note 1, Note 2, Note 7, Note 18)

V_{IN}	2.8V to 5.5V
V_{EN}	0 to (V_{IN} + 0.3V)
Junction Temperature (T_J) Range	−40°C to +125°C
Ambient Temperature (T_A) Range (Note 6)	−40°C to +85°C

Thermal Properties (Note 3, Note 5, Note 6)

Junction-to-Ambient Thermal Resistance (θ_{JA}) SQA024AE	28°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) TLA25AAA	51°C/W

General Electrical Characteristics (Note 1, Note 2, Note 7, Note 13, Note 17)

Unless otherwise noted, V_{IN} = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_Q	VINLDO12 Shutdown Current	V_{IN} = 3.6V		3		µA
V_{POR}	Power-On Reset Threshold	V_{DD} Falling Edge(Note 17)		1.9		V
T_{SD}	Thermal Shutdown Threshold			160		°C
T_{SDH}	Themal Shutdown Hysteresis			20		°C
UVLO	Under Voltage Lock Out	Rising		2.9		V
		Falling		2.7		

I²C Compatible Interface Electrical Specifications (Note 13)

Unless otherwise noted, V_{IN} = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{CLK}	Clock Frequency				400	kHz
t_{BF}	Bus-Free Time Between Start and Stop	(Note 13)	1.3			µs
t_{HOLD}	Hold Time Repeated Start Condition	(Note 13)	0.6			µs
t_{CLKLP}	CLK Low Period	(Note 13)	1.3			µs
t_{CLKHP}	CLK High Period	(Note 13)	0.6			µs
t_{SU}	Set Up Time Repeated Start Condition	(Note 13)	0.6			µs
$t_{DATAHLD}$	Data Hold time	(Note 13)	0			µs
t_{DATASU}	Data Set Up Time	(Note 13)	100			ns
T_{SU}	Set Up Time for Start Condition	(Note 13)	0.6			µs
T_{TRANS}	Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter of Both DATA & CLK Signals.	(Note 13)		50		ns

Low Drop Out Regulators, LDO1 and LDO2

Unless otherwise noted, V_{IN} = 3.6V, C_{IN} = 1.0µF, C_{OUT} = 0.47µF. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C. (Note 2, Note 7, Note 8, Note 9, Note 10, Note 11, Note 12)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Operational Voltage Range	VINLDO1 and VINLDO2 PMOS pins (Note 15)	**1.74**		**5.5**	V
V_{OUT} Accuracy	Output Voltage Accuracy (Default V_{OUT})	Load current = 1 mA	**−3**		**3**	%
ΔV_{OUT}	Line Regulation	V_{IN} = (V_{OUT} + 0.3V) to 5.0V, (Note 12), Load Current = mA			**0.15**	%/V
	Load Regulation	V_{IN} = 3.6V, Load Current = 1mA to I_{MAX}			**0.011**	%/mA
I_{SC}	Short Circuit Current Limit	LDO1-2, V_{OUT} = 0V		500		mA
$V_{IN} - V_{OUT}$	Dropout Voltage	Load Current = 50mA (Note 10)		30	**200**	mV
PSRR	Power Supply Ripple Rejection	F = 10kHz, Load Current = I_{MAX}		45		dB
θn	Supply Output Noise	10Hz < F < 100KHz		80		µVrms
I_Q (Note 11, Note 14)	Quiescent Current "On"	I_{OUT} = 0mA		40		µA
	Quiescent Current "On"	$I_{OUT} = I_{MAX}$		60		µA
	Quiescent Current "Off"	EN is de-asserted(Note 16)		0.03		µA
T_{ON}	Turn On Time	Start up from shut-down		300		µs
C_{OUT}	Output Capacitor	Capacitance for stability 0°C ≤ T_J ≤ 125°C	**0.33**	0.47		µF
		−40°C ≤ T_J ≤ 125°C	**0.68**	1.0		µF
		ESR	**5**		**500**	mΩ

Buck Converters SW1, SW2

Unless otherwise noted, V_{IN} = 3.6V, C_{IN} = 10µF, C_{OUT} = 10µF, L_{OUT} = 2.2µH ceramic. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C. (Note 2, Note 7, Note 8, Note 9, Note 11, Note 18)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	Feedback Voltage		**−3**		**+3**	%
V_{OUT}	Line Regulation	2.8< V_{IN} < 5.5 I_O =10mA		0.089		%/V
	Load Regulation	100mA < I_O < I_{MAX}		0.0013		%/mA
Eff	Efficiency	Load Current = 250mA		96		%
I_{SHDN}	Shutdown Supply Current	EN is de-asserted		0.01		µA
f_{OSC}	Internal Oscillator Frequency		**1.7**	2.1		MHz
I_{PEAK}	Buck1 Peak Switching Current Limit			1.5		A
	Buck2 Peak Switching Current Limit			1.0		
I_Q (Note 14)	Quiescent Current "On"	No load PFM Mode		33		µA
R_{DSON} (P)	Pin-Pin Resistance PFET			200		mΩ
R_{DSON} (N)	Pin-Pin Resistance NFET			180		mΩ
T_{ON}	Turn On Time	Start up from shut-down		500		µs
C_{IN}	Input Capacitor	Capacitance for stability	10			µF
C_O	Output Capacitor	Capacitance for stability	10			µF

I/O Electrical Characteristics

Unless otherwise noted: Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, T_J = –40°C to +125°C. (*Note 13*)

Symbol	Parameter	Conditions	Limit		Units
			Min	Max	
V_{IL}	Input Low Level			**0.4**	V
V_{IH}	Input High Level		**1.2**		V

Power On Reset Threshold/Function (POR)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
nPOR	nPOR = Power on reset forBuck1 and Buck2	Default		50		ms
nPOR threshold	Percentage of Target voltage Buck1 or Buck2	V_{BUCK1} AND V_{BUCK2} rising		94		%
		V_{BUCK1} OR V_{BUCK2} falling		85		
VOL	Output Level Low	Load = IoL = 500mA		0.23	0.5	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160°C (typ.) and disengages at T_J = 140°C (typ.)

Note 4: The Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. (MILSTD - 883 3015.7)

Note 5: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$. See Applications section.

Note 6: Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Note 7: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 8: C_{IN}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

Note 9: The device maintains a stable, regulated output voltage without a load.

Note 10: Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100mV below its nominal value.

Note 11: Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.

Note 12: V_{IN} minimum for line regulation values is 1.8V.

Note 13: This specification is guaranteed by design.

Note 14: The I_Q can be defined as the standing current of the LP3907 when the I²C bus is **active** and all other power blocks have been **disabled via the I²C bus**, or it can be defined as the I²C bus **active**, and the other power blocks are **active under no load condition**. These two values can be used by the system designer when the LP3907 is powered using a battery.

Note 15: Pins 24, 19 can operate from V_{IN} min of 1.74 to a V_{IN} max of 5.5V. This rating is only for the series pass PMOS power FET. It allows the system design to use a lower voltage rating if the input voltage comes from a buck output.

Note 16: The I_Q exhibits a higher current draw when the EN pin is de-asserted because the I²2 buffer pins draw an additional 2µA.

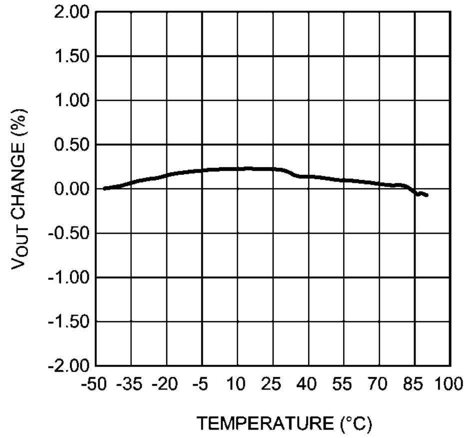
Note 17: VPOR is voltage at which the EPROM resets. This is different from the UVLO on VINLDO12, which is the voltage at which the regulators shut off; and is also different from the nPOR function, which signals if the regulators are in a specified range.

Note 18: Buck $V_{IN} \geq V_{OUT} + 1V$.

Typical Performance Characteristics — LDO

T_A = 25°C unless otherwise noted

Output Voltage Change vs Temperature (LDO1)
V_{IN} = 3.6V, V_{OUT} = 2.6V, 100mA load



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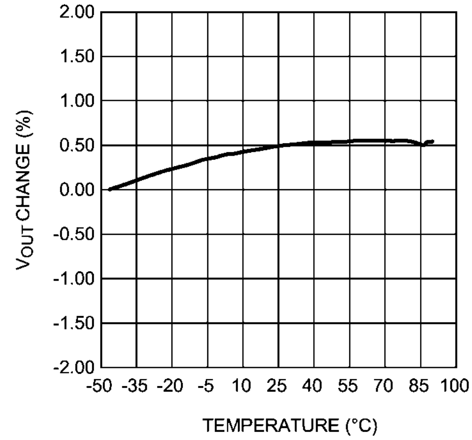
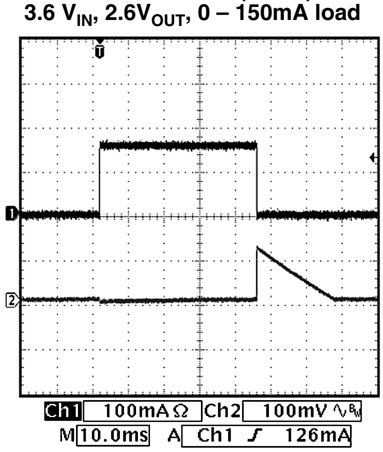
Output Voltage Change vs Temperature (LDO2)
V_{IN} = 3.6V, V_{OUT} = 3.3V, 100mA load



30017836

Load Transient (LDO1)
3.6 V_{IN}, 2.6V_{OUT}, 0 – 150mA load



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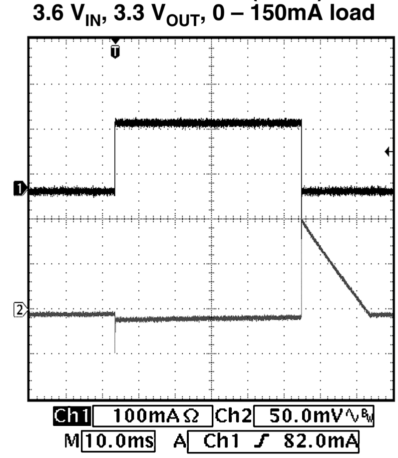
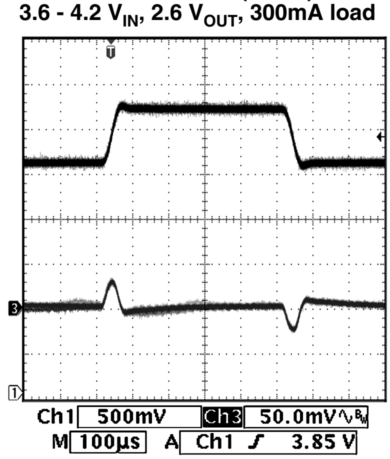
Load Transient (LDO2)
3.6 V_{IN}, 3.3 V_{OUT}, 0 – 150mA load



30017838

Line Transient (LDO1)
3.6 - 4.2 V_{IN}, 2.6 V_{OUT}, 300mA load



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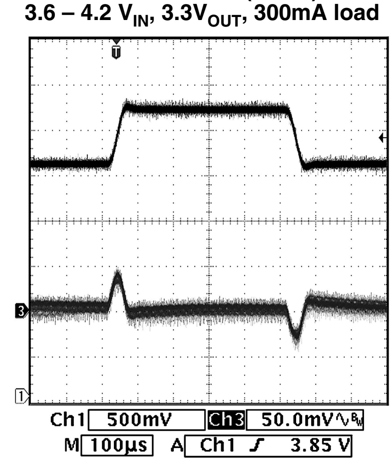
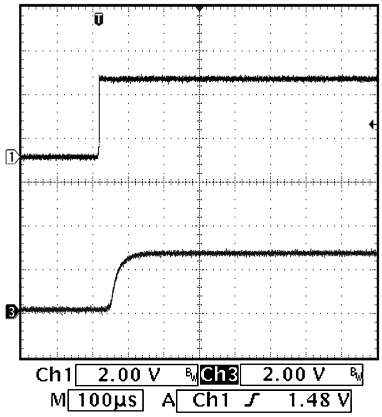
Line Transient (LDO2)
3.6 – 4.2 V_{IN}, 3.3V_{OUT}, 300mA load



30017840

Enable Start-up time (LDO1))
0-3.6 V_{IN}, 2.6 V_{OUT}, 1mA load



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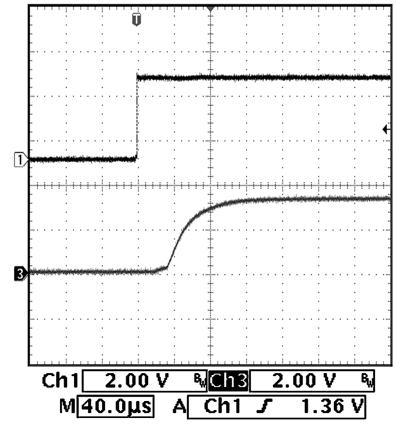
Enable Start-up time (LDO2)
0 – 3.6 V_{IN}, 3.3 V_{OUT}, 1 mA load



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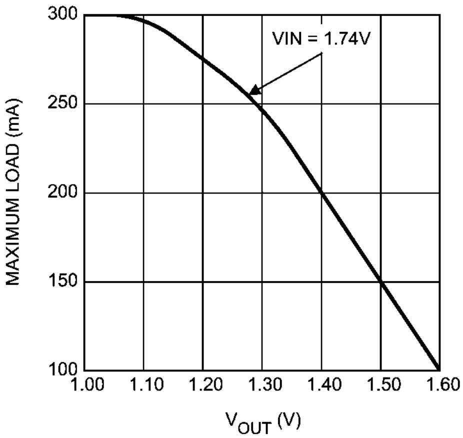
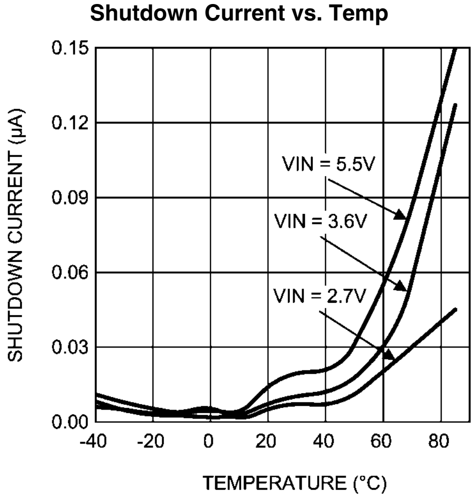
LDO Maximum Load
V_{IN} = 1.74V



30017867

Typical Performance Characteristics — Bucks

V_{IN}= 2.8V to 5.5V, T_A = 25°C



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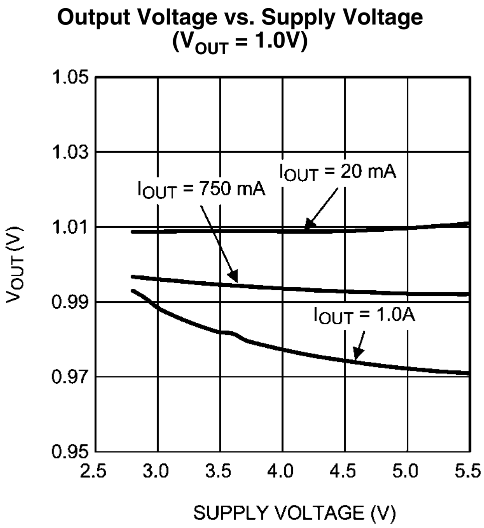

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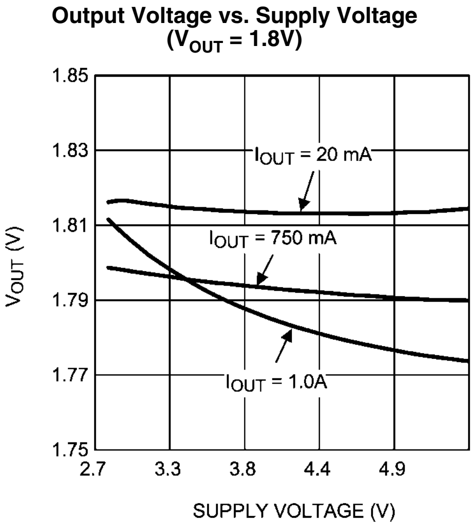

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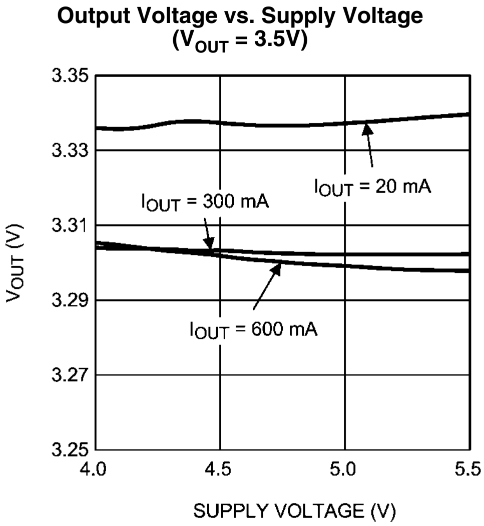
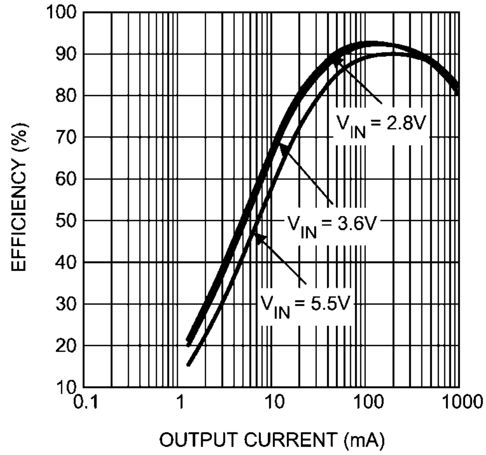


30017846

Typical Performance Characteristics — Buck1

V_{IN}= 2.8V to 5.5V, T_A = 25°C, V_{OUT} = 1.2V, 2.0V

Efficiency vs Output Current
(V_{OUT} =1.2V, L= 2.2µH —(Forced PWM mode)



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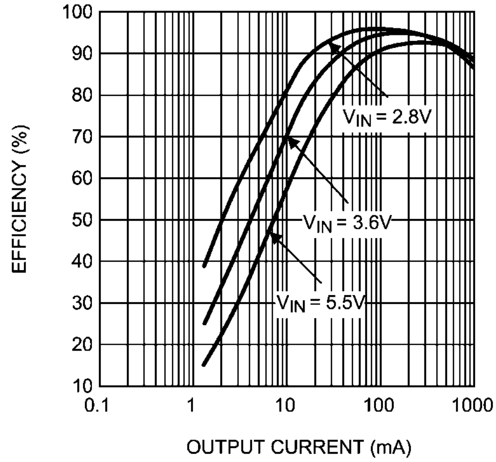
Efficiency vs Output Current
(V_{OUT} =2.0V, L= 2.2µH — Forced PWM mode)



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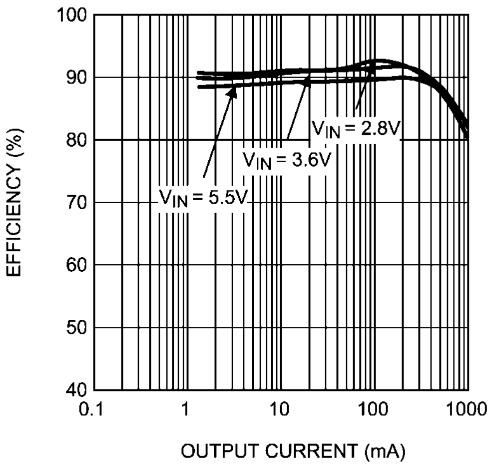
Efficiency vs Output Current
(V_{OUT} =1.2V, L= 2.2µH — PWM mode to PFM mode)



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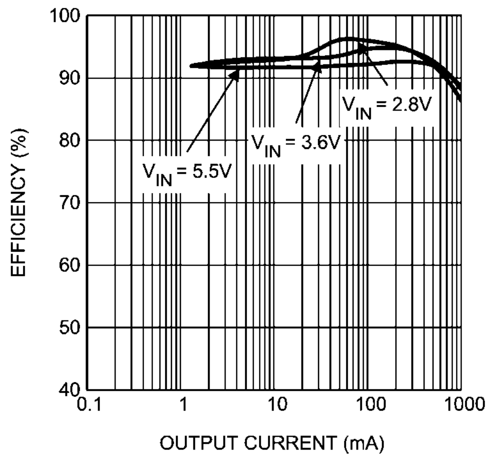
Efficiency vs Output Current
(V_{OUT} =2.0V, L= 2.2µH — PWM mode to PFM mode)



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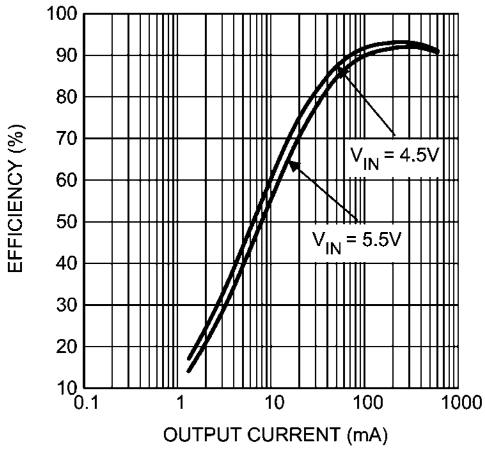
Typical Performance Characteristics — Buck2

V_{IN}= 4.5V to 5.5V, T_A = 25°C, V_{OUT} = 1.8V, 3.3V

Efficiency vs Output Current
(V_{OUT} =1.8V, L= 2.2µH —Forced PWM mode)



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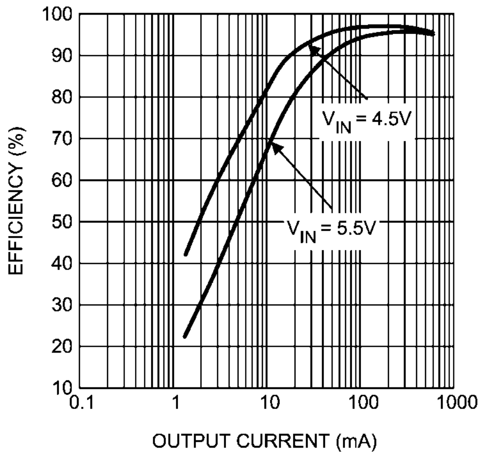
Efficiency vs Output Current
(V_{OUT} =3.3V, L= 2.2µH — Forced PWM mode)



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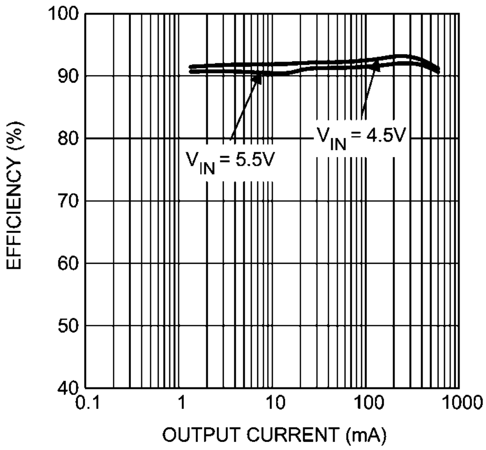
Typical Performance Characteristics — Buck2

V_{IN}= 4.3V to 5.5V, T_A = 25°C, V_{OUT} = 1.8V, 3.3V

Efficiency vs Output Current
(V_{OUT} =1.2V, L= 2.2µH — PWM mode to PFM mode)



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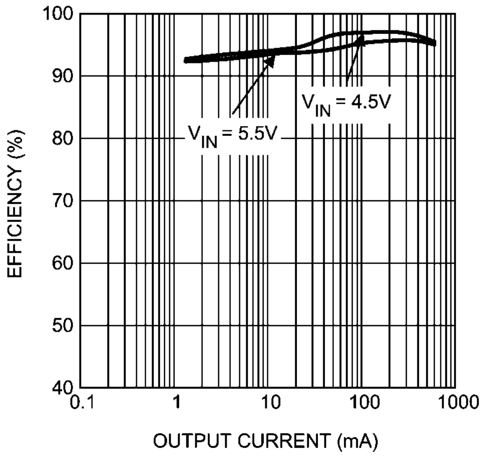
Efficiency vs Output Current
(V_{OUT} =2.0V, L= 2.2µH — PWM mode to PFM mode)



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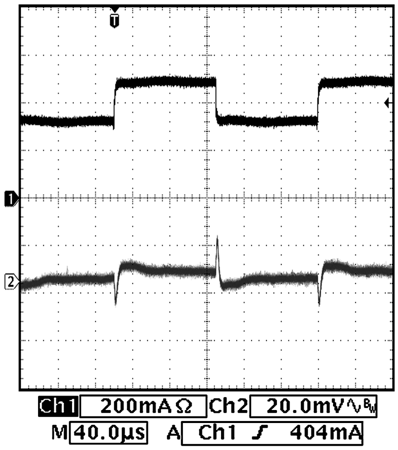
Typical Performance Characteristics — Bucks

V_{IN}= 3.6V, T_A = 25°C, V_{OUT} = 1.2V unless otherwise noted

Load Transient Response
V_{OUT} = 1.2V, I_{LOAD} = 300–500mA (PWM Mode)



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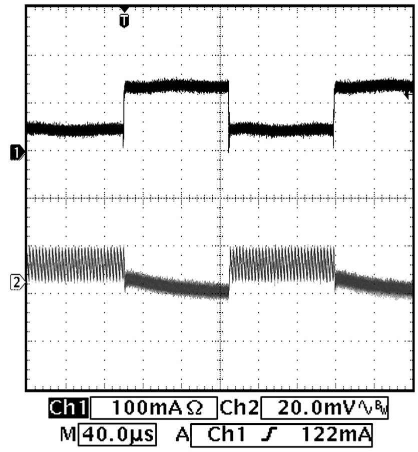
Mode Change by Load Transient
V_{OUT} = 1.2V, I_{LOAD} = 50–150mA (PFM to PWM Mode)



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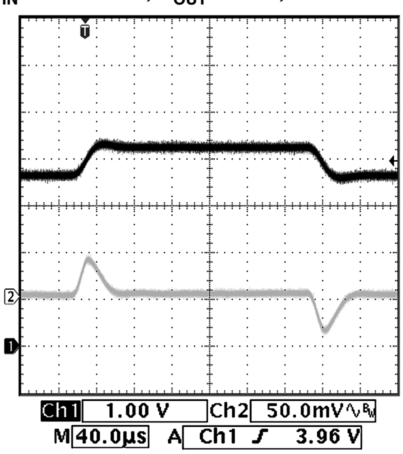
Line Transient Response
V_{IN} = 3.6 – 4.2V, V_{OUT} = 1.2V, 250mA load



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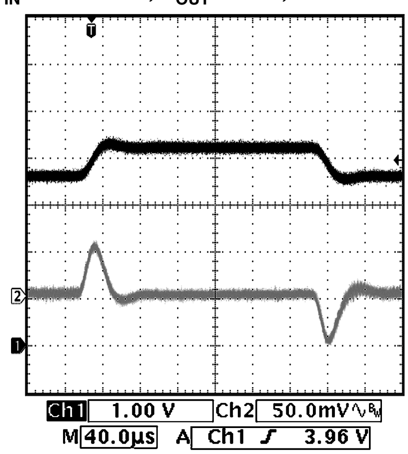
Line Transient Response
V_{IN} = 3.6 – 4.2V, V_{OUT} = 3.3V, 250 mA load



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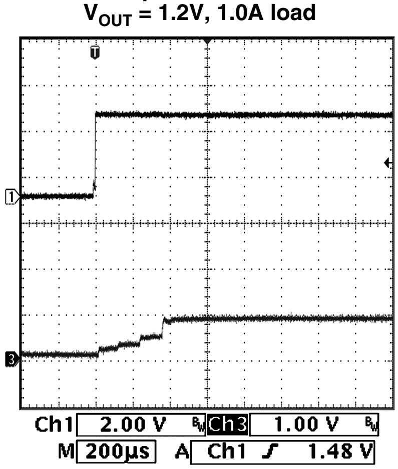
Start up into PWM Mode
V_{OUT} = 1.2V, 1.0A load



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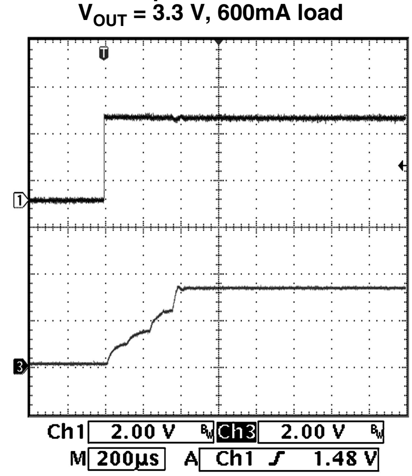
Start up into PWM Mode
V_{OUT} = 3.3 V, 600mA load



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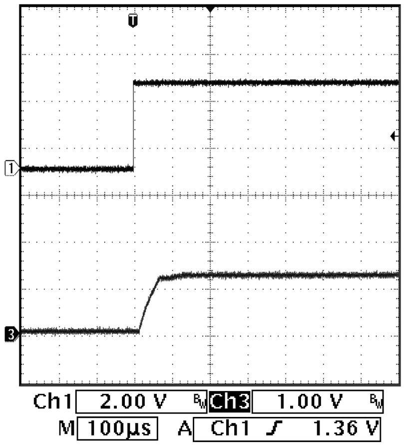
Start up into PFM Mode
V_{OUT} = 1.2V, 30mA load



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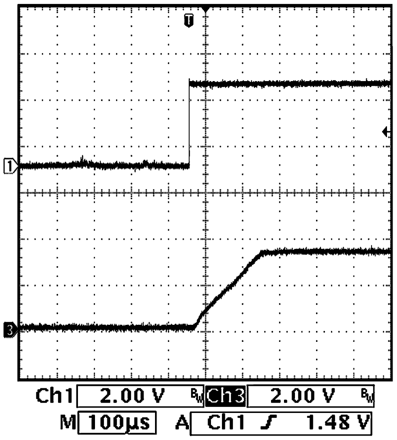
Start up into PFM Mode
V_{OUT} = 3.3V, 30mA load



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DC/DC Converters

OVERVIEW

The LP3907 supplies the various power needs of the application by means of two Linear Low Drop Regulators (LDO1 and LDO2) and two Buck converters (SW1 and SW2). The table hereunder lists the output characteristics of the various regulators.

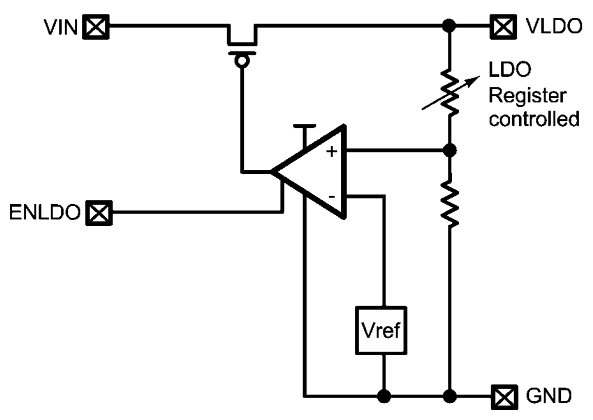
Supply Specification

Supply	Load	Output		
		V_{OUT} Range(V)	Resolution (mV)	I_{MAX} Maximum Output Current (mA)
LDO1	analog	1.0 to 3.5	100	300
LDO2	analog	1.0 to 3.5	100	300
SW1	digital	0.8 to 2.0	50	1000
SW2	digital	1.0 to 3.5	100	600

*For default values of the regulators, please consult page 3 of this datasheet.

LINEAR LOW DROPOUT REGULATORS (LDOS)

LDO1 and LDO2 are identical linear regulators targeting analog loads characterized by low noise requirements. LDO1 and LDO2 are enabled through the ENLDO pin or through the corresponding LDO1 or LDO2 control register. The output voltages of both LDOs are register programmable. The default output voltages are factory programmed during Final Test, which can be tailored to the specific needs of the system designer.



NO-LOAD STABILITY

The LDOs will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example, CMOS RAM keep-alive applications.

LDO1 AND LDO2 CONTROL REGISTERS

LDO1 and LDO2 can be configured by means of the LDO1 and LDO2 control registers. The output voltage is programmable in steps of 100mV from 1.0V to 3.5V by programming bits D4-0 in the LDO Control registers. Both LDO1 and LDO2 are enabled by applying a logic 1 to the ENLDO1 and ENLDO2 pin. Enable/disable control is also provided through enable bit of the LDO1 and LDO2 control registers. The value of the enable LDO bit in the register is logic 1 by default. The output voltage can be altered while the LDO is enabled.

SW1, SW2: Synchronous Step-Down Magnetic DC/DC Converters

FUNCTIONAL DESCRIPTION

The LP3907 incorporates two high-efficiency synchronous switching buck regulators, SW1 and SW2, that deliver a constant voltage from a single Li-Ion battery to the portable system processors. Using a voltage mode architecture with synchronous rectification, both bucks have the ability to deliver up to 1000mA and 600mA, respectively, depending on the input voltage and output voltage (voltage head room), and the inductor chosen (maximum current capability).

There are three modes of operation depending on the current required - PWM, PFM, and shutdown. PWM mode handles current loads of approximately 70mA or higher, delivering voltage precision of ±3% with 90% efficiency or better. Lighter output current loads cause the device to automatically switch into PFM for reduced current consumption (I_Q = 15µA typ.) and a longer battery life. The Standby operating mode turns off the device, offering the lowest current consumption. PWM or PFM mode is selected automatically or PWM mode can be forced through the setting of the buck control register.

Both SW1 and SW2 can operate up to a 100% duty cycle (PMOS switch always on) for low drop out control of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage.

Additional features include soft-start, under-voltage lock-out, current overload protection, and thermal overload protection.

CIRCUIT OPERATION DESCRIPTION

A buck converter contains a control block, a switching PFET connected between input and output, a synchronous rectifying NFET connected between the output and ground (BCKGND pin) and a feedback path. During the first portion of each switching cycle, the control block turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of

$$\frac{V_{IN} - V_{OUT}}{L}$$

by storing energy in a magnetic field. During the second portion of each cycle, the control block turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of

$$\frac{-V_{OUT}}{L}$$

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

PWM OPERATION

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward voltage inversely proportional to the input voltage is introduced.

INTERNAL SYNCHRONOUS RECTIFICATION

While in PWM mode, the buck uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

CURRENT LIMITING

A current limit feature allows the converter to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 1.5A for Buck1 and at 1.0A for Buck2 (typ). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

PFM OPERATION

At very light loads, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The part will automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

A. The inductor current becomes discontinuous

or

B. The peak PMOS switch current drops below the I_{MODE} level

$$(\text{Typically } I_{MODE} < 66\text{ mA} + \frac{V_{IN}}{160\Omega})$$

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between 0.8% and 1.6% (typical) above the nominal PWM output voltage. If the output voltage is below the 'low' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage exceeds the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is:

$$I_{PFM} = 66\text{ mA} + \frac{V_{IN}}{80\Omega}$$

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see figure below), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'sleep' mode is less than 30µA, which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the 'low' PFM threshold, the cycle repeats to restore the output voltage to ~1.6% above the nominal PWM output voltage.

If the load current should increase during PFM mode (see figure below) causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode.

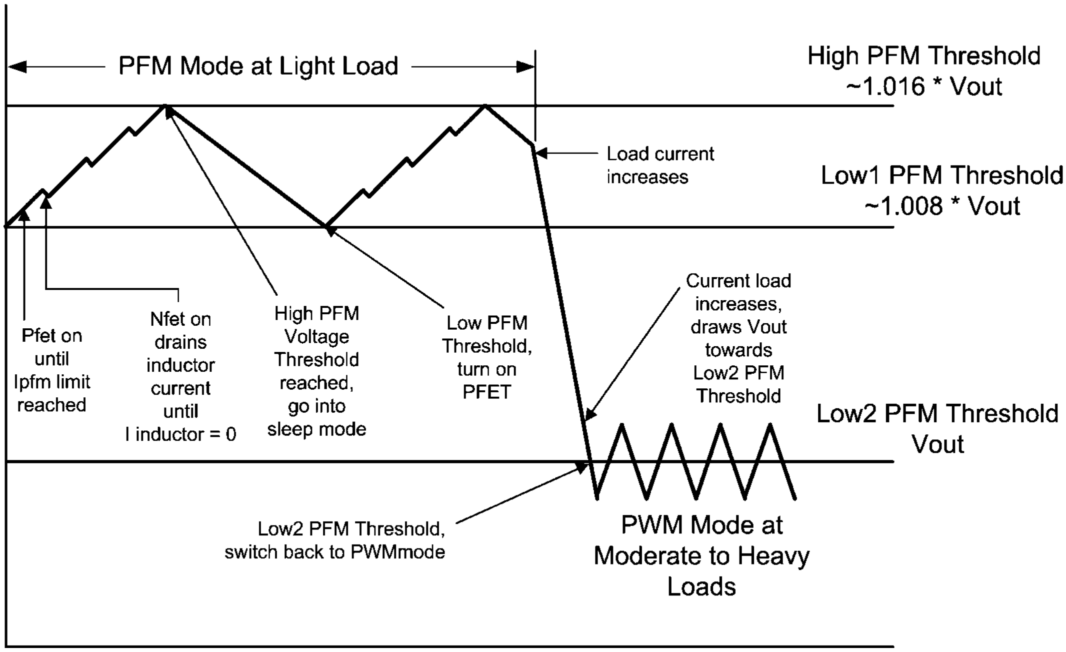
SW1, SW2 OPERATION

SW1 and SW2 have selectable output voltages ranging from 0.8V to 3.5V (typ.). Both SW1 and SW2 in the LP3907 are I²C register controlled and are enabled by default through the internal state machine of the LP3907 following a Power-On event that moves the operating mode to the Active state. (see Power On Sequence). The SW1 and SW2 output voltages revert to default values when the power on sequence has been completed. The default output voltage for each buck converter is factory programmable. (See Application Notes).

SW1, SW2 CONTROL REGISTERS

SW1, SW2 can be enabled/disabled through the corresponding control register.

The Modulation mode PWM/PFM is by default automatic and depends on the load as described above in the functional description. The modulation mode can be overridden by setting I²C bit to a logic 1 in the corresponding buck control register, forcing the buck to operate in PWM mode regardless of the load condition.



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SHUTDOWN MODE

During shutdown the PFET switch, reference, control and bias circuitry of the converters are turned off. The NFET switch will be on in shutdown to discharge the output. When the converter is enabled, soft start is activated. It is recommended to disable the converter during the system power up and under voltage conditions when the supply is less than 2.8V.

SOFT START

The soft-start feature allows the power converter to gradually reach the initial steady state operating point, thus reducing startup stresses and surges. The two LP3907 buck converters have a soft-start circuit that limits in-rush current during startup. During startup the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.8V. Soft start is implemented by increasing switch current limit in steps of 180mA, 300mA, and 720mA for Buck1; 161mA, 300mA and 536mA for Buck2 (typ. Switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up.

LOW DROPOUT OPERATION

The LP3907 can operate at 100% duty cycle (no switching; PMOS switch completely on) for low drop out support of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25mV. The minimum input voltage needed to support the output voltage is

$V_{IN, MIN} = I_{LOAD} * (R_{DSON, PFET} + R_{INDUCTOR}) + V_{OUT}$

— I_{LOAD} Load current

— $R_{DSON, PFET}$ Drain to source resistance of PFET switch in the triode region

— $R_{INDUCTOR}$ Inductor resistance

FLEXIBLE POWER SEQUENCING OF MULTIPLE POWER SUPPLIES

The LP3907 provides several options for power on sequencing. The two bucks can be individually controlled with ENSW1 and ENSW2. The two LDOs can also be individually controlled with ENLDO1 and ENLDO2.

If the user desires a set power on sequence, he can program the chip through I²C and raise EN_T from LOW to HIGH to activate the power on sequencing.

POWER UP SEQUENCING USING THE EN_T FUNCTION

EN_T assertion causes the LP3907 to emerge from Standby mode to Full Operation mode at a preset timing sequence. By default, the enables for the LDOs and Bucks (ENLDO1, ENLDO2, EN_T, ENSW1, ENSW2) are 500K internally pulled down, which causes the part to stay OFF until enabled. If the user wishes to use the preset timing sequence to power on the regulators, transition the EN_T pin from Low to High. Otherwise, simply tie the enables of each specific regulator HIGH to turn on automatically.

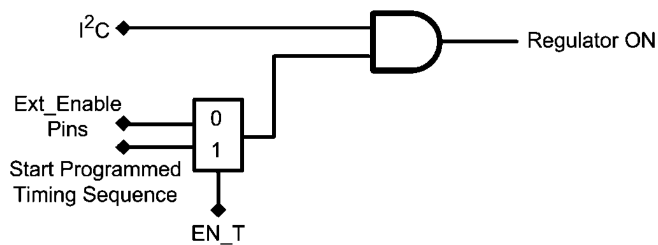
EN_T is edge triggered with rising edge signaling the chip to power on. The EN_T input is deglitched and the default is set at 1ms. As shown in the next 2 diagrams, a rising EN_T edge will start a power-on sequence, while a falling EN_T edge will start a shutdown sequence. If EN_T is high, toggling the external enables of the regulators will have no effect on the chip.

The regulators can also be programmed through I²C to turn on and off. By default, I²C enables for the regulators on ON.

The regulators are on following the pattern below:

Regulators on = (I²C enable) AND (External pin enable OR EN_T high).

Note: The EN_T power-up sequencing may also be employed immediately after V_{IN} is applied to the device. However, V_{IN} must be stable for approximately 8ms minimum before EN_T be asserted high to ensure internal bias, reference, and the Flexible POR timing are stabilized. This initial EN_T delay is necessary only upon first time device power on for power sequencing function to operate properly.



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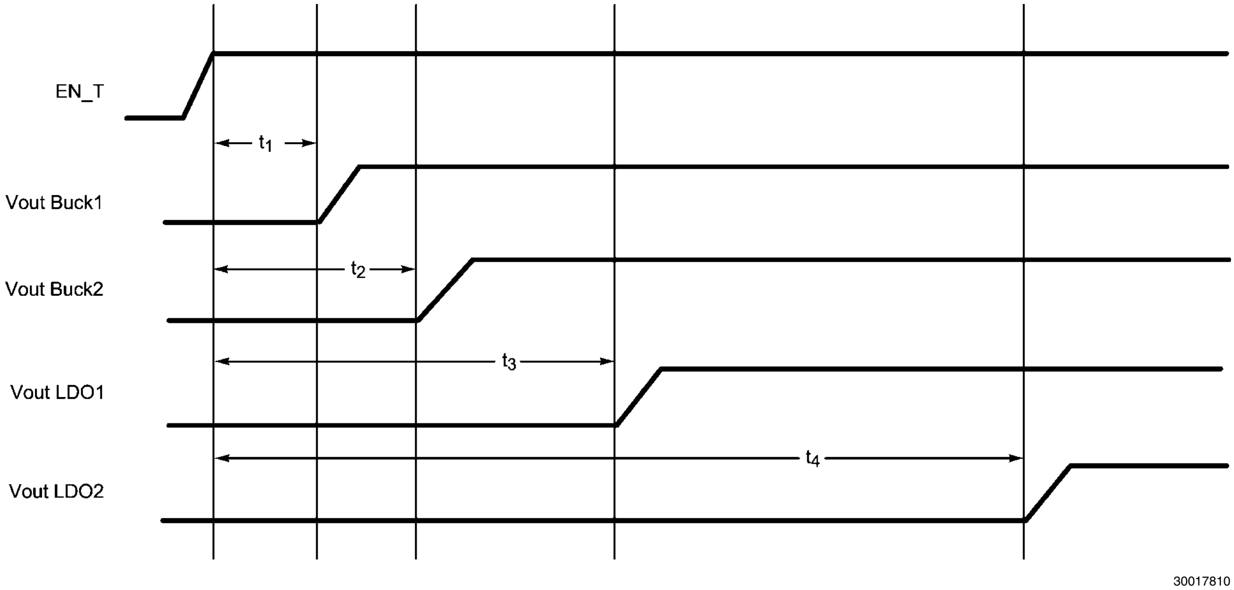
LP3907 Default Power-Up Sequence

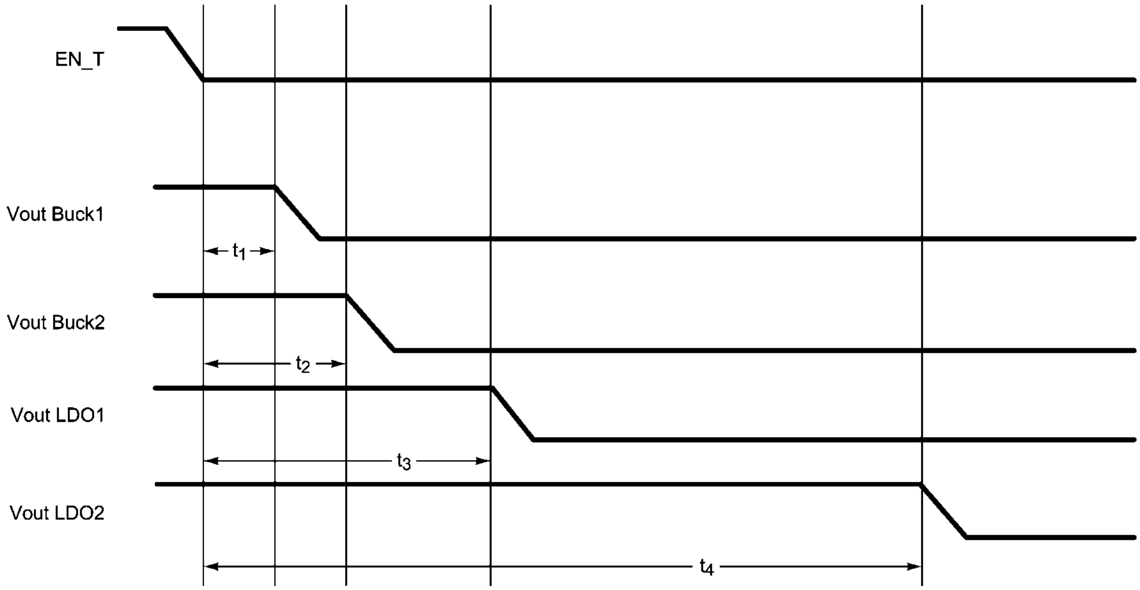


Power-On Timing Specification

Symbol	Description	Min	Typ	Max	Units
t_1	Programmable Delay from EN_T assertion to V_{CC}_Buck1 On		1.5		ms
t_2	Programmable Delay from EN_T assertion to V_{CC}_Buck2 On		2		ms
t_3	Programmable Delay from EN_T assertion to V_{CC}_LDO1 On		3		ms
t_4	Programmable Delay from EN_T assertion to V_{CC}_LDO2 On		6		ms

Note: The LP3907 default Power on delays can be reprogrammed at final test or I^2C to 1, 1.5, 2, 3, 6, or 11ms.

LP3907 Default Power-Off Sequence



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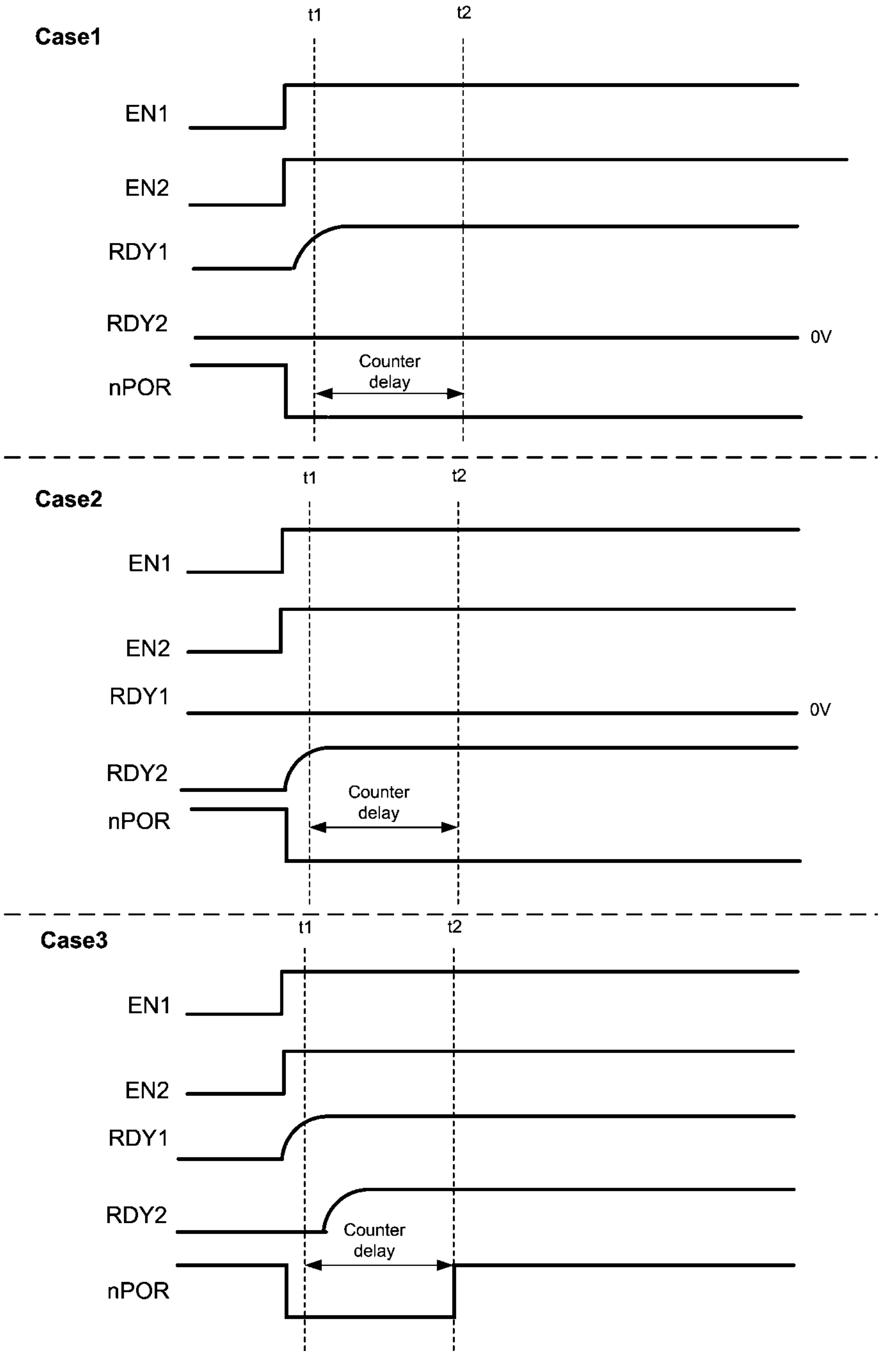
Symbol	Description	Min	Typ	Max	Units
t_1	Programmable Delay from EN_T deassertion to V_{CC}_Buck1 Off		1.5		ms
t_2	Programmable Delay from EN_T deassertion to V_{CC}_Buck2 Off		2		ms
t_3	Programmable Delay from EN_T deassertion to V_{CC}_LDO1 Off		3		ms
t_4	Programmable Delay from EN_T deassertion to V_{CC}_LDO2 Off		6		ms

Note: The LP3907 default Power on delays can be reprogrammed at final test to 0, .5, 1, 2, 5, or 10ms. Default setting is the same as the on sequence.

Flexible Power-On Reset (i.e., Power Good with delay)

The LP3907 is equipped with an internal Power-On-Reset ("POR") circuit which monitors the output voltage levels on bucks 1 and 2. The nPOR is an open drain logic output which is logic LOW when either of the buck outputs are below 91% of the rising value , or when one or both outputs fall below 82% of the desired value. The time delay between output voltage level and nPOR is enabled is (50µs, 50ms, 100ms, 200ms) 50ms by default. The system designer can choose the external pull-up resistor (i.e. 100kΩ) for the nPOR pin.

NPOR With Counter Delay

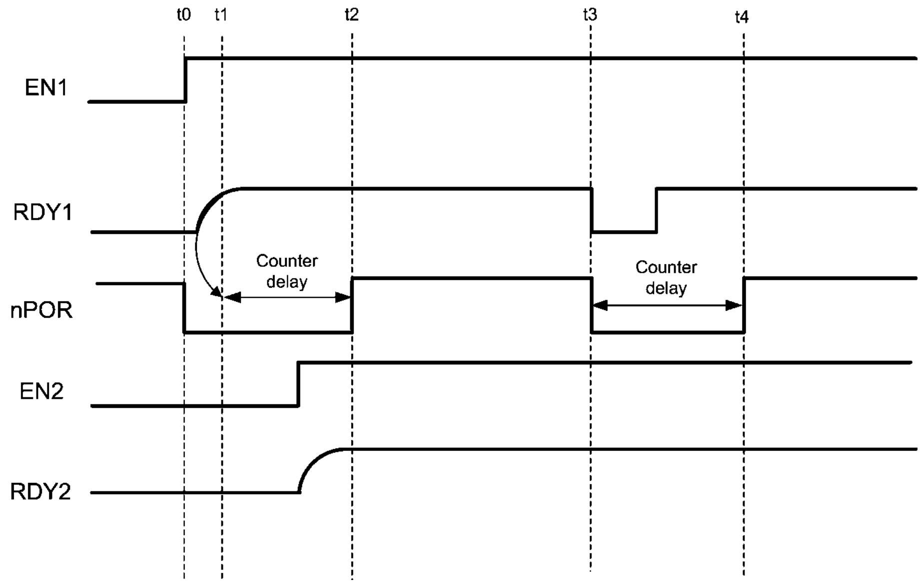


30017821

The above diagram shows the simplest application of the Power On Reset, where both switcher enables are tied together. In Case 1, EN1 causes nPOR to transition LOW and triggers the nPOR delay counter. If the power supply for Buck2 does not come on within that period, nPOR will stay LOW, indicating a power fail mode. Case 2 indicates the vice versa scenario if Buck1 supply did not come on. In both cases the nPOR remains LOW.

Case 3 shows a typical application of the Power On Reset, where both switcher enables are tied together. Even if RDY1 ramps up slightly faster than RDY2 (or vice versa), then nPOR signal will trigger a programmable delay before going HIGH, as explained below.

Faults Occurring in Counter Delay After Startup



30017881

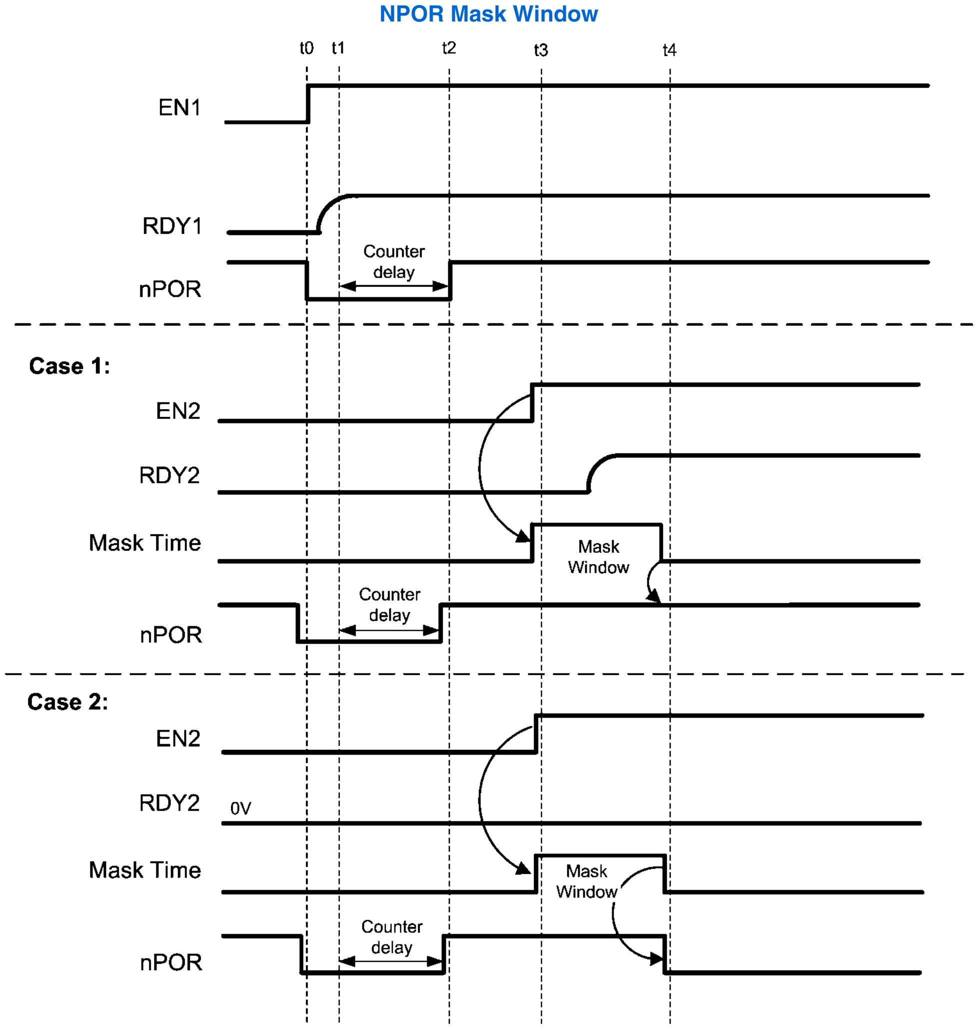
The above timing diagram details the Power good with delay with respect to the enable signals EN1, and EN2. The RDY1, RDY2 are internal signals derived from the output of two comparators. Each comparator has been trimmed as follows:

Comparator Level	Buck Supply Level
HIGH	Greater than 94%
LOW	Less than 85%

The circuits for EN1 and RDY1 is symmetrical to EN2 and RDY2, so each reference to EN1 and RDY1 will also work for EN2 and RDY2 and vice versa.

If EN1 and RDY1 signals are High at time t1, then the RDY1 signal rising edge triggers the programmable delay counter (50µs, 50ms, 100ms, 200ms). This delay forces nPOR LOW between time interval t1 and t2. nPOR is then pulled high after the programmable delay is completed. Now if EN2 and RDY2 are initiated during this interval the nPOR signal ignores this event.

If either RDY1or RDY2 were to go LOW at t3 then the programmable delay is triggered again.



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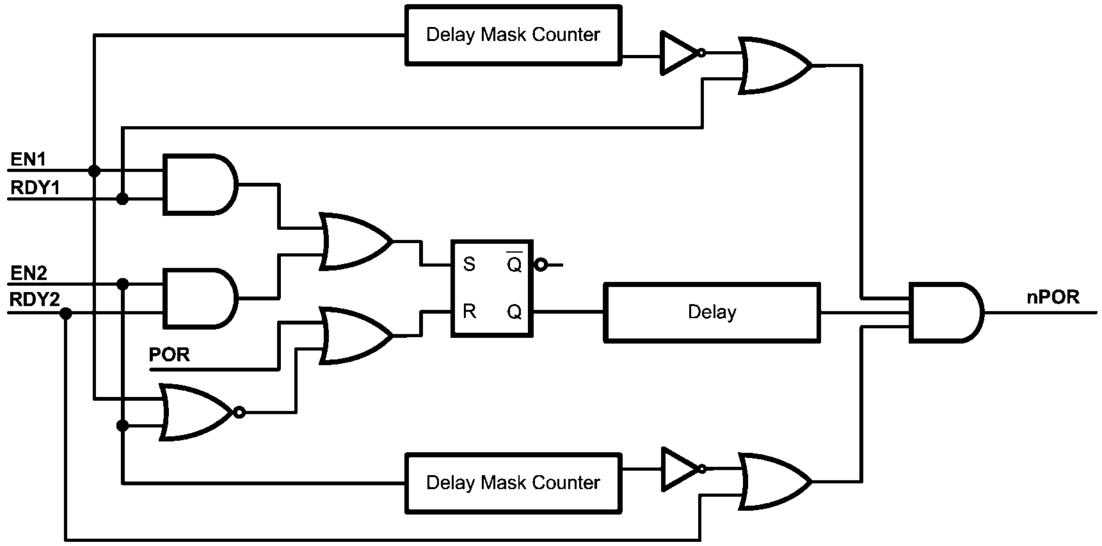
If the EN1 and RDY1 are initiated in normal operation, then nPOR is asserted and deasserted as explained above.

In Case 1, we see that case where EN2 and RDY2 are initiated after triggered programmable delay. To prevent the nPOR being asserted again, a masked window (5ms) counter delay is triggered off the EN2 rising edge. nPOR is still held HIGH for the duration of the mask, whereupon the nPOR status afterwards will depend on the status of both RDY1 and RDY2 lines.

In Case 2, we see the case where EN2 is initiated after the RDY1 triggered programmable delay, but RDY2 never goes HIGH (Buck2 never turns on). Normal operation operation of nPOR occurs wilth respect to EN1 and RDY1, and the nPOR signal is held HIGH for the duration of the mask window. We see that nPOR goes LOW after the masking window has timed out because it is now dependent on RDY1 and RDY2, where RDY2 is LOW.

Design Implementation of the Flexible Power-On Reset



30017812

An internal Power-on reset of the IC is used with EN1, and EN2 to produce a reset signal (LOW) to the delay timer nPOR. EN1 and RDY1 or EN2 and RDY2 are used to generate the set signal (HIGH) to the delay timer. S=R=1 never occurs. The mask timers are triggered off EN1 and EN2 which are gated with RDY1, and RDY2 to generate outputs to the final AND gate to generate the nPOR.

Under Voltage Lock Out

The LP3907 features an “under voltage lock out circuit”. The function of this circuit is to continuously monitor the raw input supply voltage (VINLDO12) and automatically disables the four voltage regulators whenever this supply voltage is less than 2.8VDC.

The circuit incorporates a bandgap based circuit that establishes the reference used to determine the 2.8VDC trip point for a V_{IN} OK – Not OK detector. This V_{IN} OK signal is then used to gate the enable signals to the four regulators of the LP3907. When VINLDO12 is greater than 2.8VDC the four enables control the four regulators, when VINLDO12 is less than 2.8VDC the four regulators are disabled by the V_{IN} detector being in the “Not OK” state. The circuit has built in hysteresis to prevent chattering occurring.

I²C Compatible Serial Interface

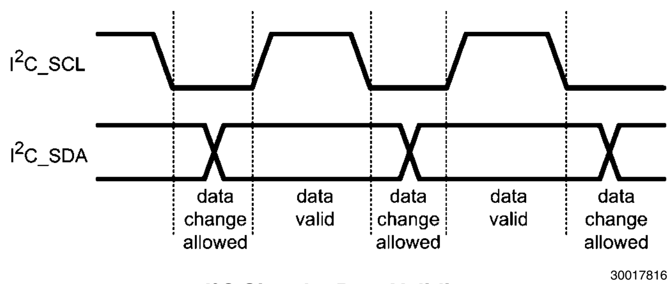
I²C SIGNALS

The LP3907 features an I²C compatible serial interface, using two dedicated pins: SCL and SDA for I²C clock and data respectively. Both signals need a pull-up resistor according to the I²C specification. The LP3907 interface is an I²C slave that is clocked by the incoming SCL clock.

Signal timing specifications are according to the I²C bus specification. The maximum bit rate is 400kbit/s. See I²C specification from Philips for further details.

I²C DATA VALIDITY

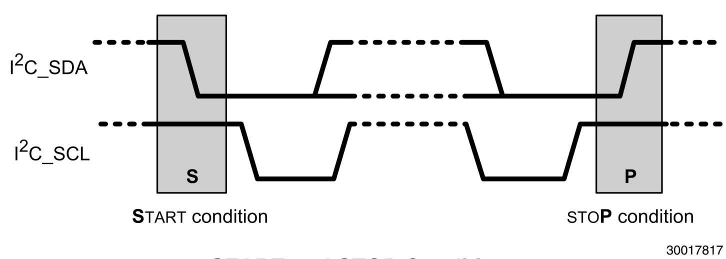
The data on the SDA line must be stable during the HIGH period of the clock signal (SCL), e.g.- the state of the data line can only be changed when CLK is LOW.



I²C Signals: Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while the SCL is HIGH. The ²C master always generates START and STOP bits. The I2C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



START and STOP Conditions

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledged related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying acknowledgement. A receiver which has been addressed must generate an acknowledgement (“ACK”) after each byte has been received.

After the START condition, the I2C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). Please note that according to industry I2C standards for 7-bit addresses, the MSB of an 8-bit address is removed, and communication actually starts with the 7th most significant bit. For the eighth bit (LSB), a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

The LP3907 has factory-programmed I2C addresses. The LLP chip has a chip address of 60'h, while the micro SMD chip has a chip address of 61'h.

MSB							LSB
ADR6 bit7	ADR5 bit6	ADR4 bit5	ADR3 bit4	ADR2 bit3	ADR1 bit2	ADR0 bit1	R/W bit0
1	1	0	0	0	0	0	

← I2C SLAVE address (chip address) →

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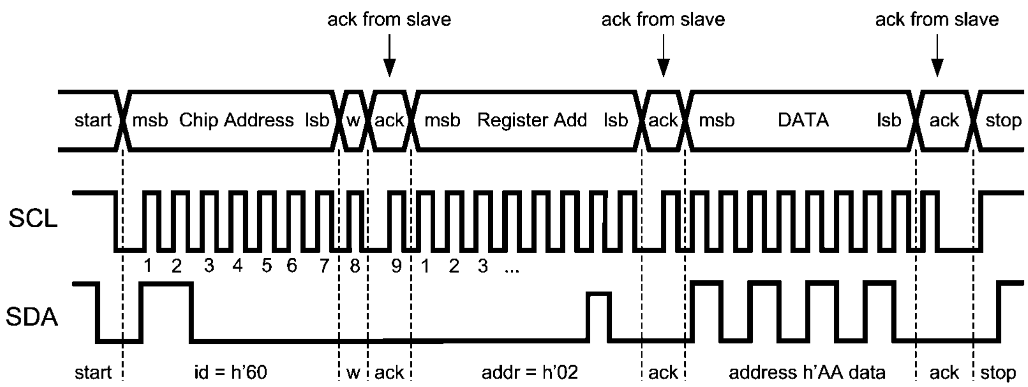
I2C Chip Address (see note above)



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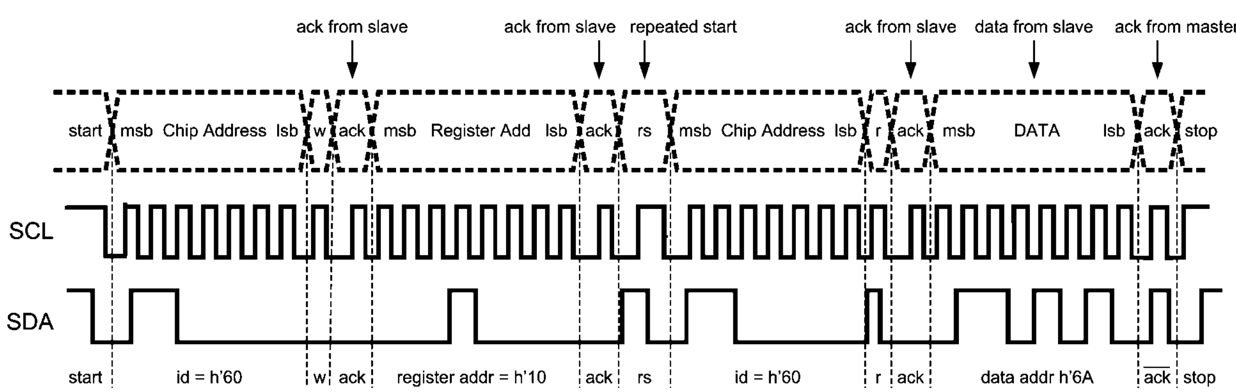
w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled down by either master or slave)
rs = repeated start
id = LP3907 LLP chip address: **0x60**; micro SMD chip address: **0x61**

I2C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.



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I2C Read Cycle

LP3907 Control Registers

Register Address	Register Name	Read/ Write	Register Description
0x02	ICRA	R	Interrupt Status Register A
0x07	SCR1	R/W	System Control 1 Register
0x10	BKLDOEN	R/W	Buck and LDO Output Voltage Enable Register
0x11	BKLDOSR	R	Buck and LDO Output Voltage Status Register
0x20	VCCR	R/W	Voltage Change Control Register 1
0x23	B1TV1	R/W	Buck1 Target Voltage 1 Register
0x24	B1TV2	R/W	Buck1 Target Voltage 2 Register
0x25	B1RC	R/W	Buck1 Ramp Control
0x29	B2TV1	R/W	Buck2 Target Voltage 1 Register
0x2A	B2TV2	R/W	Buck2 Target Voltage 2 Register
0x2B	B2RC	R/W	Buck2 Ramp Control
0x38	BFCR	R/W	Buck Function Register
0x39	LDO1VCR	R/W	LDO1 Voltage control Registers
0x3A	LDO2VCR	R/W	LDO2 Voltage control Registers

INTERRUPT STATUS REGISTER (ISRA) 0X02

This register informs the System Engineer of the temperature status of the chip.

	D7-2	D1	D0
Name	—	Temp 125°C	—
Access	—	R	—
Data	Reserved	Status bit for thermal warning PMIC T>125°C 0 – PMIC Temp. < 125°C 1 – PMIC Temp. > 125°C	Reserved
Reset	0	0	0

CONTROL 1 REGISTER (SCR1) 0X07

This register allows the user to select the preset delay sequence for power-on timing, to switch between PFM and PWM mode for the bucks, and also to select between an internal and external clock for the bucks.

	D7	D6-4	D3	D2	D1	D0
Name	—	EN_DLY	—	FPWM2	FPWM1	ECEN
Access	—	R/W	—	R/W	R/W	R/W
Data	Reserved	Selects the preset delay sequence from EN_T assertion (shown below)	Reserved	Buck2 PWM /PFM Mode select 0 – Auto Switch PFM - PWM operation 1 – PWM Mode Only	Buck 1 PWM /PFM Mode select 0 – Auto Switch PFM - PWM operation 1 – PWM Mode Only	Reserved
Reset	0	Factory-Programmed Default	1	Factory-Programmed Default	Factory-Programmed Default	0

EN_DLY PRESET DELAY SEQUENCE AFTER EN_T ASSERTION

EN_DLY<2:0>	Delay (ms)			
	Buck1	Buck2	LDO1	LDO2
000	1	1	1	1
001	1	1.5	2	2
010	1.5	2	3	6
011	1.5	2	1	1
100	1.5	2	3	6
101	1.5	1.5	2	2
110	3	2	1	1.5
111	2	3	6	11

BUCK AND LDO OUTPUT VOLTAGE ENABLE REGISTER (BKLDOEN) – 0X10

This register controls the enables for the Bucks and LDOs.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	—	LDO2EN	—	LDO1EN	—	BK2EN	—	BK1EN
Access	—	R/W	—	R/W	—	R/W	—	R/W
Data	Reserved	0 – Disable 1 – Enable	Reserved	0 – Disable 1 – Enable	Reserved	0 – Disable 1 – Enable	Reserved	0 – Disable 1 – Enable
Reset	0	1	1	1	0	1	0	1

BUCK AND LDO STATUS REGISTER (BKLDOSR) – 0X11

This register monitors whether the Bucks and LDOs meet the voltage output specifications.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	BKS_OK	LDOS_OK	LDO2_OK	LDO1_OK	—	BK2_OK	—	BK1_OK
Access	R	R	R	R	—	R	—	R
Data	0 – Buck 1-2 Not Valid 1 – Bucks Valid	0 – LDO 1-2 Not Valid 1 – LDOs Valid	0 – LDO2 Not Valid 1 – LDO2 Valid	0 – LDO1 Not Valid 1 – LDO1 Valid	Reserve d	0 – Buck2 Not Valid 1 – Buck2 Valid	Reserve d	0 – Buck1 Not Valid 1 – Buck1 Valid
Reset	0	0	0	0	0	0	0	0

BUCK VOLTAGE CHANGE CONTROL REGISTER 1 (VCCR) – 0X20

This register selects and controls the output target voltages for the buck regulators.

	D7-6	D5	D4	D3-2	D1	D0
Name	—	B2VS	B2GO	—	B1VS	B1GO
Access	—	R/W	R/W	—	R/W	R/W
Data	Reserved	Buck2 Target Voltage Select 0 – B2VT1 1 – B2VT2	Buck2 Voltage Ramp CTRL 0 – Hold 1 – Ramp to B2VS selection	Reserved	Buck1 Target Voltage Select 0 – B1VT1 1 – B1VT2	Buck1 Voltage Ramp CTRL 0 – Hold 1 – Ramp to B1VS selection
Reset	00	0	0	00	0	0

BUCK1 TARGET VOLTAGE 1 REGISTER (B1TV1) – 0X23

This register allows the user to program the output target voltage of Buck1.

	D7-5	D4-0	
Name	—	BK1_VOUT1	
Access	—	R/W	
Data	Reserved	Buck1 Output Voltage (V)	
		5'h00	Ext Ctrl
		5'h01	0.80
		5'h02	0.85
		5'h03	0.90
		5'h04	0.95
		5'h05	1.00
		5'h06	1.05
		5'h07	1.10
		5'h08	1.15
		5'h09	1.20
		5'h0A	1.25
		5'h0B	1.30
		5'h0C	1.35
		5'h0D	1.40
		5'h0E	1.45
		5'h0F	1.50
		5'h10	1.55
		5'h11	1.60
		5'h12	1.65
		5'h13	1.70
		5'h14	1.75
		5'h15	1.80
		5'h16	1.85
		5'h17	1.90
		5'h18	1.95
		5'h19	2.00
		5'h1A–5'h1F	2.00
Reset	000	Factory-Programmed Default	

* If using Ext Ctrl, contact National Sales for support.

BUCK1 TARGET VOLTAGE 2 REGISTER (B1TV2) – 0X24

This register allows the user to program the output target voltage of Buck1.

	D7-5	D4-0	
Name	—	BK1_VOUT2	
Access	—	R/W	
Data	Reserved	Buck1 Output Voltage (V)	
		5'h00	Ext Ctrl
		5'h01	0.80
		5'h02	0.85
		5'h03	0.90
		5'h04	0.95
		5'h05	1.00
		5'h06	1.05
		5'h07	1.10
		5'h08	1.15
		5'h09	1.20
		5'h0A	1.25
		5'h0B	1.30
		5'h0C	1.35
		5'h0D	1.40
		5'h0E	1.45
		5'h0F	1.50
		5'h10	1.55
		5'h11	1.60
		5'h12	1.65
		5'h13	1.70
		5'h14	1.75
		5'h15	1.80
		5'h16	1.85
		5'h17	1.90
		5'h18	1.95
		5'h19	2.00
		5'h1A–5'h1F	2.00
Reset	000	Factory-Programmed Default	

BUCK1 RAMP CONTROL REGISTER (B1RC) - 0x25

This register allows the user to program the rate of change between the target voltages of Buck1.

	D7	D6-4	D3-0	
Name	- - - -	- - - -	B1RS	
Access	- - - -	- - - -	R/W	
Data	Reserved	Reserved	Data Code	Ramp Rate mV/us
			4h'0	Instant
			4h'1	1
			4h'2	2
			4h'3	3
			4h'4	4
			4h'5	5
			4h'6	6
			4h'7	7
			4h'8	**8**
			4h'9	9
			4h'A	10
			4h'B - 4h'F	10
Reset	0	010	1000	

BUCK2 TARGET VOLTAGE 1 REGISTER (B2TV1) – 0X29

This register allows the user to program the output target voltage of Buck2.

	D7-5	D4-0	
Name	—	BK2_VOUT1	
Access	—	R/W	
Data	Reserved	Buck2 Output Voltage (V)	
		5’h00	Ext Ctrl
		5’h01	1.0
		5’h02	1.1
		5’h03	1.2
		5’h04	1.3
		5’h05	1.4
		5’h06	1.5
		5’h07	1.6
		5’h08	1.7
		5’h09	1.8
		5’h0A	1.9
		5’h0B	2.0
		5’h0C	2.1
		5’h0D	2.2
		5’h0E	2.4
		5’h0F	2.5
		5’h10	2.6
		5’h11	2.7
		5’h12	2.8
		5’h13	2.9
		5’h14	3.0
		5’h15	3.1
		5’h16	3.2
		5’h17	3.3
		5’h18	3.4
		5’h19	3.5
		5’h1A–5’h1F	3.5
Reset	000	Factory-Programmed Default	

*If using Ext Ctrl, contact National Sales for support.

BUCK2 TARGET VOLTAGE 2 REGISTER (B2TV2) – 0X2A

This register allows the user to program the output target voltage of Buck2.

	D7-5	D4-0	
Name	—	BK2_VOUT2	
Access	—	R/W	
Data	Reserved	Buck2 Output Voltage (V)	
		5’h00	Ext Ctrl
		5’h01	1.0
		5’h02	1.1
		5’h03	1.2
		5’h04	1.3
		5’h05	1.4
		5’h06	1.5
		5’h07	1.6
		5’h08	1.7
		5’h09	1.8
		5’h0A	1.9
		5’h0B	2.0
		5’h0C	2.1
		5’h0D	2.2
		5’h0E	2.4
		5’h0F	2.5
		5’h10	2.6
		5’h11	2.7
		5’h12	2.8
		5’h13	2.9
		5’h14	3.0
		5’h15	3.1
		5’h16	3.2
		5’h17	3.3
		5’h18	3.4
		5’h19	3.5
		5’h1A–5’h1F	3.5
Reset	000	Factory-Programmed Default	

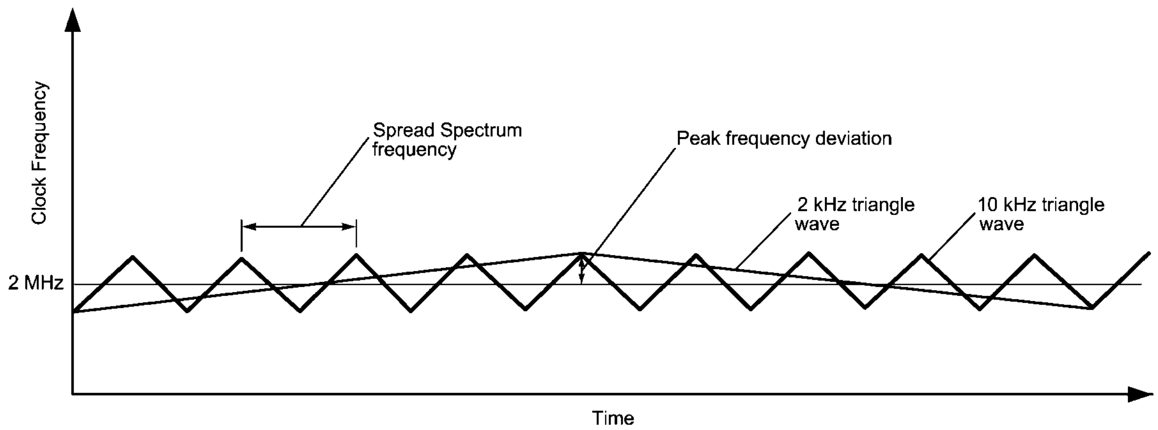
BUCK2 RAMP CONTROL REGISTER (B2RC) - 0x2B

This register allows the user to program the rate of change between the target voltages of Buck2.

	D7	D6-4	D3-0	
Name	- - - -	- - - -	B2RS	
Access	- - - -	- - - -	R/W	
Data	Reserved	Reserved	Data Code	Ramp Rate mV/us
			4h'0	Instant
			4h'1	1
			4h'2	2
			4h'3	3
			4h'4	4
			4h'5	5
			4h'6	6
			4h'7	7
			4h'8	**8**
			4h'9	9
			4h'A	10
			4h'B - 4h'F	10
Reset	0	010	1000	

BUCK FUNCTION REGISTER (BFCR) – 0x38

This register allows the Buck switcher clock frequency to be spread across a wider range, allowing for less Electro-magnetic Interference (EMI). The spread spectrum modulation frequency refers to the rate at which the frequency ramps up and down, centered at 2MHz.



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This register also allows dynamic scaling of the nPOR Delay Timing. The LP3907 is equipped with an internal Power-On-Reset ("POR") circuit which monitors the output voltage levels on the buck regulators, allowing the user to more actively monitor the power status of the chip.

The Under Voltage Lock-Out feature continuously monitor the raw input supply voltage (VINLDO12) and automatically disables the four voltage regulators whenever this supply voltage is less than 2.8VDC. This prevents the user from damaging the power source (i.e. battery), but can be disabled if the user wishes.

Note that if the supply to VDD_M is close to 2.8V with a heavy load current on the regulators, the chip is in danger of powering down due to UVLO. If the user wishes to keep the chip active under those conditions, enable the "Bypass UVLO" feature.

	D7-2	D4	D3	D1	D0
Name	—	BP_UVLO	TPOR	BK_SLOMOD	BK_SSEN
Access	—	R/W	R/w	R/W	R/W
Data	Reserved	Bypass UVLO monitoring 0 - Allow UVLO 1 - Disable UVLO	nPOR Delay Timing 00 - 50µs 01 - 50ms 10 - 100ms 11 - 200ms	Buck Spread Spectrum Modulation 0 – 10 kHz triangular wave 1 – 2 kHz triangular wave	Spread Spectrum Function Output 0 – Disabled 1 – Enabled
Reset	000	Factory-Programmed Default	01	1	0

LDO1 CONTROL REGISTER (LDO1VCR) – 0X39

This register allows the user to program the output target voltage of LDO 1.

For “JJ11” voltage options LDO1 has a fixed output voltage of 2.85V.

	D7-5	D4-0	
Name	—	LDO1_OUT	
Access	—	R/W	
Data	Reserved	LDO1 Output voltage (V)	
		5’h00	1.0
		5’h01	1.1
		5’h02	1.2
		5’h03	1.3
		5’h04	1.4
		5’h05	1.5
		5’h06	1.6
		5’h07	1.7
		5’h08	1.8
		5’h09	1.9
		5’h0A	2.0
		5’h0B	2.1
		5’h0C	2.2
		5’h0D	2.3
		5’h0E	2.4
		5’h0F	2.5
		5’h10	2.6
		5’h11	2.7
		5’h12	2.8
		5’h13	2.9
		5’h14	3.0
		5’h15	3.1
		5’h16	3.2
		5’h17	3.3
		5’h18	3.4
		5’h19	3.5
		5’h1A–5’h1F	3.5
Reset	000	Factory-Programmed Default	

LDO2 CONTROL REGISTER (LDO2VCR) – 0X3A

This register allows the user to program the output target voltage of LDO 2.

For “JJ11” voltage options LDO2 has a fixed output voltage of 2.85V.

	D7-5	D4-0	
Name	—	LDO2_OUT	
Access	—	R/W	
Data	Reserved	LDO2 Output voltage (V)	
		5’h00	1.0
		5’h01	1.1
		5’h02	1.2
		5’h03	1.3
		5’h04	1.4
		5’h05	1.5
		5’h06	1.6
		5’h07	1.7
		5’h08	1.8
		5’h09	1.9
		5’h0A	2.0
		5’h0B	2.1
		5’h0C	2.2
		5’h0D	2.3
		5’h0E	2.4
		5’h0F	2.5
		5’h10	2.6
		5’h11	2.7
		5’h12	2.8
		5’h13	2.9
		5’h14	3.0
		5’h15	3.1
		5’h16	3.2
		5’h17	3.3
		5’h18	3.4
		5’h19	3.5
		5’h1A–5’h1F	3.5
Reset	000	Factory-Programmed Default	

Application Notes

ANALOG POWER SIGNAL ROUTING

All power inputs should be tied to the main VDD source (i.e. battery), unless the user wishes to power it from another source. (i.e. external LDO output).

The analog VDD inputs power the internal bias and error amplifiers, so they should be tied to the main VDD. The analog VDD inputs must have an input voltage between 2.8 and 5.5V, as specified in the Electrical Characteristics Section in the front of the datasheet.

The other V_{IN}s (V_{IN}LDO1, V_{IN}LDO2, $V_{IN}1$, $V_{IN}2$) can actually have inputs lower than 2.8V, as long as it's higher than the programmed output (+0.3V, to be safe).

The analog and digital grounds should be tied together outside of the chip to reduce noise coupling.

COMPONENT SELECTION

Inductors for SW1 and SW2

There are two main considerations when choosing an inductor; the inductor should not saturate and the inductor current ripple is small enough to achieve the desired output voltage ripple. Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25ºC, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

There are two methods to choose the inductor saturation current rating:

Method 1:

The saturation current is greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as follows:

$$I_{sat} > I_{outmax} + I_{ripple}$$

$$\text{where} \quad I_{ripple} = \left(\frac{1}{f}\right) \times \left(\frac{V_{IN} - V_{OUT}}{2L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right)$$

I_{RIPPLE}: Average to peak inductor current

I_{OUTMAX}: Maximum load current

V_{IN}: Maximum input voltage to the buck

L: Min inductor value including worse case tolerances (30% drop can be considered for method 1)

f: Minimum switching frequency (1.6 MHz)

V_{OUT}: Buck Output voltage

Method 2:

A more conservative and recommended approach is to choose an inductor that has saturation current rating greater than the maximum current limit of 1250mA for Buck1 and 1750mA for Buck2.

Given a peak-to-peak current ripple (I_{PP}) the inductor needs to be at least

$$L \geq \left(\frac{V_{IN} - V_{OUT}}{I_{PP}}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f}\right)$$

Inductor	Value	Unit	Description	Notes
$L_{SW}1,2$	2.2	µH	SW1,2 inductor	D.C.R. 70mΩ

External Capacitors

The regulators on the LP3907 require external capacitors for regulator stability. These are specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

LDO CAPACITOR SELECTION

Input Capacitor

An input capacitor is required for stability. It is recommended that a 1.0µF capacitor be connected between the LDO input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge currents when connected to a low impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain approximately 1.0µF over the entire operating temperature range.

Output Capacitor

The LDOs on the LP3907 are designed specifically to work with very small ceramic output capacitors. A 0.47µF ceramic capacitor (temperature types Z5U, Y5V or X7R) with ESR between 5 mΩ to 500mΩ, is suitable in the application circuit.

It is also possible to use tantalum or film capacitors at the device output, C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost.

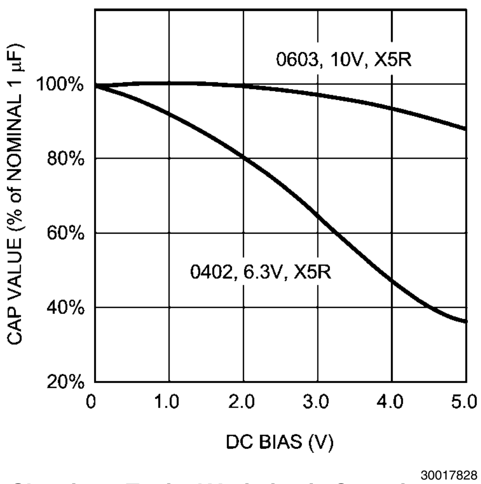
The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

Capacitor Characteristics

The LDOs are designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47µF to 4.7µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1.0µF ceramic capacitor is in the range of 20mΩ to 40mΩ, which easily meets the ESR requirement for stability for the LDOs.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependent on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, below is typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot.



Graph Showing a Typical Variation in Capacitance vs. DC Bias

As shown in the graph, increasing the DC Bias condition can result in the capacitance value that falls below the minimum value given in the recommended capacitor specifications table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

Input Capacitor Selection for SW1 and SW2

A ceramic input capacitor of 10µF, 6.3V is sufficient for the magnetic dc/dc converters. Place the input capacitor as close as possible to the input of the device. A large value may be used for improved input voltage filtering. The recommended capacitor types are X7R or X5R. Y5V type capacitors should not be used. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. The input filter capacitor supplies current to the PFET switch of the dc/dc converter in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR (Equivalent Series Resistance) provides the best noise filtering of the input voltage spikes due to fast current transients. A capacitor with sufficient ripple current rating should be selected. The Input current ripple can be calculated as:

$$I_{rms} = I_{outmax} \sqrt{\frac{V_{OUT}}{V_{IN}}\left(1 + \frac{r^2}{12}\right)}$$

$$\text{where} \quad r = \frac{(V_{in} - V_{out}) \times V_{out}}{L \times f \times I_{outmax} \times V_{in}}$$

The worse case is when $V_{IN} = 2V_{OUT}$.

Output Capacitor Selection for SW1, SW2

A 10µF, 6.3V ceramic capacitor should be used on the output of the sw1 and sw2 magnetic dc/dc converters. The output capacitor needs to be mounted as close as possible to the output of the device. A large value may be used for improved input voltage filtering. The recommended capacitor types are X7R or X5R. Y5V type capacitors should not be used. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and DC bias curves should be requested from them and analyzed as part of the capacitor selection process.

The output filter capacitor of the magnetic dc/dc converter smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESD to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its ESR and can be calculated as follows:

$$V_{pp\text{-}c} = \frac{I_{ripple}}{4 \times f \times C}$$

Voltage peak-to-peak ripple due to ESR can be expressed as follows:

$$V_{PP-ESR} = 2 \times I_{RIPPLE} \times R_{ESR}$$

Because the $V_{PP\text{-}C}$ and $V_{PP\text{-}ESR}$ are out of phase, the rms value can be used to get an approximate value of the peak-to-peak ripple:

$$V_{pp\text{-}rms} = \sqrt{V_{pp\text{-}c}^{\,2} + V_{pp\text{-}esr}^{\,2}}$$

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}). The R_{ESR} is frequency dependent as well as temperature dependent. The R_{ESR} should be calculated with the applicable switching frequency and ambient temperature.

Capacitor	Min Value	Unit	Description	Recommended Type
C_{LDO1}	0.47	µF	LDO1 output capacitor	Ceramic, 6.3V, X5R
C_{LDO2}	0.47	µF	LDO2 output capacitor	Ceramic, 6.3V, X5R
C_{SW1}	10.0	µF	SW1 output capacitor	Ceramic, 6.3V, X5R
C_{SW2}	10.0	µF	SW2 output capacitor	Ceramic, 6.3V, X5R

I²C Pullup Resistor

Both SDA and SCL terminals need to have pullup resistors connected to VINLDO12 or to the power supply of the I²C master. The values of the pull-up resistors (typ. ~1.8kΩ) are determined by the capacitance of the bus. Too large of a resistor combined with a given bus capacitance will result in a rise time that would violate the max. rise time specification. A too small resistor will result in a contention with the pull-down transistor on either slave(s) or master.

Operation without I²C Interface

Operation of the LP3907 without the I²C interface is possible if the system can operate with default values for the LDO and Buck regulators. (Read below: Factory programmable options). The I²C-less system must rely on the correct default output values of the LDO and Buck converters.

Factory Programmable Options

The following options are EPROM programmed during final test of the LP3907. The system designer that needs specific options is advised to contact the local National Semiconductor sales office.

Factory programmable options	Current value
Enable delay for power on	code 010 (see Control 1 register section)
SW1 ramp speed	8 mV/µs
SW2 ramp speed	8 mV/µs

The I²C Chip ID address is offered as a metal mask option. The current address for the LLP chip equals **0x60**, while the address for the micro SMD chip is **0x61**.

HIGH V_{IN} HIGH-LOAD OPERATION

Additional information is provided when the IC is operated at extremes of V_{IN} and regulator loads. These are described in terms of the Junction temperature and, Buck output ripple management.

JUNCTION TEMPERATURE

The maximum junction temperature $T_{J\text{-}MAX\text{-}OP}$ of 125°C of the IC package.

The following equations demonstrate junction temperature determination, ambient temperature $T_{A\text{-}MAX}$ and Total chip power must be controlled to keep T_J below this maximum:

$T_{J\text{-}MAX\text{-}OP} = T_{A\text{-}MAX} + (\theta_{JA})$ [°C/ Watt] * $(P_{D\text{-}MAX})$ [Watts]

Total IC power dissipation $P_{D\text{-}MAX}$ is the sum of the individual power dissipation of the four regulators plus a minor amount for chip overhead. Chip overhead is Bias, TSD & LDO analog.

$P_{D\text{-}MAX} = P_{LDO1} + P_{LD02} + P_{BUCK1} + P_{BUCK2} + (0.0001A * V_{IN})$ [Watts].

Power dissipation of LDO1

$P_{LDO1} = (V_{INLDO1} - V_{OUTLDO1}) * Iout_{LDO1}$ [V*A]

Power dissipation of LDO2

$P_{LDO2} = (V_{INLDO2} - Vout_{LDO2}) * Iout_{LDO2}$ [V*A]

Power dissipation of Buck1

$P_{Buck1} = P_{IN} – P_{OUT} =$

$Vout_{Buck1} * Iout_{Buck1} * (1 - \eta_1) / \eta_1$ [V*A]

η_1 = efficiency of buck 1

Power dissipation of Buck2

$P_{Buck2} = P_{IN} – P_{OUT} =$

$Vout_{Buck2} * Iout_{Buck2} * (1 - \eta_2) / \eta_2$ [V*A]

η_2 = efficiency of Buck2

Where η is the efficiency for the specific condition taken from efficiency graphs.

Thermal Performance of the LLP Package

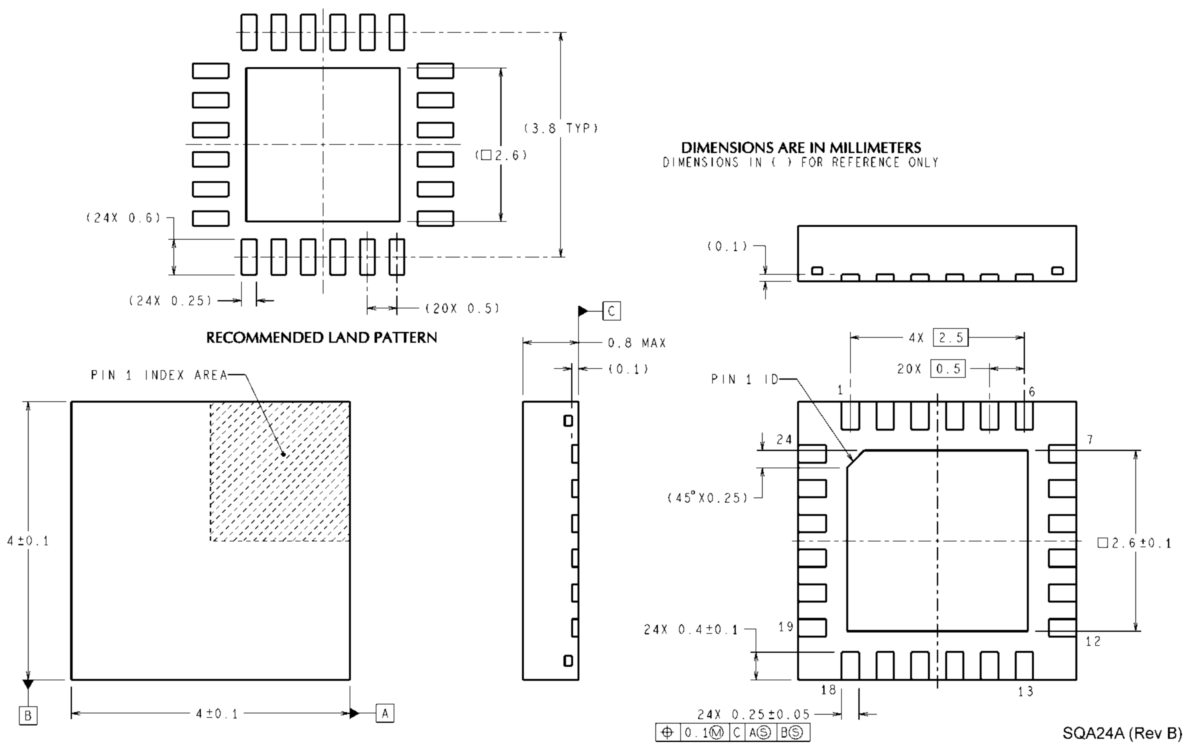
The LP3907 is a monolithic device with integrated power FETs. For that reason, it is important to pay special attention to the thermal impedance of the LLP package and to the PCB layout rules in order to maximize power dissipation of the LLP package.

The LLP package is designed for enhanced thermal performance and features an exposed die attach pad at the bottom center of the package that creates a direct path to the PCB for maximum power dissipation. Compared to the traditional leaded packages where the die attach pad is embedded inside the molding compound, the LLP reduces one layer in the thermal path.

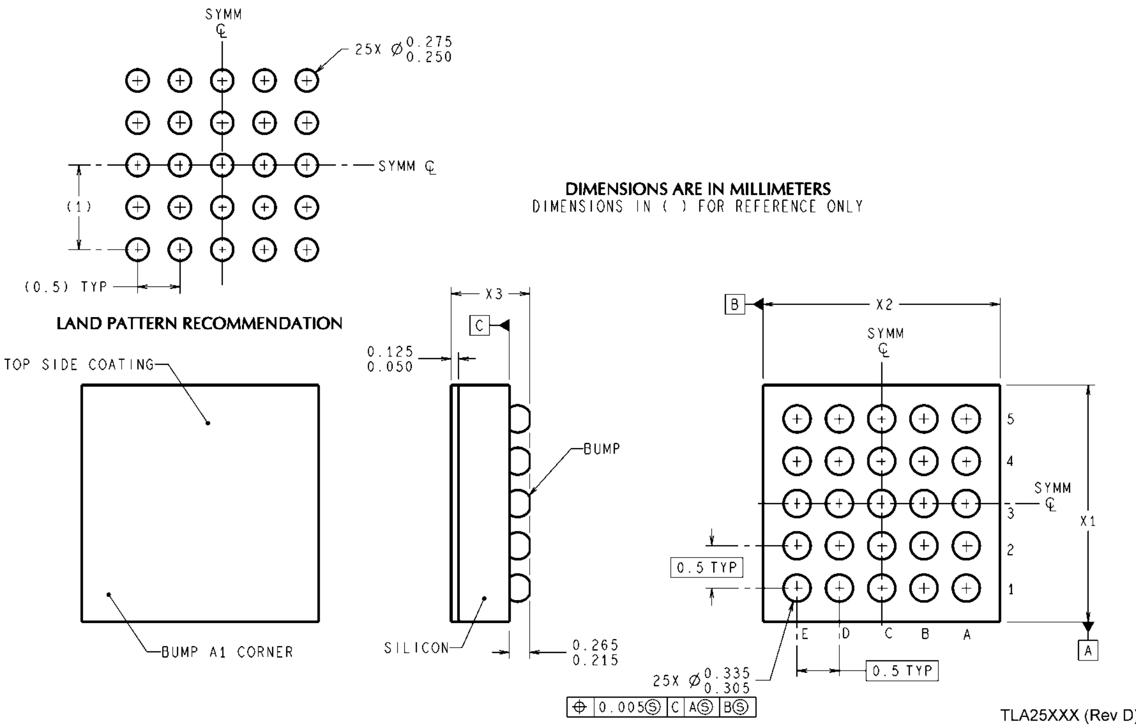
The thermal advantage of the LLP package is fully realized only when the exposed die attach pad is soldered down to a thermal land on the PCB board with thermal vias planted underneath the thermal land. Based on thermal analysis of the LLP package, the junction-to-ambient thermal resistance (θJA) can be improved by a factor of two when the die attach pad of the LLP package is soldered directly onto the PCB with thermal land and thermal vias, as opposed to an alternative with no direct soldering to a thermal land. Typical pitch and outer diameter for thermal vias are 1.27mm and 0.33mm respectively. Typical copper via barrel plating is 1oz, although thicker copper may be used to further improve thermal performance. The LP3907 die attach pad is connected to the substrate of the IC and therefore, the thermal land and vias on the PCB board need to be connected to ground (GND pin).

For more information on board layout techniques, refer to Application Note AN–1187 “Leadless Lead frame Package (LLP).” on http://www.national.com This application note also discusses package handling, solder stencil and the assembly process.

Physical Dimensions inches (millimeters) unless otherwise noted



4 X 4 X 0.8 mm 24-Pin LLP Package
NS Package SQA24A
For ordering, refer to Ordering Information table



2.5 X 2.5 mm 25-Bump micro SMD Package
NS Package TLA25AAA
For ordering, refer to Ordering Information table
X1 = 2492 ± 30µm
X2 = 2492 ± 30µm
X3 = 600 ± 75µm

Notes

Notes

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Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
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