Intel® 6702PXH 64-bit PCI Hub

Datasheet

September 2004

Reference Number: 303633-001

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Revision History

Revision	Doc #	Description	Date
001	303633	Initial Release.	September 2004

Intel® 6702PXH 64-bit PCI Hub Features

- PCI Express* Interface
  - — Compatible with *PCI Express Base Specification 1.0a*
  - — Raw bit-rate on the data pins of 2.5 Gbit/s, resulting in a raw bandwidth per pin of 250 MB/s
  - — x8 and x4 modes of operation, support for x4 on 3:0 (with 3 being lane 3) and 4:7 (with 4 being lane 3)
  - — Support for x8, x4 lane reversal
  - — Support for x4 lane reversal only on the lower 4 lanes
  - — Maximum realized bandwidth (in x8 mode) on PCI Express interface is 2 GB/s in each direction simultaneously, for an aggregate of 4 GB/s
  - — Full-speed self-test and diagnostic (IBIST) functionality
  - — Automatic link initialization, configuration and re-training out of reset
  - — Runtime detection and recovery for loss of link synchronization
- PCI-X Interface
  - — PCI Spec rev 2.3 compliant
  - — PCI-X 1.0b spec compliant
  - — 64-bit 66MHz, 3.3V
  - — 6 external REQ/GNT Pairs for internal arbiter (only 3 pairs are available when operating SHPC in parallel mode)
  - — On-die termination of 8.33K ohms @ +/- 40%
  - — 64 bit addressing, inbound and outbound and support for DAC command
- RAS Features
  - — PCI Express interfaces protected with 32-bit CRC
  - — Full access to all registers via SMBus
  - — PCI bus protected with parity
- PCI standard Hot Plug
  - — PCI Standard Hot-Plug controller Specification Rev 1.0 compliant
  - — Support for 6 slots maximum
  - — Parallel mode operation for 1 and 2 slot systems and slot interface logic not needed.
  - — Serial mode operation for other systems with hot-plug slots from 3 to 6. Slot interface logic needed to serialize and de-serialize information from Intel® 6702PXH 64-bit PCI Hub
  - — 1-slot-no-glue parallel mode operation when the number of slots controlled is one and there are no other devices on the PCI bus. No on-board Q-Switches are needed for bus isolation in this mode
- I/OxAPIC
  - — One I/OxAPIC controller per PCI bus segment
  - — 24 interrupts per controller
  - — 16 physical PCI interrupt pins per PCI bus in the server mode
  - — PCI virtual wire interrupt support via writing to Pin Assertion Register in the I/OxAPIC
- SMBus Interface
  - — Electrically compliant with System Management Bus 2.0 Specification with PEC support
  - — Slave mode operation only
  - — Full read/write access to all configuration and memory spaces in Intel® 6702PXH 64-bit PCI Hub
- Power Management
  - — Support for PCI Express Active State Power Management (ASPM) L0s link state
  - — Support for PCI PM 1.1 compatible D0, D3hot and D3cold device power states
  - — Support for PME# event propagation on behalf of PCI devices

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1 Introduction

The Intel® 6702PXH 64-bit PCI Hub are peripheral chips that perform PCI bridging functions between the PCI Express interface and the PCI Bus. The Intel® 6702PXH 64-bit PCI Hub contains a single PCI bus interface that can be configured to operate in PCI (33 or 66 MHz) or PCI-X Mode 1 (66, 100, or 133 MHz).

The Intel® 6702PXH 64-bit PCI Hub further support the new *PCI Standard Hot-Plug Controller and Subsystem Specification,* Revision 1.0. Each PCI interface contains an I/OxAPIC with 24 interrupts and a standard hot plug controller.

1.1 Related Documents

- *PCI Express Base Specification*, Revision 1.0a, from www.pci-sig.com.
- *PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification*, Revision 2.0a, and *PCI-X Protocol Addendum to the PCI Local Bus Specification*, Revision 2.0a, both from www.pci-sig.com.
- *PCI Local Bus Specification*, Revision 2.3, from www.pci-sig.com.
- *PCI Standard Hot-Plug Controller and Subsystem Specification*, Revision 1.0, from www.pci-sig.com.
- *PCI to PCI Bridge Architecture Specification*, Revision 1.1, from www.pci-sig.com.
- *PCI Power Management Interface Specification*, Revision 1.1, from www.pci-sig.com.
- *SMBus Specification*, Revision 2.0.
- *IEEE Standard Test Access Port and Boundary Scan Architecture 1149.1a.*

1.2 Intel® 6702PXH 64-bit PCI Hub Overview

1.2.1 PCI Express Interface (Primary Bus)

The primary bus interface between the Intel® 6702PXH 64-bit PCI Hub and the core logic chipset component is the PCI Express interface. Maximum realized bandwidth on this interface is 2 GB/s in each direction simultaneously, for an aggregate of 4 GB/s. The PCI Express interface is compatible with the *PCI Express Base Specification*, Revision 1.0a. The Intel® 6702PXH 64-bit PCI Hub supports X1, X4, and X8 widths for PCI Express. X4 width is supported on 3:0 (with 3 being lane 3) and 4:7 (with 4 being lane 3), and X1 width is supported on lanes 7, 4, 3, and 0. The Intel® 6702PXH 64-bit PCI Hub also supports X8 lane reversal, plus X4 lane reversal on the lower 4 lanes only.

1.2.2 PCI/PCI-X Bus Interfaces (Secondary Bus)

The Intel® 6702PXH 64-bit PCI Hub has a single PCI Bus interface (PCI Bus A). In this document these buses are referred to as the secondary buses. These interfaces can be independently configured as either a PCI Bus or PCI-X Bus. The Intel® 6702PXH 64-bit PCI Hub support conventional PCI and PCI-X Mode 1. PCI Bus extensions are also supported; these include 64-bit addressing outbound, with the capability to assert DAC, and full 64-bit addressing inbound. The inbound packet size is based on cache line size of the platform.

The PCI Bus interface is compliant with the *PCI Local Bus Specification,* Revision 2.3. The PCI-X interface on the Intel® 6702PXH 64-bit PCI Hub is compliant with the *PCI-X Addendum to the PCI Local Bus Specification,* Revision 1.0b as well as the Mode 1 section of the *PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification*, Revision 2.0a and the *PCI-X Protocol Addendum to the PCI Local Bus Specification,* Revision 2.0a. For conventional PCI Mode, the Intel® 6702PXH 64-bit PCI Hub supports PCI bus frequencies of 33 MHz and 66 MHz. For the PCI-X Mode 1, the Intel® 6702PXH 64-bit PCI Hub supports PCI bus frequencies of 66 MHz, 100 MHz, and 133 MHz.

1.2.3 PCI Standard Hot Plug Controller

The Intel® 6702PXH 64-bit PCI Hub hot plug controller is compliant with *PCI Standard-Hot Plug Controller and Subsystem Specification*, Revision 1.0 and allows PCI card removal, replacement, and addition without powering down the system. The Intel® 6702PXH 64-bit PCI Hub hot plug controller supports three to six PCI slots through an input/output serial interface when operating in Serial Mode, and one to two slots through an input/output parallel interface when operating in Parallel Mode. The Intel® 6702PXH 64-bit PCI Hub can also operate in “one-slot-no-glue” hot plug mode, which does not require and on-board logic for enabling and disabling the bus and clocks signals to the PCI/PCI-X hot plug slots. The input serial interface is polling and is in continuous operation. The output serial interface is “demand” and acts only when requested. These serial interfaces run at about 8.25 MHz regardless of the speed of the PCI bus. In parallel mode, the Intel® 6702PXH 64-bit PCI Hub performs the serial to parallel conversion internally, so the serial interface cannot be observed. However, internally the hot plug controller always operates in a serial mode.

1.2.4 I/OxAPIC Controller

The Intel® 6702PXH 64-bit PCI Hub contains one I/OxAPIC controller, which reside on the primary bus. The intended use of this controller for the Intel® 6702PXH 64-bit PCI Hub is to have the interrupt from PCI bus A connected to the interrupt controller on device 0, function 1.

1.2.5 SMBus Interface

The SMBus interface can be used for system and power management related tasks. The interface is compliant with *System Management Bus Specification,* Revision 2.0. The SMBus interface allows full read/write access to all configuration and memory spaces in the Intel® 6702PXH 64-bit PCI Hub.

1.2.6 JTAG

The Intel® 6702PXH 64-bit PCI Hub has a JTAG (TAP) port compliant with the *IEEE Standard Test Access Port and Boundary Scan Architecture 1149.1 Specifications.* The TAP controller is accessed serially through five dedicated pins. This can be used for test and debug purposes. System board interconnects can be DC tested using the boundary scan logic in pads.

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2 Signal Description

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name the signal is asserted when at the high voltage level.

Note: Segment "A" signifies the interface of the PCI bus segment of the Intel® 6702PXH 64-bit PCI Hub. All Intel® 6702PXH 64-bit PCI Hub PCI bus signals will use the letter "A" in these signal names. For example, in the PCI Bus interface, PAAD[31:0] refer to the AD bus signals on PCI Bus A.

The following notations are used to describe the signal type:

P Power pin

I Input pin

O Output pin

I/O Bi-directional Input/Output pin

2.1 PCI Express Interface

Table 2-1. PCI Express* Interface Signals

Signal	Type	Description
EXP_CLK EXP_CLK#	I	**PCI Express* Reference Clocks:** 100 MHz differential clock pair. Connect to an external 100 MHz differential clock.
EXP_COMP[1:0]	I	**PCI Express Compensation Inputs:** Analog signals.
EXP_RXP[7:0] EXP_RXN[7:0]	I	**PCI Express Serial Data Inputs:** PCI Express differential data receive signals. For 4X mode, only signals EXP_RXP[3:0] and EXP_RXN[3:0] are used. For 8X mode, all of these signals, EXP_RXP[7:0] and EXP_RXN[7:0], are used. These signals are the PExRp[7:0] and PExRn[7:0] signals per the PCI SIG convention.
EXP_TXP[7:0] EXP_TXN[7:0]	O	**PCI Express Serial Data Outputs:** PCI Express differential data transmit signals. For 4X mode, only signals EXP_TXP[3:0] and EXP_TXN[3:0] are used. For 8X mode, all of these signals, EXP_TXP[7:0] and EXP_TXN[7:0], are used. These signals are the PExTp[7:0] and PExTn[7:0] signals per the PCI SIG convention.

2.2 PCI/PCI-X Bus Interface

Table 2-2. PCI Bus Interface A Signals (Sheet 1 of 2)

Signal	Type	Description
PA133EN	I	Only relevant when Intel® 6702PXH 64-bit PCI Hub samples PAPCIXCAP at a level indicating 133MHz PCI-X capability. **PCI-X 133 MHz Enable:** Sets the maximum frequency capability of a PCI-X mode 1 bus to either 100 MHz or 133 MHz. This pin, when high, allows the PCI-X segment to run at a maximum 133 MHz when in PCI-X mode 1. When low, the PCI-X segment is limited to a maximum frequency of 100 MHz when in PCI-X mode 1.
PAAD[31:0]	I/O	**PCI Address/Data:** These signals are a multiplexed address and data bus. During the address phase or phases of a transaction, the initiator drives a physical address on PAAD[31:0]. During the data phases of a transaction, the initiator drives write data, or the target drives read data.
PACBE_[3:0]#	I/O	**Bus Command and Byte Enables:** These signals are a multiplexed command field and byte enable field. During the address phase or phases of a transaction, the initiator drives the transaction type on PACBE_[3:0]#. For both read and write transactions, the initiator drives byte enables on PACBE_[3:0]# during the data phases.
PADEVSEL#	I/O	**Device Select:** The Intel® 6702PXH 64-bit PCI Hub asserts PADEVSEL# to claim a PCI transaction. As a target, the Intel® 6702PXH 64-bit PCI Hub asserts PADEVSEL# when a PCI master peripheral attempts an access to an internal address or an address destined for the PCI Express* interface. As an initiator, PADEVSEL# indicates the response to a Intel® 6702PXH 64-bit PCI Hub-initiated transaction on the PCI bus. PADEVSEL# is tri-stated from the leading edge of PAPCIRST#. PADEVSEL# remains tri-stated by the Intel® 6702PXH 64-bit PCI Hub until driven as a target.
PAFRAME#	I/O	**Frame:** PAFRAME# is driven by the Initiator to indicate the beginning and duration of an access. While PAFRAME# is asserted, data transfers continue. When PAFRAME# is negated, the transaction is in the final data phase.
PAGNT_[5:0]#	O	**PCI Grants:** Bus grant output corresponding to request inputs 5 through 0 from the Intel® 6702PXH 64-bit PCI Hub arbiter. This signal indicates that an initiator can start a transaction on the PCI bus.
PAIRDY#	I/O	**Initiator Ready:** PAIRDY# indicates the ability of the initiator to complete the current data phase of the transaction. A data phase is completed when both PAIRDY# and PATRDY# are sampled asserted.
PAM66EN	I/O	Only relevant when Hot Plug Mode is disabled (HPA_SLOT[3] = 0) or when in one-slot-no-glue hot plug mode (HPA_SLOT[3:0] = 1111). **66 MHz Enable:** This input signal from the PCI Bus indicates the speed of the PCI Bus. If it is high, the bus speed is 66 MHz; if it is low, the bus speed is 33 MHz. This signal will be used to generate the appropriate clock (33 MHz or 66 MHz) on the PCI Bus. **Hot Plug Mode Enabled:** Not used. The PCI bus will power up as 33 MHz PCI and the Intel® 6702PXH 64-bit PCI Hub will drive this pin low. Also, if software ever writes 00 to the PFREQ Register, the Intel® 6702PXH 64-bit PCI Hub will drive this pin low. **Hot Plug Mode Disabled:** Controls max frequency (33 MHz or 66 MHz) of the PCI segment when running in conventional PCI mode: 0 = 33 MHz PCI 1 = 66 MHz PCI

Table 2-2. PCI Bus Interface A Signals (Sheet 2 of 2)

Signal	Type	Description
PAPAR	I/O	**Parity:** Even parity calculated on 36 bits (PAAD[31:0] plus PACBE_[3:0]#). It is calculated on all 36 bits, regardless of the valid byte enables. It is driven identically to the PAAD[31:0] lines, except it is delayed by exactly one PCI clock.
PAPCIRST#	O	**PCI Reset:** The Intel® 6702PXH 64-bit PCI Hub asserts PAPCIRST# to reset devices that reside on the secondary PCI bus. The Intel® 6702PXH 64-bit PCI Hub asserts PAPCIRST# due to one of the following events: • RSTIN# is asserted. • The PCI Reset (bit 6) in the Bridge Control Register is set. Connect to the RST# pin of the PCI slot(s).
PAPCIXCAP	I	Only relevant when Hot Plug Mode is disabled (HPA_SLOT[3] = 0) or when in one-slot-no-glue hot plug mode (HPA_SLOT[3:0] = 1111). **PCI-X Capable:** This signal indicates whether all devices on the PCI bus are PCI-X devices, so that the Intel® 6702PXH 64-bit PCI Hub can switch into PCI-X mode.
PAPCLKI	I	**PCI Clock Input.**
PAPCLKO[6:0]	O	**PCI Clock Output:** These signals provide 33/66/100/133 MHz clock for a PCI/PCI-X device. PAPCLKO[0] goes to slot or device #1, PAPCLKO[1] goes to slot or device #2, etc. PAPCLKO[6] is connected to the PAPCLKI input. Unused PCI Clock outputs should be turned off by BIOS and left as no connects on the system board.
PAPERR#	I/O	**Parity Error:** PAPERR# is driven by an external PCI device when it receives data that has a parity error. Driven by the Intel® 6702PXH 64-bit PCI Hub when, as an initiator it detects a parity error during a read transaction and as a target during write transactions.
PAPLOCK#	O	**PCI Lock:** This signal indicates an exclusive bus operation and may require multiple transactions to complete. The Intel® 6702PXH 64-bit PCI Hub asserts PAPLOCK# when it is doing exclusive transactions on the PCI bus. PAPLOCK# is ignored when PCI masters are granted the bus. The Intel® 6702PXH 64-bit PCI Hub does not propagate locked transactions upstream.
PAPME#	I	**PCI Power Management Event:** PCI bus power management event signal. This is a shared open drain signal from all the PCI cards on the corresponding PCI bus segment. This is a level sensitive signal that will be converted to a PME event on the PCI Express bus.
PAREQ_[5:0]#	I	**PCI Request:** Request input into the Intel® 6702PXH 64-bit PCI Hub arbiter.
PASERR#	I	**System Error:** PASERR# can be pulsed active by any PCI device that detects a system error condition except the Intel® 6702PXH 64-bit PCI Hub. The Intel® 6702PXH 64-bit PCI Hub samples PASERR# as an input and conditionally forwards it to the PCI Express interface.
PASTOP#	I/O	**Stop:** PASTOP# indicates that the target is requesting an initiator to stop the current transaction.
PATRDY#	I/O	**Target Ready:** PATRDY# indicates the ability of the target to complete the current data phase of the transaction. A data phase is completed when both PATRDY# and PAIRDY# are sampled asserted. PATRDY# is tri-stated from the leading edge of PAPCIRST#. PATRDY# remains tri-stated by the Intel® 6702PXH 64-bit PCI Hub until driven as a target.

2.3 PCI Bus Interface 64-bit Extension

Table 2-3. PCI Bus Interface 64-bit Extension Interface A Signals

Signal	Type	Description
PAACK64#	I/O	**PCI Interface Acknowledge 64-bit Transfer:** This signal is asserted by the target only when PAREQ64# is asserted by the initiator. It indicates the target's ability to transfer data using 64 bits. It has the same timing as PADEVSEL#.
PAAD[63:32]	I/O	**PCI Address/Data:** These signals are a multiplexed address and data bus. This bus provides an additional 32 bits to the PCI bus. During the data phases of a transaction, the initiator drives the upper 32 bits of 64-bit write data, or the target drives the upper 32 bits of 64-bit read data, when PAREQ64# and PAACK64# are both asserted.
PACBE_[7:4]#	I/O	**Bus Command and Byte Enables (Upper 4 bits):** These signals are a multiplexed command field and byte enable field. For both read and write transactions, the initiator will drive byte enables for the PAAD[63:32] data bits on PACBE_[7:4]# during the data phases when PAREQ64# and PAACK64# are both asserted.
PAPAR64	I/O	**PCI Interface Upper 32-bits Parity:** This signal carries the even parity of the 36 bits of PAAD[63:32] and PACBE_[7:4]# for both address and data phases.
PAREQ64#	I/O	**PCI interface Request 64-bit Transfer:** This signal is asserted by the initiator to indicate that the initiator is requesting a 64-bit data transfer. It has the same timing as PAFRAME#. When the Intel® 6702PXH 64-bit PCI Hub is the initiator, this signal is an output. When the Intel® 6702PXH 64-bit PCI Hub is the target, this signal is an input.

2.4 Interrupt Interface

This section lists the interrupt interface signals.

Table 2-4. Interrupt Interface A Signals

Signal	Type	Description
PAIRQ_[15:0]#	I	**Interrupt Request Bus:** The PAIRQ# lines from PCI interrupts PIRQ[A:D] can be routed to these interrupt lines.

2.5 Hot Plug Interface

Table 2-5. General Hot Plug Interface A Signals – All Hot Plug Modes

Signal	Type	Description
HPA_SLOT[3]	I	**Enable/Disable PCI Hot Plug Mode:** 1 = Hot Plug Mode Enabled 0 = Hot Plug Mode Disabled
HPA_SLOT[2:0]	I	**Hot Plug Mode / # of PCI Slots:** Used in conjunction with HPA_SLOT[3] signal to determine PCI Hot Plug Mode and number of PCI slots on a bus segment. HPA_SLOT[3:0] = Hot Plug Mode Enable/Disable, # of PCI slots 0000 = hot plug disabled, 1 slot (optional) 0001 = hot plug disabled, 2 slots (optional) 0010 = hot plug disabled, 3 slots (optional) 0011 = hot plug disabled, 4 slots (optional) 0100 = hot plug disabled, 5 slots (optional) 0101 = hot plug disabled, 6 slots (optional) 0110 = hot plug disabled, 7 slots (optional) 0111 = hot plug disabled, 8 slots (optional) 1000 = reserved 1001 = hot plug enabled, 1 slot (parallel mode) 1010 = hot plug enabled, 2 slots (parallel mode) 1011 = hot plug enabled, 3 slots (serial mode) 1100 = hot plug enabled, 4 slots (serial mode) 1101 = hot plug enabled, 5 slots (serial mode) 1110 = hot plug enabled, 6 slots (serial mode) 1111 = hot plug enabled, 1-slot-no-glue (parallel mode)

Table 2-6. Serial Mode Hot Plug Signals – Interface A – 3 to 6 Slots (Sheet 1 of 2)

Signal	Type	Description
HPA_SLOT[3:0]	I	**Hot Plug Mode Enable / # of PCI Slots:** Used to enable/disable hot plug mode and to determine number of hot plug slots. HPA_SLOT[3:0]: 1011 = hot plug enabled, 3 slots (serial mode) 1100 = hot plug enabled, 4 slots (serial mode) 1101 = hot plug enabled, 5 slots (serial mode) 1110 = hot plug enabled, 6 slots (serial mode)
HPA_PRST#	O	**Primary Bus Reset Out (HPA_PRST#):** This is asserted whenever the primary side of the Intel® 6702PXH 64-bit PCI Hub goes through a reset, even if hot plug is disabled. Resets the slot interface logic in hot plug serial mode.
HPA_SIC	O	**Serial Input Clock:** This signal is normally high. It pulses low to shift external serial input shift register data one bit position. (The shift registers should be similar to standard “74x165” series).
HPA_SID	I	**Serial Input Data:** Data shifted in from external logic on HPA_SIC.

Table 2-6. Serial Mode Hot Plug Signals – Interface A – 3 to 6 Slots (Sheet 2 of 2)

Signal	Type	Description
HPA_SIL#	O	**Serial Input Load:** This signal is normally high. It pulses low to synchronously parallel load external serial input shift registers on the next rising edge of HPA_SIC.
HPA_SOC	O	**Serial Output Clock:** This signal is normally high. It pulses low to shift internal serial output shift register data one bit position. (The shift registers should be similar to standard “74x164” series.)
HPA_SOD	O	**Serial Output Data:** Data is shifted out to external logic on HPA_SOC.
HPA_SOL	O	**Serial Output Non-Reset Latch Load:** This signal is normally high. It pulses low to clock external latches (power-enable, clock-enable, slot bus-enable, and LED latches). The high edge acts as the clock.
HPA_SOLR	O	**Serial Output Reset Latch Load:** This signal is normally high. It pulses high to clock external latches (Reset latches) reading the serial output shift registers. The high edge acts as the clock.

Table 2-7. Parallel Mode Hot Plug Signals – Interface A – 1 to 2 Slots (Sheet 1 of 4)

Signal	Type	Description
HPA_SLOT[3:0]	I	**Hot Plug Mode Enable / # of PCI Slots:** Used to enable/disable hot plug mode and to determine number of hot plug slots. HPA_SLOT[3:0]: 1111 = hot plug enabled, one-slot-no-glue hot plug mode 1001 = hot plug enabled, 1 slot (parallel mode) 1010 = hot plug enabled, 2 slots (parallel mode)
HAATNLED_1#	O	**Slot 1 Attention LED:** Control for attention LED of the first hot plug slot, which is yellow or amber in color. Only used when in one-slot-no-glue, single-slot parallel, or dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1111, 1001, or 1010).
HPA_SOLR/ HAATNLED2#	O	**Slot 2 Attention LED:** Control for attention LED of the second hot plug slot, which is yellow or amber in color. Only used when in dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1010).
PAGNT_[5]#/ HABUSEN_1#	O	**Slot 1 Bus Enable:** Bus enable signals that connect the PCI bus signals of the first PCI slot to the system bus PCI bus via FET isolation switches. Only used when in single-slot or dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1001 or 1010).
PAGNT_[4]#/ HABUSEN_2#	O	**Slot 2 Bus Enable:** Bus enable signals that connect the PCI bus signals of the second PCI slot to the system bus PCI bus via FET isolation switches. Only used when in dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1010).
PAIRQ_[8]#/ HABUTTON_1#	I	**Slot 1 Attention Button:** Optional. Attention button input signal connected to the first hot plug slot’s attention button. When low, indicates that the operator has requested attention. If attention button is not implemented, then this input must be wired to a high logic level. Only used when in one-slot-no-glue, single-slot or dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1111, 1001 or 1010).

Table 2-7. Parallel Mode Hot Plug Signals – Interface A – 1 to 2 Slots (Sheet 2 of 4)

Signal	Type	Description
HPA_SOL/ HABUTTON2#	O	**Slot 2 Attention Button:** Optional. Attention button input signal connected to the second hot plug slot's attention button. When low, indicates that the operator has requested attention. If attention button is not implemented, then this input must be wired to a high logic level. Only used when in dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1010).
HPA_SIL#/ HACLKEN_1#	O	**Slot 1 Clock Enable:** Clock enable signals that connect the PCI clock signals of the first PCI slot to the system bus PCI bus via FET isolation switches. Only used when in single-slot or dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1001 or 1010).
HPA_SOD/ HACLKEN_2	O	**Slot 2 Clock Enable:** Clock enable signals that connect the PCI clock signals of the second PCI slot to the system bus PCI bus via FET isolation switches. Only used when in dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1010).
PAIRQ_[11]#/ HAM66EN_1	I	**Slot 1 M66EN:** Determines if an add-in card is capable of running at 66 MHz in conventional PCI mode for the first hot plug slot. Only used when in one-slot-no-glue, single-slot parallel, or dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1111, 1001, or 1010).
PAIRQ_[12]#/ HAM66EN_2	I	**Slot 2 M66EN:** Determines if an add-in card is capable of running at 66 MHz in conventional PCI mode for the second hot plug slot. Only used when in dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1010).
PAIRQ_[15]#/ HAMRL1#	I	**Slot 1 Manual Retention Latch:** Optional. Manually operated retention latch sensor input. A logic low input that is connected directly to the MRL sensor on the first hot plug slot. When asserted it indicates that the MRL latch is closed. If a platform does not support MRL sensors, this must be wired to a low logic level (MRL closed). Only used when in one-slot-no-glue, single-slot parallel, or dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1111, 1001, or 1010).
HPA_SLOT[0]/ HAMRL_2#	I	**Slot 2 Manual Retention Latch:** Optional. Manually operated retention latch sensor input. A logic low input that is connected directly to the MRL sensor on the second hot plug slot. When asserted it indicates that the MRL latch is closed. If a platform does not support MRL sensors, this must be wired to a low logic level (MRL closed). Only used when in dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1010).
PAIRQ_[10]#/ HAPCIXCAP1_1	I	**Slot 1 PCIXCAP1:** Determines if the first hot plug slot is PCI-X capable, and if so, whether it can operate at 133 MHz. PCIXCAP1 and PCIXCAP2 represent a decoded version of the three-state PCIXCAP pin present on each slot. PCIXCAP2 represents whether the PCIXCAP pin was ground or not ground (i.e., PCI-X capable), and PCIXCAP1 represents whether the PCIXCAP pin was "low" (66 MHz only) or high (133 MHz capable). The system initially powers up at 33 MHz PCI, and all hot plug slots are scanned by firmware. If the system is capable, the bus is reset to run in the appropriate PCI-X mode. These pins are used only in one-slot-no-glue, single-slot parallel or dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1111,1001 or 1010).

Table 2-7. Parallel Mode Hot Plug Signals – Interface A – 1 to 2 Slots (Sheet 3 of 4)

Signal	Type	Description
PAIRQ_[9]#/ HAPCIXCAP2_1	I	**Slot 1 PCIXCAP2:** Determines if the first hot plug slot is PCI-X capable, and if so, whether it can operate at 133 MHz. PCIXCAP1 and PCIXCAP2 represent a decoded version of the three-state PCIXCAP pin present on each slot. PCIXCAP2 represents whether the PCIXCAP pin was ground or not ground (i.e., PCI-X capable), and PCIXCAP1 represents whether the PCIXCAP pin was “low” (66 MHz only) or high (133 MHz capable). The system initially powers up at 33 MHz PCI, and all hot plug slots are scanned by firmware. If the system is capable, the bus is reset to run in the appropriate PCI-X mode. These pins are used only in one-slot-no-glue, single-slot parallel or dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1111,1001 or 1010).
HPA_SID/ HAPCIXCAP1_2	I	**Slot 2 PCIXCAP1:** Determines if the first hot plug slot is PCI-X capable, and if so, whether it can operate at 133 MHz. PCIXCAP1 and PCIXCAP2 represent a decoded version of the three-state PCIXCAP pin present on each slot. PCIXCAP2 represents whether the PCIXCAP pin was ground or not ground (i.e., PCI-X capable), and PCIXCAP1 represents whether the PCIXCAP pin was “low” (66 MHz only) or high (133 MHz capable). The system initially powers up at 33 MHz PCI, and all hot plug slots are scanned by firmware. If the system is capable, the bus is reset to run in the appropriate PCI-X mode. These pins are used only in dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1010).
HPA_SOC/ HAPCIXCAP2_2	I	**Slot 2 PCIXCAP2:** Determines if the second hot plug slot is PCI-X capable, and if so, whether it can operate at 133 MHz. PCIXCAP1 and PCIXCAP2 represent a decoded version of the three-state PCIXCAP pin present on each slot. PCIXCAP2 represents whether the PCIXCAP pin was ground or not ground (i.e., PCI-X capable), and PCIXCAP1 represents whether the PCIXCAP pin was “low” (66 MHz only) or high (133 MHz capable). The system initially powers up at 33 MHz PCI, and all hot plug slots are scanned by firmware. If the system is capable, the bus is reset to run in the appropriate PCI-X mode. These pins are used only in the dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1010).
HPA_SLOT[1]/ HAPRSNT1_1#	I	**Slot 1 PRESENT1#:** Input signal (optional). Used in conjunction with HAPRSNT2_1# to indicate to the Intel® 6702PXH 64-bit PCI Hub whether an add-on card is installed in the first hot plug slot and its power requirements. Only used when in one-slot-no-glue, single-slot or dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1111, 1001 or 1010).
PAREQ_[5]#/ HAPRSNT1_2#	I	**Slot 2 PRESENT1#:** Input signal (optional). Used in conjunction with HAPRSNT2_2# to indicate to the Intel® 6702PXH 64-bit PCI Hub whether an add-on card is installed in the second hot plug slot and its power requirements. Only used when in dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1010).
PAREQ_[3]#/ HAPRSNT2_1#	I	**Slot 1 PRESENT2#:** Input signal (optional). Used in conjunction with HAPRSNT1_1# to indicate to the Intel® 6702PXH 64-bit PCI Hub whether an add-on card is installed in the first hot plug slot and its power requirements. This signal is directly connected to the present bits on the PCI/PCI-X add-on card. Only used when in one-slot-no-glue, single-slot or dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1111, 1001 or 1010).
PAREQ_[4]#/ HAPRSNT2_2#	I	**Slot 2 PRESENT2#:** Input signal (optional). Used in conjunction with HAPRSNT1_2# to indicate to the Intel® 6702PXH 64-bit PCI Hub whether an add-on card is installed in the second hot plug slot and its power requirements. This signal is directly connected to the present bits on the PCI/PCI-X add-on card. Only used when in dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1010).

Table 2-7. Parallel Mode Hot Plug Signals – Interface A – 1 to 2 Slots (Sheet 4 of 4)

Signal	Type	Description
HAPWREN_1	O	**Slot 1 Power Enable:** Connected to slot 1 on-board power controller to regulate current and voltage flow of the PCI slot. Only used when in one-slot-no-glue, single-slot parallel, or dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1111, 1001, or 1010).
PAGNT_[3]#/ HAPWREN_2	O	**Slot 2 Power Enable:** Connected to slot 2 on-board power controller to regulate current and voltage flow of the PCI slot. Only used when in dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1010).
PAIRQ_[14]#/ HAPWRFLT_1#	I	**Slot 1 Power Fault:** Power controller fault indication for over-current / under-voltage condition for the first hot plug slot. When asserted, the Intel® 6702PXH 64-bit PCI Hub, if enabled, immediately asserts reset to the slot and disconnects the PCI slot from the bus. Only used when in one-slot-no-glue, single-slot parallel, or dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1111, 1001, or 1010).
PAIRQ_[13]#/ HAPWRFLT_2#	I	**Hot Plug Parallel Mode only - (HAPWRFLT_2#):** Power controller fault indication for over-current / under-voltage condition for the second hot plug slot. When asserted, the Intel® 6702PXH 64-bit PCI Hub, if enabled, immediately asserts reset to the slot and disconnects the slot from the bus. Only used when in dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1010).
HPA_SLOT[3]/ HAPWRLED1#	O	**Slot 1 Power LED:** Output signal connected to the green power LED corresponding to the first hot plug slot. Only used when in one-slot-no-glue, single-slot parallel, or dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1111, 1001, or 1010).
HPA_SIC/ HAPWRLED2#	O	**Slot 2 Power LED:** Output signal connected to the power LED corresponding to the second hot plug slot, which is green in color. Only used when in dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1010).
HPA_PRST#/ HPA_RST1#	O	**Slot 1 Reset:** This is the slot 1 reset in the parallel hot plug mode. Connected to the RST# pin of the first PCI hot plug slot. Only used when in one-slot-not-glue, single-slot or dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1111, 1001 or 1010).
HPA_RST2#	O	**Slot 2 Reset:** This is the slot 2 reset in the parallel hot plug mode. Connected to the RST# pin of the second PCI hot plug slot. Only used when in dual-slot parallel hot plug mode (HPA_SLOT[3:0] = 1010).

2.6 SMBus Interface

Table 2-8. SMBus Interface Signals

Signal	Type	Description
SCLK	I	**SMBus Clock**
SDTA	I/OD	**SMBus Data**
SMBUS[5] SMBUS[3:1]	I	SMBus Addressing Straps: SMBus Addressing: Bit 7----------‘1’ Bit 6----------‘1’ Bit 5----------SMBUS[5] Bit 4----------‘0’ Bit 3----------SMBUS[3] Bit 2----------SMBUS[2] Bit 1----------SMBUS[1]

2.7 Miscellaneous Signals

Table 2-9. Miscellaneous Signals

Signal	Type	Description
PWROK	I	**Power Supply OK:** When high indicates that the system power supply has stabilized. When low, asynchronously resets the Intel® 6702PXH 64-bit PCI Hub. Most of the strap pins on the Intel® 6702PXH 64-bit PCI Hub are sampled on the rising edge of this signal. Please refer to Section 2.18.2.1 for details on the timing relationship between PWROK, the PCI Express* clocks, and all voltages supplied to the Intel® 6702PXH 64-bit Hub.
RSTIN#	I	**Reset In:** When asserted, this signal asynchronously resets the Intel® 6702PXH 64-bit PCI Hub logic and asserts PAPCIRST# active output from each PCI interface. This signal is typically connected to the PAPCIRST# output of the ICH5 or the PLTRST# output of the ICH6.
TCK	I	**TAP Clock In:** This is the input clock to the JTAG TAP controller active rising edge, which runs from 0-16 MHz.
TDI	I	**Test Data In:** This is the serial data input to the JTAG BSCAN shift register chain and to the BSCAN control logic. This is latched in on the rising edge of TCK. If not using JTAG, this signal can be a no connect.
TDO	O	**Test Data Output:** This is the serial data output from the BSCAN logic. If not using JTAG, this signal can be a no connect.
TMS	I	**Test Mode Select:** This signal controls the TAP controller state machine to move to different states and is sampled on the rising edge of TCK. This signal can be a no connect if JTAG is not being used.
TRST#	I	**Test Reset In:** This signal is used to asynchronously reset the JTAG BSCAN logic.

2.8 Power and Ground

Table 2-10. Voltage Pins

Signal	Description
RCOMP	**PCI RCOMP:** Analog compensation pin for PCI (0.75V nominal).
VCC	**1.5V Core Voltage:** This is the voltage for the core, 1.5V.
VCCAEXP	**Analog PCI Express* Voltage:** 1.5V
VCCAPCI[2:0]	**Analog PCI Voltages:** 1.5V.
VCCBGEXP	**Analog Bandgap Voltage:** 2.5V
VCCEXP	**1.5V PCI Express* Voltage:** 1.5V.
VCC15	**1.5V I/O Voltage:** 1.5V.
VCC33	**3.3V PCI I/O Voltage:** This is the voltage for PCI I/O, 3.3V.
VREFPCI	**Analog Reference Voltage to PCI:** Input signal (0.75V nominal).
VSS	**Ground:** Ground for all voltage rails.
VSSAEXP	Analog PCI Express Ground.
VSSBGEXP	Analog Bandgap Ground.

2.9 Pin Straps

The following signals are used for static configuration. These signals are all sampled on the rising edge of PWROK, and then return to normal usage afterward.

Table 2-11. Normal Functional Pin Straps (Sheet 1 of 2)

Strap Pin	Function
HPA_SIC	**Intel Test Mode:** 1 = Normal operation 0 = Reserved
HPA_SID	**Intel Test Mode:** 1 = Reserved 0 = Normal operation
HPA_SLOT[3]	**Enable/Disable PCI Hot Plug Mode:** 1 = Hot Plug Mode Enabled 0 = Hot Plug Mode Disabled
HPA_SLOT[2:0]	**Hot Plug Mode / # of PCI Slots:** Used in conjunction with HPA_SLOT[3] signal to determine PCI Hot Plug Mode and number of PCI slots on a bus segment. HPA_SLOT[3:0] = Hot Plug Mode Enable/Disable, # of PCI slots 0000 = hot plug disabled, 1 slot (optional) 0001 = hot plug disabled, 2 slots (optional) 0010 = hot plug disabled, 3 slots (optional) 0011 = hot plug disabled, 4 slots (optional) 0100 = hot plug disabled, 5 slots (optional) 0101 = hot plug disabled, 6 slots (optional) 0110 = hot plug disabled, 7 slots (optional) 0111 = hot plug disabled, 8 slots (optional) 1000 = reserved 1001 = hot plug enabled, 1 slot (parallel mode) 1010 = hot plug enabled, 2 slots (parallel mode) 1011 = hot plug enabled, 3 slots (serial mode) 1100 = hot plug enabled, 4 slots (serial mode) 1101 = hot plug enabled, 5 slots (serial mode) 1110 = hot plug enabled, 6 slots (serial mode) 1111 = hot plug enabled, 1 slot-no-glue (parallel mode)
PA133EN	Only relevant when Hot Plug Mode is disabled (HPA_SLOT[3] = 0) OR when in one-slot-no-glue hot plug mode (HPA_SLOT[3:0] = 1111), AND when in PCI-X Mode (PAPCIXCAP = 1). **133 MHz PCI-X Enable/Disable:** Determines the maximum frequency (100 MHz or 133 MHz) of the PCI bus segment when in PCI-X Mode: 1 = 133 MHz PCI-X capable 0 = 100 MHz PCI-X max bus frequency

Table 2-11. Normal Functional Pin Straps (Sheet 2 of 2)

Strap Pin	Function
PAM66EN	Only relevant when Hot Plug Mode is disabled (HPA_SLOT[3] = 0) OR when in one-slot-no-glue hot plug mode (HPA_SLOT[3:0] = 1111) AND when in conventional PCI mode (PAPCIXCAP = 0). **PCI 66 MHz Enable/Disable:** Determines the maximum frequency (33 MHz or 66 MHz) of the PCI bus segment when in conventional PCI mode: 1 = 66 MHz capable when in conventional PCI mode 0 = 33 MHz max frequency when in conventional PCI mode Sampled on the rising edge of PWROK.
PASTRAP0	**Intel Test Mode:** 1 = Reserved 0 = Normal operation
HAATNLED_1#/ CMODE	This pin strap is used to configure PCI Express 1.0a support and is muxed with HAATNLED_1#. The CMODE/HAATNLED_1# pin does not have ODT (On-Die Termination). Please refer to the latest revision of the appropriate Platform Design Guide for board implementation details.
SMBUS[5] SMBUS[3:1]	**SMBus Addressing Straps:** Sets the SMBus address. SMBus Addressing: Bit 7----------'1' Bit 6----------'1' Bit 5----------SMBUS[5] Bit 4----------'0' Bit 3---------- SMBUS[3] Bit 2---------- SMBUS[2] Bit 1---------- SMBUS[1] Sampled on the rising edge of PWROK.

2.10 Intel® 6702PXH 64-bit PCI Hub Pin Strapping

Table 2-12. Intel® 6702PXH 64-bit PCI Hub Pin Strapping (Sheet 1 of 2)

Strap Pin	Strapping
STRAP_PXHV_1	Pull up to VCC33.
STRAP_PXHV_2	Pull up to VCC33.
STRAP_PXHV_3	Pull up to VCC33.
STRAP_PXHV_4	Pull up to VCC33.
STRAP_PXHV_5	Pull up to VCC33.
STRAP_PXHV_6	Pull up to VCC33.
STRAP_PXHV_7	Pull up to VCC33.
STRAP_PXHV_8	Pull up to VCC33.
STRAP_PXHV_9	Pull up to VCC33.
STRAP_PXHV_10	Pull up to VCC33.
STRAP_PXHV_11	Pull up to VCC33.

Table 2-12. Intel® 6702PXH 64-bit PCI Hub Pin Strapping (Sheet 2 of 2)

Strap Pin	Strapping
STRAP_PXHV_12	Pull up to VCC33.
STRAP_PXHV_13	Pull up to VCC33.
STRAP_PXHV_14	Pull up to VCC33.
STRAP_PXHV_15	Pull down to GND.

2.11 Signal Summary

2.11.1 Signals, Interfaces and Power Planes

Table 2-13. Intel® 6702PXH 64-bit PCI Hub Signals, Interfaces and Power Planes (Sheet 1 of 4)

Intel® 6702PXH 64-bit PCI Hub Signal	Hot Plug Muxed Signal (Parallel Mode, 1-2 Slots)	No. of Signals	Interface	Type	Operating Voltage	Notes
EXP_CLK#	N/A	1	PCI Express*	I	1.5V	100 MHz differential clock
EXP_CLK	N/A	1	PCI Express	I	1.5V	100 MHz differential clock
EXP_COMP[0]	N/A	1	PCI Express	I	0.5V	Analog voltage
EXP_COMP[1]	N/A	1	PCI Express	I	0.5V	Analog voltage
EXP_RXN[7:0]	N/A	8	PCI Express	I	1.5V	Serial data input
EXP_RXP[7:0]	N/A	8	PCI Express	I	1.5V	Serial data input
EXP_TXN[7:0]	N/A	8	PCI Express	I	1.5V	Serial data output
EXP_TXP[7:0]	N/A	8	PCI Express	I	1.5V	Serial data output
HAATNLED_1#	N/A	2	PCI	O	3.3V	Common clock
HAPWREN_1	N/A	2	Hot Plug	O	3.3V	Common clock
HPA_PRST#	HPA_RST1#	2	Hot Plug	O	3.3V	Common clock
HPA_RST2#	N/A	2	Hot Plug	O	3.3V	Common clock
HPA_SIC	HAPWRLED2#	2	Hot Plug	I	3.3V	Common clock
HPA_SID	HAPCIXCAP1_2	2	Hot Plug	I	3.3V	Common clock
HPA_SIL#	HACLKEN_1#	2	Hot Plug	I	3.3V	Common clock
HPASLOT[3]	HAPWRLED1#	2	Hot Plug	I	3.3V	Common clock, straps
HPASLOT[2]	N/A	2	Hot Plug	I	3.3V	Common clock, straps
HPASLOT[1]	HAPRSNT1_1#	2	Hot Plug	I	3.3V	Common clock, straps
HPASLOT[0]	HAMRL_2#	2	Hot Plug	I	3.3V	Common clock, straps

Table 2-13. Intel® 6702PXH 64-bit PCI Hub Signals, Interfaces and Power Planes (Sheet 2 of 4)

Intel® 6702PXH 64-bit PCI Hub Signal	Hot Plug Muxed Signal (Parallel Mode, 1-2 Slots)	No. of Signals	Interface	Type	Operating Voltage	Notes
HPASOC	HAPCIXCAP2_2	2	PCI / Hot Plug	O	3.3V	Common clock
HPASOD	HACLKEN_2#	2	Hot Plug	O	3.3V	Common clock
HPASOL	HABUTTON2#	2	Hot Plug	O	3.3V	Common clock
HPASOLR	HAATNLED2#	2	Hot Plug	O	3.3V	Common clock
PA133EN	N/A	2	PCI	I	3.3V	Common clock
PAACK64#	N/A	2	PCI	I/O	3.3V/1.5V	Source-synchronous
PAAD[63:0]	N/A	128	PCI	I/O	3.3V/1.5V	Source-synchronous
PACBE_[7]#	N/A	2	PCI	I/O	3.3V/1.5V	Source-synchronous
PACBE_[6]#	N/A	2	PCI	I/O	3.3V/1.5V	Source-synchronous
PACBE_[5]#	N/A	2	PCI	I/O	3.3V/1.5V	Source-synchronous
PACBE_[4]#	N/A	2	PCI	I/O	3.3V/1.5V	Source-synchronous
PACBE_[3]#	N/A	2	PCI	I/O	3.3V/1.5V	Source-synchronous
PACBE_[2]#	N/A	2	PCI	I/O	3.3V/1.5V	Source-synchronous
PACBE_[1]#	N/A	2	PCI	I/O	3.3V/1.5V	Source-synchronous
PACBE_[0]#	N/A	2	PCI	I/O	3.3V/1.5V	Source-synchronous
PADEVSEL#	N/A	2	PCI	I/O	3.3V	Common clock
PAFRAME#	N/A	2	PCI	I/O	3.3V	Common clock
PAGNT_[5]#	HABUSEN_1#	2	PCI / Hot Plug	O	3.3V	Common clock
PAGNT_[4]#	HABUSEN_2#	2	PCI / Hot Plug	O	3.3V/1.5V	Source-synchronous
PAGNT_[3]#	HAPWREN_2	2	PCI / Hot Plug	O	3.3V/1.5V	Source-synchronous
PAGNT_[2]#	N/A	2	PCI	O	3.3V/1.5V	Source-synchronous
PAGNT_[1]#	N/A	2	PCI	O	3.3V	Common clock
PAGNT_[0]#	N/A	2	PCI	O	3.3V	Common clock
PAIRDY#	N/A	2	PCI	I/O	3.3V	Common clock
PAIRQ_[15]#	HAMRL1#	2	PCI / Hot Plug	I	3.3V	Common clock
PAIRQ_[14]#	HAPWRFLT_1#	2	PCI / Hot Plug	I	3.3V	Common clock
PAIRQ_[13]#	HAPWRFLT_2#	2	PCI / Hot Plug	I	3.3V	Common clock
PAIRQ_[12]#	HAM66EN_2	2	PCI / Hot Plug	I	3.3V	Common clock
PAIRQ_[11]#	HAM66EN_1	2	PCI / Hot Plug	I	3.3V	Common clock

Table 2-13. Intel® 6702PXH 64-bit PCI Hub Signals, Interfaces and Power Planes (Sheet 3 of 4)

Intel® 6702PXH 64-bit PCI Hub Signal	Hot Plug Muxed Signal (Parallel Mode, 1-2 Slots)	No. of Signals	Interface	Type	Operating Voltage	Notes
PAIRQ_[10]#	HAPCIXCAP1_1	2	PCI / Hot Plug	I	3.3V	Common clock
PAIRQ_[9]#	HAPCIXCAP2_1	2	PCI / Hot Plug	I	3.3V	Common clock
PAIRQ_[8]#	HABUTTON_1#	2	PCI / Hot Plug	I	3.3V	Common clock
PAIRQ_[7]#	N/A	2	PCI	I	3.3V	Common clock
PAIRQ_[6]#	N/A	2	PCI	I	3.3V	Common clock
PAIRQ_[5]#	N/A	2	PCI	I	3.3V	Common clock
PAIRQ_[4]#	N/A	2	PCI	I	3.3V	Common clock
PAIRQ_[3]#	N/A	2	PCI	I	3.3V	Common clock
PAIRQ_[2]#	N/A	2	PCI	I	3.3V	Common clock
PAIRQ_[1]#	N/A	2	PCI	I	3.3V	Common clock
PAIRQ_[0]#	N/A	2	PCI	I	3.3V	Common clock
PAM66EN	N/A	2	PCI	I/O	3.3V	Common clock
PAPAR	N/A	2	PCI	I/O	3.3V/1.5V	Source-synchronous
PAPAR64	N/A	2	PCI	I/O	3.3V/1.5V	Source-synchronous
PAPCIRST#	N/A	2	PCI	O	3.3V	Common clock
PAPCIXCAP	N/A	2	PCI	I	3.3V	PCI/PCI-X Strap
PAPCLKI	N/A	2	PCI	I	3.3V	Common clock
PAPCLKO[6:0]	N/A	14	PCI	O	3.3V	Common clock
PAPERR#	N/A	2	PCI	I/O	3.3V	Common clock
PAPLOCK#	N/A	2	PCI	O	3.3V	Common clock
PAPME#	N/A	2	PCI	I	3.3V	Common clock
PAREQ_[5]#	HAPRSNT1_2#	2	PCI / Hot Plug	I/O	3.3V/1.5V	Source-synchronous
PAREQ_[4]#	HAPRSNT2_2#	2	PCI / Hot Plug	I	3.3V	Common clock
PAREQ_[3]#	HAPRSNT2_1#	2	PCI / Hot Plug	I	3.3V	Common clock
PAREQ_[2]#	N/A	2	PCI	I	3.3V	Common clock
PAREQ_[1]#	N/A	2	PCI	I	3.3V	Common clock
PAREQ_[0]#	N/A	2	PCI	I	3.3V	Common clock
PAREQ64#	N/A	2	PCI	I/O	3.3V/1.5V	Source-synchronous
PASERR#	N/A	2	PCI	I	3.3V	Common clock
PASTOP#	N/A	2	PCI	I/O	3.3V	Common clock
PASTRAP0	N/A	2	PCI	I	3.3V	Common clock
PATRDY#	N/A	2	PCI	I/O	3.3V	Common clock
PWROK	N/A	1	Miscellaneous	I	3.3V	Miscellaneous
RCOMP	N/A	1	PCI	I	0.75V	Analog Signal

Table 2-13. Intel® 6702PXH 64-bit PCI Hub Signals, Interfaces and Power Planes (Sheet 4 of 4)

Intel® 6702PXH 64-bit PCI Hub Signal	Hot Plug Muxed Signal (Parallel Mode, 1-2 Slots)	No. of Signals	Interface	Type	Operating Voltage	Notes
RESERVED	N/A	2	PCI	O	3.3V	Common clock
RESERVED	N/A	7	Miscellaneous	N/A	N/A	RESERVED
RSTIN#	N/A	1	Miscellaneous	I	3.3V	Reset
SCLK	N/A	1	SMBus	I	3.3V	SMBus clock
SDTA	N/A	1	SMBus	I/OD	3.3V	SMBus data
SMBUS[5]	N/A	1	SMBus	I	3.3V	SMBus strap
SMBUS[3]	N/A	1	SMBus	I	3.3V	SMBus strap
SMBUS[2]	N/A	1	SMBus	I	3.3V	SMBus strap
SMBUS[1]	N/A	1	SMBus	I	3.3V	SMBus strap
TCK	N/A	1	JTAG	I	3.3V	16MHz test clock for JTAG
TDI	N/A	1	JTAG	I	3.3V	Test interface
TDO	N/A	1	JTAG	O	3.3V	Test interface
TMS	N/A	1	JTAG	I	3.3V	Test interface
TRST#	N/A	1	JTAG	I	3.3V	Test interface
VCC	N/A	18	1.5V core voltage	N/A	1.5V	Supply voltage
VCC15	N/A	17	1.5V I/O voltage	N/A	1.5V	Supply voltage
VCC33	N/A	31	3.3V PCI voltage	N/A	3.3V	Supply voltage
VCCAEXP	N/A	1	PCI Express	N/A	1.5V	Analog voltage
VCCAPCI[2:0]	N/A	3	PCI	I	1.5V	Analog voltage
VCCBGEXP	N/A	1	PCI Express	N/A	2.5V	Analog voltage
VCCEXP	N/A	9	PCI Express	N/A	1.5V	Supply voltage
VREFPCI	N/A	1	PCI	I	VCC/2 ±3%	Analog reference
VSS	N/A	143	Ground	N/A	0V	Ground
VSSAEXP	N/A	1	Ground	N/A	0V	Analog ground
VSSBGEXP	N/A	1	Ground	N/A	0V	Analog ground

2.11.2 Power Planes

Table 2-14. Intel® 6702PXH 64-bit PCI Hub Platform Power Planes

Plane	Signal	Description
Core Voltage 1.5V	VCC	Provides the core power for the Intel® 6702PXH 64-bit PCI Hub.
PCI Express* Voltage 1.5V	VCCEXP	Provides Voltage for the PCI Express Interface.
1.5V I/O Voltage 1.5V	VCC15	1.5V I/O Voltage.
PCI/PCI-X Mode 1 Voltage 3.3V	VCC33	Provides 3.3V for the PCI and PCI-X Mode 1 operations.
Bandgap Voltage 2.5V	VCC25	Needed for Bandgap Analog Filter.

2.11.3 Signals and Default States

Table 2-15. Intel® 6702PXH 64-bit PCI Hub Signals and Default States (Sheet 1 of 3)

Signal	Power Plane	Type	During Reset	Immediately After Reset
HAATNLED_1#	3.3V	O	High-Z	HAATENLED_1#: Undefined
HAPWREN_1	3.3V	O	High-Z	Pulled High
HPA_PRST#	3.3V	O	High	High
HPA_RST2#	3.3V	O	High-Z	High
HPA_SIC	3.3V	I	High-Z	Undefined
HPA_SID	3.3V	I	High-Z	Undefined
HPA_SIL#	3.3V	I	High-Z	Pulled High
HPASLOT[3]	3.3V	I	High-Z	Undefined
HPASLOT[2]	3.3V	I	High-Z	Undefined
HPASLOT[1]	3.3V	I	High-Z	Undefined
HPASLOT[0]	3.3V	I	High-Z	Undefined
HPASOC	3.3V	O	High-Z	Pulled High
HPASOD	3.3V	O	High-Z	Pulled High
HPASOL	3.3V	O	High-Z	Pulled High
HPASOLR	3.3V	O	Undefined	Pulled High
PA133EN	3.3V	I	High-Z	Undefined
PAACK64#	3.3V/1.5V	I/O	High-Z	Pulled High
PAAD[63:0]	3.3V/1.5V	I/O	High-Z	Pulled High
PACBE_[7]#	3.3V/1.5V	I/O	High-Z	Pulled High

Table 2-15. Intel® 6702PXH 64-bit PCI Hub Signals and Default States (Sheet 2 of 3)

Signal	Power Plane	Type	During Reset	Immediately After Reset
PACBE_[6]#	3.3V/1.5V	I/O	High-Z	Pulled High
PACBE_[5]#	3.3V/1.5V	I/O	High-Z	Pulled High
PACBE_[4]#	3.3V/1.5V	I/O	High-Z	Pulled High
PACBE_[3]#	3.3V/1.5V	I/O	High-Z	Pulled High
PACBE_[2]#	3.3V/1.5V	I/O	High-Z	Pulled High
PACBE_[1]#	3.3V/1.5V	I/O	High-Z	Pulled High
PACBE_[0]#	3.3V/1.5V	I/O	High-Z	Pulled High
PADEVSEL#	3.3V	I/O	High-Z	Pulled High
PAFRAME#	3.3V	I/O	High-Z	Pulled High
PAGNT_[5]#	3.3V	O	High	Pulled High
PAGNT_[4]#	3.3V/1.5V	O	High	Pulled High
PAGNT_[3]#	3.3V/1.5V	O	High	Pulled High
PAGNT_[2]#	3.3V/1.5V	O	High	Pulled High
PAGNT_[1]#	3.3V	O	High	Pulled High
PAGNT_[0]#	3.3V	O	High	Pulled High
PAIRDY#	3.3V	I/O	High-Z	Pulled High
PAIRQ_[15]#	3.3V	I	High-Z	Pulled High
PAIRQ_[14]#	3.3V	I	High-Z	Pulled High
PAIRQ_[13]#	3.3V	I	High-Z	Pulled High
PAIRQ_[12]#	3.3V	I	High-Z	Undefined
PAIRQ_[11]#	3.3V	I	High-Z	Undefined
PAIRQ_[10]#	3.3V	I	High-Z	Pulled High
PAIRQ_[9]#	3.3V	I	High-Z	Pulled High
PAIRQ_[8]#	3.3V	I	High-Z	Pulled High
PAIRQ_[7]#	3.3V	I	High-Z	Pulled High
PAIRQ_[6]#	3.3V	I	High-Z	Pulled High
PAIRQ_[5]#	3.3V	I	High-Z	Pulled High
PAIRQ_[4]#	3.3V	I	High-Z	Pulled High
PAIRQ_[3]#	3.3V	I	High-Z	Pulled High
PAIRQ_[2]#	3.3V	I	High-Z	Pulled High
PAIRQ_[1]#	3.3V	I	High-Z	Pulled High
PAIRQ_[0]#	3.3V	I	High-Z	Pulled High
PAM66EN	3.3V	I/O	High-Z	Undefined
PAPAR	3.3V/1.5V	I/O	High-Z	Pulled High
PAPAR64	3.3V/1.5V	I/O	High-Z	Pulled High
PAPCIXCAP	3.3V	I	High-Z	Pulled High
PAPERR#	3.3V	I/O	High-Z	Pulled High
PAPLOCK#	3.3V	O	High-Z	Pulled High

Table 2-15. Intel® 6702PXH 64-bit PCI Hub Signals and Default States (Sheet 3 of 3)

Signal	Power Plane	Type	During Reset	Immediately After Reset
PAPME#	3.3V	I	High-Z	Undefined
PAREQ_[5]#	3.3V/1.5V	I/O	High-Z	Pulled High
PAREQ_[4]#	3.3V	I	High-Z	Pulled High
PAREQ_[3]#	3.3V	I	High-Z	Pulled High
PAREQ_[2]#	3.3V	I	High-Z	Pulled High
PAREQ_[1]#	3.3V	I	High-Z	Pulled High
PAREQ_[0]#	3.3V	I	High-Z	Pulled High
PAREQ64#	3.3V/1.5V	I/O	High-Z	Pulled High
PASERR#	3.3V	I	High-Z	Pulled High
PASTOP#	3.3V	I/O	High-Z	Pulled High
PASTRAP0	3.3V	I	High-Z	Pulled Low
PATRDY#	3.3V	I/O	High-Z	Pulled High
SCLK	3.3V	I	High-Z	High-Z
SDTA	3.3V	I/O	High-Z	High-Z
SMBUS[5]	3.3V	I	High-Z	Undefined
SMBUS[3]	3.3V	I	High-Z	Undefined
SMBUS[2]	3.3V	I	High-Z	Undefined
SMBUS[1]	3.3V	I	High-Z	Undefined

2.12 PCI/PCI-X Interface

2.12.1 Initialization

The Intel® 6702PXH 64-bit PCI Hub is the source bridge for the PCI bus. The Intel® 6702PXH 64-bit PCI Hub senses the PAM66EN, PA133EN, and the PAPCIXCAP pins to decide the mode and frequency of operation (when not in hot plug mode or when in one-slot-no-glue hot plug mode).

Table 2-16. PCI/PCI-X Mode and Frequency Encoding (Sheet 1 of 2)

PCI Capability	PCI-X Capability	PAM66EN	PA133EN	PAPCIXCAP (on the card)
33 MHz	Not Capable	GND	X	GND
66 MHz	Not Capable	Pull-up	X	GND
33 MHz	PCI-X 66 MHz	GND	X	Pull-down
66 MHz	PCI-X 66 MHz	No Connect	X	Pull-down
33 MHz	PCI-X 100 MHz	GND	Pull-down	Capacitor to GND
66 MHz	PCI-X 100 MHz	No Connect	Pull-down	Capacitor to GND
33 MHz	PCI-X 133 MHz	GND	Pull-up	Capacitor to GND

Table 2-16. PCI/PCI-X Mode and Frequency Encoding (Sheet 2 of 2)

PCI Capability	PCI-X Capability	PAM66EN	PA133EN	PAPCIXCAP (on the card)
66 MHz	PCI-X 133 MHz	No Connect	Pull-up	Capacitor to GND

Once the Intel® 6702PXH 64-bit PCI Hub identifies the capabilities of the PCI bus devices, it drives the initialization pattern on the PADEVSEL#, PASTOP#, PATRDY#, PAFRAME# and PAIRDY# pins as per Table 2-17 to initialize the PCI bus devices to the proper mode and frequency.

Table 2-17. PCI-X Initialization Pattern Driven by the Intel® 6702PXH 64-bit PCI Hub

PAPERR#	PADEVSEL#	PASTOP#	PATRDY#	Mode	Clock Period (ns)		Clock Freq (MHz)	
					Max	Min	Min	Max
Deasserted	Deasserted	Deasserted	Deasserted	PCI	•	30	0	33
				PCI	30	15	33	66
Deasserted	Deasserted	Deasserted	Asserted	PCI-X Mode 1	20	15	50	66
Deasserted	Deasserted	Asserted	Deasserted	PCI-X Mode 1	15	10	66	100
Deasserted	Deasserted	Asserted	Asserted	PCI-X Mode 1	10	7.5	100	133
Deasserted	Asserted	Deasserted	Deasserted	PCI-X Mode 1	Reserved[1]			
Deasserted	Asserted	Deasserted	Asserted	PCI-X Mode 1	Reserved[1]			
Deasserted	Asserted	Asserted	Deasserted	PCI-X Mode 1	Reserved[1]			
Deasserted	Asserted	Asserted	Asserted	PCI-X Mode 1	Reserved[1]			

NOTE: The Intel® 6702PXH 64-bit PCI Hub never drives these patterns on the rising edge of PAPCIRST# signal; however, these patterns may appear before the signals settle to a steady value at the rising edge of PAPCIRST#.

2.12.2 Transaction Types

2.12.2.1 PCI Transactions

Table 2-18 lists the PCI transactions supported by the Intel® 6702PXH 64-bit PCI Hub. As a PCI master, the Intel® 6702PXH 64-bit PCI Hub has full access to the 64-bit address space and can generate dual address cycles (DAC). As a target, the Intel® 6702PXH 64-bit PCI Hub can accept dual address cycles up to the full 64-bit address space. The Intel® 6702PXH 64-bit PCI Hub supports linear increment address mode only for bursting memory transfers (indicated when the low 2 address bits are equal to 0). If either of these address bits is nonzero, the Intel® 6702PXH 64-bit PCI Hub disconnects the transaction after the first data transfer.

The Intel® 6702PXH 64-bit PCI Hub decodes all PCI cycles in medium PADEVSEL# timing.

Table 2-18. Intel® 6702PXH 64-bit PCI Hub PCI Transactions

Type of Transaction		Intel® 6702PXH 64-bit PCI Hub As		Type of Transaction		Intel® 6702PXH 64-bit PCI Hub As	
		Master	Target			Master	Target
0000	Interrupt acknowledge	No	No	1000	Reserved[1]	No	No
0001	Special cycle	Yes	No	1001	Reserved[1]	No	No
0010	I/O read	Yes	No	1010	Configuration Read	Yes	No
0011	I/O write	Yes	No	1011	Configuration Write	Yes	No
0100	Reserved[1]	No	No	1100	Memory Read Multiple	No	Yes
0101	Reserved[1]	No	No	1101	Dual Address Cycle	Yes	Yes
0110	Memory read	Yes	Yes	1110	Memory Read Line	No	Yes
0111	Memory write	Yes	Yes	1111	Memory Write and Invalidate	No	Yes

NOTE:
1. The Intel® 6702PXH 64-bit PCI Hub never initiates a PCI transaction with a reserved command code and ignores reserved command codes as a target.

2.12.2.2 PCI-X Transactions

Table 2-19 lists the transactions supported by the Intel® 6702PXH 64-bit PCI Hub when the PCI Interface is in PCI-X mode.

Table 2-19. PCI-X Transactions Supported

Type of Transaction		Intel® 6702PXH 64-bit PCI Hub As		Type of Transaction		Intel® 6702PXH 64-bit PCI Hub As	
		Master	Target			Master	Target
0000	Interrupt acknowledge	No	No	1000	Alias to Memory Read Block	No	Yes
0001	Special cycle	Yes	No	1001	Alias to Memory Write Block	No	Yes
0010	I/O read	Yes	No	1010	Configuration Read	Yes	No
0011	I/O write	Yes	No	1011	Configuration Write	Yes	No
0100	Reserved	No	No	1100	Split Completion	Yes	Yes
0101	Reserved	No	No	1101	Dual Address Cycle	Yes	Yes
0110	Memory Read DWord	Yes	Yes	1110	Memory Read Block	Yes	Yes
0111	Memory Write	Yes	Yes	1111	Memory Write Block	Yes	Yes

2.12.3 Read Transactions

2.12.3.1 Prefetchable

Any memory read line or memory read multiple commands on the PCI bus that are decoded by the Intel® 6702PXH 64-bit PCI Hub are prefetched on the PCI Express interface. The amount of data prefetched depends on the clock frequency, PAREQ64#, and command type. The Intel® 6702PXH 64-bit PCI Hub does not prefetch past a 4-Kbyte page boundary.

2.12.3.2 Delayed

All memory read transactions are delayed read transactions. When the Intel® 6702PXH 64-bit PCI Hub accepts a delayed read request, it samples the address, command, and address parity. This information is entered into the delayed transaction queue. When in PCI-X mode, transactions follow the split transaction model of PCI-X. Read data returned from PCI Express for an active delayed transaction entry is forwarded to the PCI-X master as a split completion.

2.12.3.3 Internal CSR Space

Memory reads to internal CSR space are handled with an immediate completion on the PCI bus (in both PCI and PCI-X modes). The Intel® 6702PXH 64-bit PCI Hub never asserts PAACK64# for memory transactions to CSR space and hence CSR reads are 32-bit transactions. Reads to CSR memory bypass the normal inbound queues towards PCI Express and complete on the PCI bus within 16 PCI clocks. The Intel® 6702PXH 64-bit PCI Hub disconnects CSR memory reads after the first data-phase, i.e. the Intel® 6702PXH 64-bit PCI Hub does not support PCI burst read accesses to CSR memory space. Since the CSR space is non-prefetchable, only the bytes requested within the DWord are returned.

Note: Since CSR reads bypass the PCI Express queues, semaphore reads to CSR space do not push upstream writes that might contain the payload. In such cases, software must do a dummy read to PCI Express to push the upstream writes.

2.12.4 Configuration Transactions

Type 0 configuration transactions are issued when the intended target resides on the same PCI bus as the initiator. A Type 0 configuration transaction is identified by the configuration command and the lowest 2 bits of the address set to 00b.

Type 1 configuration transactions are issued when the intended target resides on another PCI bus, or when a special cycle is to be generated on another PCI bus. A Type 1 configuration command is identified by the configuration command and the lowest 2 address bits set to 01b.

The register number is found in both Type 0 and Type 1 formats and gives the DWord address of the configuration register to be accessed. The function number is also included in both Type 0 and Type 1 formats and indicates which function of a multifunction device is to be accessed. For single-function devices, this value is not decoded. Type 1 configuration transaction addresses also include a 5-bit field designating the device number that identifies the device on the target PCI bus that is to be accessed. In addition, the bus number in Type 1 transactions specifies the PCI bus to which the transaction is targeted.

2.12.5 Transaction Termination

2.12.5.1 PCI Mode Transaction Termination

2.12.5.1.1 Normal Master Termination

As a PCI master, the Intel® 6702PXH 64-bit PCI Hub uses normal termination if PADEVSEL# is returned by the target within five clock cycles of PAFRAME# assertion. It terminates a transaction when the following conditions are met:

- All write data for the transaction is transferred from the Intel® 6702PXH 64-bit PCI Hub data buffers to the target.
- All read data for a read transaction have been transferred from the target to the Intel® 6702PXH 64-bit PCI Hub.
- The master latency timer expires and the Intel® 6702PXH 64-bit PCI Hub's bus grant is de-asserted.

2.12.5.1.2 Master Abort Termination

If an Intel® 6702PXH 64-bit PCI Hub initiated transaction does not get a response with PADEVSEL# within five clocks of PAFRAME# assertion, the Intel® 6702PXH 64-bit PCI Hub terminates the transaction with a master abort. The Intel® 6702PXH 64-bit PCI Hub sets the received master abort bit in the status register corresponding to the target bus. Read requests (configuration, I/O, or memory) that receive master abort termination are sent back to the PCI Express bus (or peer PCI bus for Intel® 6702PXH 64-bit PCI Hub) with a master abort status. Delayed write requests that receive a master abort are sent back to PCI Express with master abort status.

Note: When the Intel® 6702PXH 64-bit PCI Hub performs a Type 1 to special cycle translation, a master abort is the expected termination for the special cycle on the target bus. In this case, the master abort received bit is not set, and the Type 1 configuration transaction is disconnected after the first data phase.

2.12.5.1.3 Target Termination Received by the Intel® 6702PXH 64-bit PCI Hub

If the Intel® 6702PXH 64-bit PCI Hub receives a target abort, and the cycle requires completion on the PCI Express bus, the Intel® 6702PXH 64-bit PCI Hub will return the target abort status to PCI Express. The Intel® 6702PXH 64-bit PCI Hub sets the received target abort status bit in the secondary status register for all target aborts it receives on the PCI bus. Target abort can happen on any data phase of a PCI-X transaction, and a read completion packet to PCI Express (or peer PCI bus for Intel® 6702PXH 64-bit PCI Hub) incurring a target abort in the middle would return valid data to the point of the target abort and a target abort completion status for the remainder.

2.12.5.1.4 Disconnect and Retry

If the Intel® 6702PXH 64-bit PCI Hub receives a disconnect response from a target, it will re-initiate the transfer with the remaining length. When the Intel® 6702PXH 64-bit PCI Hub receives a retry, it will wait at least two PCI clocks before it retries the transaction. If the retried transaction is a write, the Intel® 6702PXH 64-bit PCI Hub will retry the write until it completes normally, or with a target or master abort. If the retried transaction is a delayed read or delayed write

transaction, the Intel® 6702PXH 64-bit PCI Hub will allow memory reads and writes to pass the transaction. A retry is not considered an error condition, and so there is no error logging or reporting done on a retry.

2.12.5.1.5 Target Termination Initiated by the Intel® 6702PXH 64-bit PCI Hub

The Intel® 6702PXH 64-bit PCI Hub returns a target retry to an initiator when any of the following conditions is met:

- A new memory read transaction occurs and the Intel® 6702PXH 64-bit PCI Hub delayed transaction queue is full.
- A memory read occurs that has already been queued, but has not completed on the PCI Express bus.
- A memory read occurs that has been queued and completed on the PCI Express bus but ordering rules require an outbound posted write to complete ahead of it.
- A memory read or write to CSR space occurs and a previously posted write to CSR space has not yet internally completed.
- A LOCK transaction is established from the PCI Express to the PCI bus.
- A memory write transaction occurs and the Intel® 6702PXH 64-bit PCI Hub has no free buffer space to accept the write.
- A memory write occurs from a master other than the master that was previously retried (this is a starvation prevention mechanism).
- A previously posted memory write to CSR space has not yet internally completed.
- The Configuration Lockout bit is set in the PXH_CONFIG register and the Intel® 6702PXH 64-bit PCI Hub is being configured locally after a cold boot sequence or during normal system operation.

The Intel® 6702PXH 64-bit PCI Hub disconnects an initiator when one of the following conditions is met:

- The Intel® 6702PXH 64-bit PCI Hub cannot accept any more write data.
- The Intel® 6702PXH 64-bit PCI Hub has no more read data to deliver.
- The memory address is non-linear.
- CSR memory reads and writes after the first data phase occur.
- Configuration reads and writes after the first data phase occur.
- The inverse decode window ends.

The Intel® 6702PXH 64-bit PCI Hub returns a target abort to the PCI bus when:

- The cycle master aborted or target aborted on the PCI Express bus (or the peer PCI bus for Intel® 6702PXH 64-bit PCI Hub).
- Configuration reads and writes occur with address or data parity errors.
- CSR memory reads and writes occur with address or data parity errors.

2.12.5.2 PCI-X Mode Transaction Termination

2.12.5.2.6 Initiator Disconnect or Satisfaction of Byte Count

As a PCI-X master, the Intel® 6702PXH 64-bit PCI Hub uses normal termination (initiator disconnect or satisfaction of byte count) if PADEVSEL# is returned by the target within six clock cycles after the address phase. The Intel® 6702PXH 64-bit PCI Hub terminates a transaction when one of the following conditions are met:

- All write data indicated in the byte count of the write transaction is transferred from Intel® 6702PXH 64-bit PCI Hub data buffers to the target. The Intel® 6702PXH 64-bit PCI Hub never does an initiator disconnect on a write before the byte count size has been satisfied.
- An initiator disconnect occurs at the next ADB on a split read completion because the Intel® 6702PXH 64-bit PCI Hub data buffer has run dry.
- An initiator disconnect at the next ADB when the master latency timer has expired and the Intel® 6702PXH 64-bit PCI Hub's bus grant signal is de-asserted.

2.12.5.2.7 Master Abort Termination

If a Intel® 6702PXH 64-bit PCI Hub initiated transaction is not responded to with PADEVSEL# within six clocks after address phase, the Intel® 6702PXH 64-bit PCI Hub terminates the transaction with a master abort. The Intel® 6702PXH 64-bit PCI Hub sets the received master abort bit in the secondary status register. Read requests (configuration, I/O, memory) that receive master abort termination are sent back to PCI Express / peer PCI with a master abort status. Delayed write requests that receive master abort are sent back to PCI Express with a master abort status.

Note: When the Intel® 6702PXH 64-bit PCI Hub performs a Type 1 to special cycle translation, a master abort is the expected termination for the special cycle on the target bus. In this case, the master abort received bit is not set, and the Type 1 configuration transaction is disconnected after the first data phase.

2.12.5.2.8 Target Termination Received by the Intel® 6702PXH 64-bit PCI Hub

If the Intel® 6702PXH 64-bit PCI Hub receives a target abort, and the cycle requires completion on the PCI Express bus, the Intel® 6702PXH 64-bit PCI Hub will return the target abort status to PCI Express. The Intel® 6702PXH 64-bit PCI Hub sets the received target abort status bit in the secondary status register for all target aborts it receives on the PCI bus. Target abort can happen on any data phase of a PCI-X transaction, and a read completion packet to PCI Express / peer PCI, incurring a target abort in the middle of the packet would return valid data to the point of target abort and all 1s for the reminder of the length and a target abort completion status for the entire packet.

2.12.5.2.9 Disconnect and Retry

If the Intel® 6702PXH 64-bit PCI Hub receives a disconnect response (single data phase or at next ADB) from a target, it will re-initiate the transfer with the remaining length. When the Intel® 6702PXH 64-bit PCI Hub receives a retry, it will wait at least two PCI clocks before it retries the transaction. If the retried transaction is a write, the Intel® 6702PXH 64-bit PCI Hub will retry the write till it completes normally or with a target or master abort. If the retried transaction is

a delayed read or delayed write transaction, the Intel® 6702PXH 64-bit PCI Hub will allow memory reads, split completions and writes to pass the transaction. A retry is not considered an error condition and so there is no error logging or reporting done on a retry.

2.12.5.2.10 Split Response

The Intel® 6702PXH 64-bit PCI Hub can receive split response for memory reads, I/O and configuration read and write transactions.

2.12.5.2.11 Target Termination Initiated by the Intel® 6702PXH 64-bit PCI Hub

The Intel® 6702PXH 64-bit PCI Hub returns a target retry to an initiator when any of the following conditions is met:

- A new memory read transaction and the Intel® 6702PXH 64-bit PCI Hub delayed transaction queue is full.
- A memory read or write to CSR space and a previously posted write to CSR space has not yet internally completed.
- A LOCK transaction has been established from PCI Express to PCI.
- A memory write transaction and the Intel® 6702PXH 64-bit PCI Hub has no free buffer space to accept the write.
- A memory write is from a master other than the master that was previously retried (starvation prevention mechanism).
- A configuration transaction to the secondary configuration space and a previously posted memory write to CSR space has not yet internally completed.
- The Configuration Lockout bit is set in the PXH_CONFIG register and the Intel® 6702PXH 64-bit PCI Hub is being configured locally after a cold boot sequence or during normal system operation.

The Intel® 6702PXH 64-bit PCI Hub never retries a completion since it always has enough buffer space for all split requests it sends out. No transaction information is retained on any writes.

The Intel® 6702PXH 64-bit PCI Hub disconnects an initiator when one of the following conditions is met:

- The Intel® 6702PXH 64-bit PCI Hub cannot accept any more write data and an ADB is reached.
- A split completion packet is being sent, an ADB is reached, and the Intel® 6702PXH 64-bit PCI Hub read buffers are running dry.
- A CSR memory read or write occurs after the first data phase.
- The inversed decode window ends and an inbound write is in progress, regardless of write buffer availability.

The Intel® 6702PXH 64-bit PCI Hub returns a target abort to PCI when:

- A split completion packet is sent to a PCI-X agent and the split cycle target aborted on the PCI Express bus (or peer PCI bus for Intel® 6702PXH 64-bit PCI Hub).
- A configuration read or write occurs with address or data parity errors or attribute phase parity errors.

- A CSR memory read or write occurs with address or data parity errors or attribute phase parity errors.

All memory read cycles that cross the Intel® 6702PXH 64-bit PCI Hub receive a split transaction termination, if they are not retried.

2.12.5.3 Intel® 6702PXH 64-bit PCI Hub Termination on Device Boundary Crossing

On the PCI-X bus, any split request to the Intel® 6702PXH 64-bit PCI Hub that crosses a BAR boundary (initial address + length > BAR limit) will result in a normal response up to the BAR range and a "byte count out of range" response for the reminder of the length.

2.12.6 PCI-X Protocol Specifics

2.12.6.1 Attributes

Table 2-20 describes how the Intel® 6702PXH 64-bit PCI Hub fills in attribute fields where the PCI-X bus specification leaves some implementation leeway.

Table 2-20. Intel® 6702PXH 64-bit PCI Hub Implementation of Requester Attribute Fields

Attribute	Function
No Snoop (NS)	The Intel® 6702PXH 64-bit PCI Hub just forwards this attribute in both directions and does nothing with it internally.
Relaxed Ordering (RO)	This bit allows relaxed ordering of transactions, which the Intel® 6702PXH 64-bit PCI Hub does not permit. This bit is simply forwarded in the Intel® 6702PXH 64-bit PCI Hub, and is never generated on the PCI-X bus from a PCI Express* packet, or vice-versa.
Tag	Since the Intel® 6702PXH 64-bit PCI Hub can have two outstanding requests on the PCI-X bus at a time, this field can be either 0 or 1.
Byte Counts	This is based upon the length field from PCI Express, which is DWord-based.

2.12.6.2 4-Gbyte and 4-Kbyte Page Crossover

The PCI-X bus specification allows burst transactions to cross page (in the Intel® 6702PXH 64-bit PCI Hub's case, this is 4 Kbytes) and 4-Gbyte address boundaries. As a PCI-X bus master, the Intel® 6702PXH 64-bit PCI Hub will always end the transaction at a 4-Kbyte boundary. As a PCI-X bus target, the Intel® 6702PXH 64-bit PCI Hub will allow a burst past a 4-Kbyte page boundary. Note that on the PCI Express bus, requests never cross a 4-Kbyte boundary on reads or writes.

2.12.6.3 Wait States

The Intel® 6702PXH 64-bit PCI Hub will never generate wait states as a target except in the case of CSR memory reads and configuration read and write accesses, which are handled with immediate completions.

2.12.6.4 Split Transactions

2.12.6.4.12 Completer Attributes

Table 2-21. Intel® 6702PXH 64-bit PCI Hub Implementation Completion Attribute Fields

Attribute	Function
Byte Count Modified (BCM)	The Intel® 6702PXH 64-bit PCI Hub sets this bit only in NT mode when the burst read starts from within 3 data phases of the BAR boundary and crosses the BAR boundary.
Split Completion Error (SCE)	The Intel® 6702PXH 64-bit PCI Hub will only set this bit if a memory read command from PCI-X master or target aborted on the PCI Express* bus, and also for byte count out-of-range error in NT mode.
Split Completion Message (SCM)	This bit shadows the SCE bit.

2.12.6.4.13 Requirements for Accepting Split Completions

The Intel® 6702PXH 64-bit PCI Hub asserts PADEVSEL# and discards the data if the Requester ID matches the bridge, but the tag does not match that of any outstanding requests from this device.

2.12.6.4.14 Split Completion Messages

The Intel® 6702PXH 64-bit PCI Hub can only generate error messages for cycles that cross the bridge and which master or target abort. No DWord cycles that require completion (i.e. I/O cycles) will cross the bridge. Therefore, the Intel® 6702PXH 64-bit PCI Hub can only generate a “PCI-X Bridge Error” completion message for the memory read commands as indicated in Table 2-22.

Table 2-22. Split Completion Abort Registers

Index	Message
00h	**Master-Abort:** The Intel® 6702PXH 64-bit PCI Hub encountered a Master-Abort on the destination bus.
01h	**Target-Abort:** The Intel® 6702PXH 64-bit PCI Hub encountered a Target-Abort on the destination bus.

2.12.7 LOCK Cycles

A lock is established when a memory read from the PCI Express bus that targets a PCI bus agent with the lock bit set is responded to with a PATRDY# by a PCI target. The bus is unlocked when the Unlock Special Cycle is sent on the PCI Express interface. When the PCI bus is locked, all inbound memory transactions from that bus are retried. The Intel® 6702PXH 64-bit PCI Hub inbound read prefetch engine stops issuing any more requests on the PCI Express bus. Note though that read completions for inbound read requests issued ahead of the lock being established on the PCI bus could return on the PCI Express bus after the PCI lock has been established, and the Intel® 6702PXH 64-bit PCI Hub accepts them.

Once the bus is locked, any PCI Express cycle to PCI will be driven with the PALOCK# pin asserted, even if that particular cycle is not locked. This should not occur, because under lock, peer-to-peer accesses will be internally blocked and the MCH should not be sending any non-locked transactions downstream.

When one PCI bus segment is locked on the Intel® 6702PXH 64-bit PCI Hub the other is still free to accept cycles, i.e. that bus is not locked. However, these cycles are not allowed to proceed on the PCI Express bus or the locked PCI segment. Therefore, once the PCI bus is locked, no more cycles will proceed onto the PCI Express bus from the non-locked PCI segment, or from the I/OxAPIC(s).

If during the LOCK sequence, any of the locked read commands results in a master or target abort (either on the PCI bus or the internal switch interconnect), then the Intel® 6702PXH 64-bit PCI Hub loses lock after sending a completion packet on the PCI Express bus. In the case of a memory write receiving a target or master abort during a LOCK sequence, the Intel® 6702PXH 64-bit PCI Hub only unlocks after the unlock message is received on the PCI Express bus. Outbound LOCK is supported by the Intel® 6702PXH 64-bit PCI Hub.

Inbound LOCK transactions are treated with the LOCK signal ignored. Also locks to internal devices, the SHPC, or the I/OxAPIC are not supported by the Intel® 6702PXH 64-bit PCI Hub. See the summary in Table 2-23 for a summary of Intel® 6702PXH 64-bit PCI Hub responses to LOCK transactions.

Table 2-23. LOCK Transaction Handling

End Point	Source	
	PCI	PCI Express*
SHPC Memory	Ignore[2]	Error Reported[1]
I/OxAPIC	Ignore[2]	Error Reported[1]
CSR Memory	N/A	N/A
PCI	N/A	Forward to PCI with PALOCK#
PCI Express*	Ignore[2]	N/A

NOTES:
1. For locked reads, a response of UR-EC is reported on the PCI Express* bus.
2. The transaction is treated as if it were a normal read or write transaction.

2.13 Hot Plug Controllers

The Intel® 6702PXH 64-bit PCI Hub hot plug controller allows PCI card removal, replacement, and addition without powering down the system. The controller is compatible with the *PCI Standard Hot-Plug Controller and Subsystem Specification*, Revision 1.0. The specification includes two new register sets that are defined for the SHPC Capabilities List and the SHPC Working Register Set. The new registers are defined as a PCI-PCI bridge capability in the Intel® 6702PXH 64-bit PCI Hub and not as a separate PCI controller device. The new specification also fixes the architectural proximity of the SHPC function to the PCI slots it controls. The Intel® 6702PXH 64-bit PCI Hub may only control slots on its secondary bus(es) and there must be a separate SHPC function associated with each of the logical PCI-PCI bridge configuration spaces. The Standard Hot-Plug Controller in the Intel® 6702PXH 64-bit PCI Hub can control a maximum of 6 slots in the system. It supports three to six PCI slots through an input/output serial interface when operating in Serial Mode, and 1 to 2 slots through an input/output parallel interface when operating in Parallel Mode. The input serial interface is polling and is in continuous operation. The output serial interface is “demand” and acts only when requested. These serial interfaces run at about 8.25 MHz regardless of the speed of the PCI bus. In parallel mode, the Intel® 6702PXH 64-bit PCI Hub performs the serial to parallel conversion internally, so the serial interface cannot be observed. However, internally the hot plug controller always operates in a serial mode.

2.13.1 Mode Determination

The standard hot plug controller is enabled and the mode selected through pin strappings that are sampled on the rising edge of PWROK signal. Table 2-24 shows the information. When the standard hot plug controller is disabled (HPA_SLOT[3] = “0”), the standard hot plug capability registers and the working register set are hidden from software and the standard hot plug controller is essentially disabled. The number of standard hot plug slots the controller handles is logged into the slot configuration register at offset 0Ch in the SHPC working register set. This register is a read-only register and cannot be written to by BIOS to change the mode of operation of the controller in the Intel® 6702PXH 64-bit PCI Hub (between serial and parallel).

Table 2-24. Hot Plug Mode Settings

HPA_SLOT[3:0]	# of Slots (Intel® 6702PXH 64-bit PCI Hub SHPC Mode)	Slot Configuration Register [4:0]
Hot Plug Disabled (see Note)		
0000	1 Slot	00001
0001	2 Slots	00010
0010	3 Slots	00011
0011	4 Slots	00100
0100	5 Slots	00101
0101	6 Slots	00110
0110	7 Slots	00111
0111	8 Slots	01000
Hot Plug Enabled		
1000	Reserved	N/A
1001	1-slot (parallel)	00001
1010	2-slot (parallel)	00010
1011	3-slot (serial)	00011
1100	4-slot (serial)	00100
1101	5-slot (serial)	00101
1110	6-slot (serial)	00110
1111	1-slot-no-glue (parallel)	00001

NOTE: HPA_SLOT[2:0] are optional when Hot Plug is disabled.

2.13.2 Output Control

The output interface is responsible for driving six bits per slot. These signals are mapped onto Intel® 6702PXH 64-bit PCI Hub pins as shown in Table 2-25 and Table 2-26 for serial mode and Table 2-27 for parallel mode.

- **POWER ENABLE:** Connected to an analog component designed to regulate current and voltage of the PCI slot, and generates a (power) fault signal when an abnormal condition is detected.
- **CLOCK ENABLE#:** Connects the PCI clock signals of the PCI slot to the PCI bus via FET isolation switches.
- **BUS ENABLE#:** Connects the PCI bus signals of the PCI slot to the system bus PCI bus via FET isolation switches.
- **RESET#:** Connected to the RST# pin of the PCI slot.
- **ATNLED#:** Connected to the optional attention LED, which is yellow or amber in color.
- **PWRLED#:** Connected to the power LED, which is green in color.

2.13.3 Input Control

The input interface captures eight inputs from each slot. These signals are mapped onto Intel® 6702PXH 64-bit PCI Hub pins as shown in Table 2-25 and Table 2-26 for serial mode and Table 2-27 for parallel mode.

- **FAULT#:** Over-current / Under-volt indication: When asserted, the Intel® 6702PXH 64-bit PCI Hub, if enabled, immediately asserts reset and disconnects the PCI slot from the bus.
- **PRSNT1# and PRSNT2#:** Signals which determine whether or not a card is installed to budget system power. These inputs are connected to the PRSNT1# and PRSNT2# pins on the PCI card.
- **M66EN:** Determines if a card is capable of running at 66 MHz in conventional PCI mode.

PRSNT1#	PRSNT2#	Meaning
1	1	No expansion card present
0	1	Expansion card present; 25 W maximum
1	0	Expansion card present; 15 W maximum
0	0	Expansion card present; 7.5 W maximum

- **PCIXCAP1 and PCIXCAP2:** Determines if a PCI slot is PCI-X capable, and if so, at which bus frequency it can operate.

PCIXCAP1	PCIXCAP2	Meaning
1	1	100/133 MHz PCI-X Mode
0	1	66 MHz PCI-X Mode
1	0	Reserved
0	0	PCI Mode

- **MRL#:** Manually operated retention latch sensor input. A logic low input that is connected directly to the MRL sensor. When asserted it indicates that the MRL latch is closed. If a platform does not support MRL sensors, this must be wired to a low logic level (MRL closed).
- **ATTENTION BUTTON#:** Signal connected to the PCI slot's attention button. When low, indicates that the operator has requested attention. If an attention button is not implemented, then this input must be wired to a high logic level.

2.13.4 Serial Mode Operation

During Serial mode operation, the Intel® 6702PXH 64-bit PCI Hub sends and receives information serially from the slot control logic. The slot control logic is required to deserialize the output information to the bus switches and slot. The Slot control logic is also required to convert parallel input information from the slots into serial data to the Intel® 6702PXH 64-bit PCI Hub. The serial interface will run at 16.5 MHz. In this mode, the Intel® 6702PXH 64-bit PCI Hub constantly polls the slot inputs, serially looking for an event at any of the hot plug slots. The output serial stream from the Intel® 6702PXH 64-bit PCI Hub is on-demand and is only sent when the Intel® 6702PXH 64-bit PCI Hub needs to schedule an event at a slot.

2.13.4.1 Serial Input Stream

The input stream shifted out by the Intel® 6702PXH 64-bit PCI Hub consists of 48 bits and is fixed. If the board implements less than 6 slots in serial mode, a bit stream value of 1 must be shifted into the Intel® 6702PXH 64-bit PCI Hub for the slot locations not implemented. The sequence is shown below. Since the control bits corresponding to a slot are clustered into a group and the control bits for slot 1 come last, the Intel® 6702PXH 64-bit PCI Hub does not support stutter mode.

Table 2-25. Serial Input Stream (Sheet 1 of 2)

Bit#	Value	Bit#	Value
1	Slot1_ATTNB	25	Slot4_ATTNB
2	Slot1_MRL	26	Slot4_MRL
3	Slot1_PWRFLT	27	Slot4_PWRFLT
4	Slot1_PRSNT1	28	Slot4_PRSNT1
5	Slot1_PRSNT2	29	Slot4_PRSNT2
6	Slot1_PCIXCAP1	30	Slot4_PCIXCAP1
7	Slot1_PCIXCAP2	31	Slot4_PCIXCAP2
8	Slot1_M66EN	32	Slot4_M66EN
9	Slot2_ATTNB	33	Slot5_ATTNB
10	Slot2_MRL	34	Slot5_MRL
11	Slot2_PWRFLT	35	Slot5_PWRFLT
12	Slot2_PRSNT1	36	Slot5_PRSNT1
13	Slot2_PRSNT2	37	Slot5_PRSNT2
14	Slot2_PCIXCAP1	38	Slot5_PCIXCAP1
15	Slot2_PCIXCAP2	39	Slot5_PCIXCAP2
16	Slot2_M66EN	40	Slot5_M66EN

Table 2-25. Serial Input Stream (Sheet 2 of 2)

Bit#	Value	Bit#	Value
17	Slot3_ATTNB	41	Slot6_ATTNB
18	Slot3_MRL	42	Slot6_MRL
19	Slot3_PWRFLT	43	Slot6_PWRFLT
20	Slot3_PRSNT1	44	Slot6_PRSNT1
21	Slot3_PRSNT2	45	Slot6_PRSNT2
22	Slot3_PCIXCAP1	46	Slot6_PCIXCAP1
23	Slot3_PCIXCAP2	47	Slot6_PCIXCAP2
24	Slot3_M66EN	48	Slot6_M66EN

2.13.4.2 Serial Output Stream

The sequence below shows how the slot outputs are scanned out in order. If the board implements less than six slots, then the serial input bits corresponding to those slots are arbitrary and are ignored by the Intel® 6702PXH 64-bit PCI Hub.

Every round of polling by the Intel® 6702PXH 64-bit PCI Hub involves shifting all 36 bits, regardless of the number of slots implemented. Bit 1 in Table 2-26 represents the first bit that shifted into the Intel® 6702PXH 64-bit PCI Hub in the sequence of 36 bits.

Table 2-26. Serial Output Stream

Bit#	Value	Bit#	Value
1	Slot6_PWREN	19	Slot3_PWREN
2	Slot6_CLKEN	20	Slot3_CLKEN
3	Slot6_BUSEN	21	Slot3_BUSEN
4	Slot6_RST	22	Slot3_RST
5	Slot61_PLED	23	Slot3_PLED
6	Slot61_ALED	24	Slot3_ALED
7	Slot5_PWREN	25	Slot2_PWREN
8	Slot5_CLKEN	26	Slot2CLKEN
9	Slot5_BUSEN	27	Slot2_BUSEN
10	Slot5_RST	28	Slot2_RST
11	Slot5_PLED	29	Slot2_PLED
12	Slot5_ALED	30	Slot2_ALED
13	Slot4_PWREN	31	Slot1_PWREN
14	Slot4_CLKEN	32	Slot1_CLKEN
15	Slot4_BUSEN	33	Slot1_BUSEN
16	Slot4_RST	34	Slot1_RST
17	Slot4_PLED	35	Slot1_PLED
18	Slot4_ALED	36	Slot1_ALED

2.13.5 Parallel Mode Operation

In parallel mode, the Intel® 6702PXH 64-bit PCI Hub provides 6 slot control outputs and 8 slot control inputs for each of the two slots it can control. The Intel® 6702PXH 64-bit PCI Hub operates in this mode if the number of hot plug slots implemented is either 1 or 2, as programmed into the slot configuration register.

If the number of slots is set to 1, then the Intel® 6702PXH 64-bit PCI Hub ignores the second port. Platforms must tie this port to its benign value. Refer to Table 2-27 for how the parallel hot plug mode pins are reused (muxed) with other Intel® 6702PXH 64-bit PCI Hub pins.

Table 2-27. Muxed Hot Plug Mode Signals Parallel Mode

Signal	Type	Multiplexed With
		Bus A
HAATNLED_1#	O	HAATNLED_1#
HAATNLED_2#	O	HPA_SOLR
HABUSEN_1#	O	PAGNT_[5]#
HABUSEN_2#	O	PAGNT_[4]#
HABUTTON_1#	I	PAIRQ_[8]#
HABUTTON_2#	I	HPA_SOL
HACLKEN_1#	O	HPA_SIL#
HACLKEN_2#	O	HPA_SOD
HAM66EN_1	I	PAIRQ_[11]#
HAM66EN_2	I	PAIRQ_[12]#
HAMRL_1#	I	PAIRQ_[15]#
HAMRL_2#	I	HPA_SLOT[0]
HAPCIXCAP1_1	I	PAIRQ_[10]#
HAPCIXCAP1_2	I	HPA_SID
HAPCIXCAP2_1	I	PAIRQ_[9]#
HAPCIXCAP2_2	I	HPA_SOC
HAPRSNT1_1#	I	HPA_SLOT[1]
HAPRSNT1_2#	I	PAREQ_[5]#
HAPRSNT2_1#	I	PAREQ_[3]#
HAPRSNT2_2#	I	PAREQ_[4]#
HAPWREN_1	O	HAPWREN_1
HAPWREN_2	O	PAGNT_[3]#
HAPWRFLT_1#	I	PAIRQ_[14]#
HAPWRFLT_2#	I	PAIRQ_[13]#
HAPWRLED_1#	O	HPA_SLOT[3]
HAPWRLED_2#	O	HPA_SIC
HARST_1#	O	HPA_PRST#
HARST_2#	O	HPA_RST2#

2.13.6 One-Slot-No-Glue Mode

When only 1 slot is implemented, bus and clock isolation switches are not required. It is not necessary to isolate the card from the Intel® 6702PXH 64-bit PCI Hub's I/O buffers. The Intel® 6702PXH 64-bit PCI Hub enters this mode if HPA_SLOT[3:0] is sampled as "1111". This section describes special requirements for how PCI bus signals are handled in this mode.

2.13.6.1 Driving Bus To Ground When PCI Card is Disconnected

When in one-slot-no-glue mode, all PCI signals are to be driven to ground when the PCI card is disconnected. The signals that must be driven to ground by the Intel® 6702PXH 64-bit PCI Hub are the following:

- PAAD[63:0], PACBE_[7:0]#, PAPAR, PAPAR64, PAREQ64#, PAACK64#
- PAFRAME#, PAIRDY#, PATRDY#, PASTOP#, PADEVSEL#, PALOCK#
- PAGNT_[2:0]#
- PAREQ_[2:0]#
- PAPERR#, PASERR#
- PAPCLKO[5:0] (Only driven to ground if enabled through the bridge – otherwise these outputs remain high. PAPCLKO[6] is not driven to ground because it is connected back to PAPCLKIN)
- PAIRQ_[7:0]#
- PAPME#

These signals will be driven back to their normal PCI levels at various times in the clock connection process. When a card is reconnected to the bus, it follows the following algorithm:

- Power is applied to the card. This does not affect any of the PCI signals that are now being driven to ground.
- After a fixed (refer to *Standard Hot-Plug Controller and Subsystem Specification,* Revision 1.0) period of time, the clock is connected to the card. When this occurs, PAPCLKO[5:0] will no longer be driven to ground, but will toggle normally (assuming that software has not disabled that particular PAPCLKO pin). In hot plug terms, this is the equivalent of the "CLKEN#" signal.
- After another fixed (refer to *Standard Hot-Plug Controller and Subsystem Specification,* Revision 1.0) period of time, the bus is connected to the card. When this occurs, The remaining signals listed above which were driven to ground will be driven to their default values, except for PAPCIRST#, which will continue to be driven to ground. The new signal values are listed below:
  - PAAD[63:0], PACBE_[7:0]#, PAPAR, PAPAR64, PAREQ64#, PAACK64# - driven
  - PAFRAME#, PAIRDY#, PATRDY#, PASTOP#, PADEVSEL#, PALOCK# - driven to VCC33 for one clock, then tri-stated
  - PAGNT_[5:0]# - driven to VCC33 for one clock, then tri-stated
  - PAPERR#, PASERR# - driven to VCC33 for one clock, then tri-stated
  - PAPME# - tri-stated
  - PAIRQ_[7:0]# - tri-stated

In hot plug terms, this is the equivalent of the “BUSEN#” signal.

- After a final fixed period of time, the card is taken out of reset. When this occurs, the PAPCIRST# pin will be continuously driven to VCC33. This algorithm could be altered (for example, the bus could be enabled before the clock). The implication, however, is that there are three communication signals from the hot plug logic (BUSEN#, CLKEN#, and PCIRST#) to I/O buffer logic to control the state of their corresponding pins.

2.13.6.2 Aborting Outbound PCI Cycles When Card is Disconnected

When a PCI card is not present in a multi-slot system, it has been isolated. This means that all cycles destined for that particular card (peer traffic or other CPU based traffic) will master abort on the PCI bus because no PADEVSEL# will be driven. To be consistent in a single-slot system, the Intel® 6702PXH 64-bit PCI Hub must master abort cycles that are destined for that PCI bus when the card is disconnected. Therefore, the buffer interface will have to internally master abort all outbound transactions destined for that PCI bus until card is connected again.

2.13.7 Initialization

2.13.7.1 In-box Architecture

With the in-box solution it is assumed that Intel® 6702PXH 64-bit PCI Hub would be an embedded part of the system board and the system BIOS has complete knowledge of the PCI buses below the Intel® 6702PXH 64-bit PCI Hub, like the loading characteristics of the bus, the slot numbering scheme on the bus, etc. In such an architecture, whenever the SHPC in the Intel® 6702PXH 64-bit PCI Hub is initialized (power-on or a PCI Express bus reset) the system BIOS/firmware is invoked to initialize the SHPC working register set with board-specific information (HWInit Registers) and also initialize the PCI bus beneath Intel® 6702PXH 64-bit PCI Hub to the proper mode and frequency. Whenever the standard hot plug controller is reset, the slot interface outputs are reset to the following:

- PCIRST# is asserted.
- BUSEN# is de-asserted (disconnected from the bus).
- CLKEN# is de-asserted (PCI clock disconnected from the bus).
- PWREN is de-asserted (slot power is removed).
- All PWRLED# and ATNLED# outputs are set to OFF.

When HPA_SLOT[3] for a PCI interface is “1” (hot plug is enabled), then whenever the SHPC is initialized, the PCI bus will power up operating at 33 MHz PCI and all hot plug slots isolated from the bus. The platform BIOS/firmware could later determine the capabilities of the non-hot plug PCI cards (reading the PCI-X and 66 MHz capability bits in the PCI register space of the cards) and also the capabilities of the inserted hot plug cards, for PCI-X capability, or PCI capability at 66 MHz, and then could reset the PCI bus to operate in the new mode. The software could execute a set bus frequency/mode command to achieve the mode.

2.13.7.2 Remote-I/O-Box Architecture

This architecture is characterized by routing the hot plug interrupt to a generic interrupt pin as described in the *PCI Standard Hot-Plug Controller and Subsystem Specification,* Revision 1.0. When the OS detects the SHPC in a peer-to-peer bridge, it is required by the specification to run the OSHP ACPI control method. The code that initializes the SHPC registers can be placed in the control method. Refer to Section 5.5.1 of the *PCI Standard Hot-Plug Controller and Subsystem Specification*, Revision 1.0 for more details on the OSHP method.

2.13.8 M66EN Pin Handling

The Intel® 6702PXH 64-bit PCI Hub can drive the PAM66EN pin on each PCI bus to GND in Serial mode and in 2-Slot parallel mode. There are three possible cases where the Intel® 6702PXH 64-bit PCI Hub will drive the PAM66EN pin:

- The PFREQ and PMODE registers are reprogrammed for 33-MHz PCI mode and a secondary bus reset is completed.
- The Intel® 6702PXH 64-bit PCI Hub is powered on with any Hot Plug mode enabled by strapping the HPA_SLOT[3] pin to “1” at the rising edge of PWROK.
- A change frequency/mode command is executed by the standard hot plug controller with the frequency set at 33 MHz.

In each of these cases, the Intel® 6702PXH 64-bit PCI Hub will drive the PAM66EN pin to GND for the affected PCI bus. However, it should be noted that when the Intel® 6702PXH 64-bit PCI Hub is in 1-Slot mode and the slot is disconnected, the Intel® 6702PXH 64-bit PCI Hub will never drive the PAM66EN pin. This is to allow the hot plug controller the ability to correctly sample the M66EN pin on the PCI slot when the PCI bus is grounded (not connected) but the PCI card is powered on. In this mode, it is recommended that the M66EN pin be pulled up to the PCI slot's 3.3V power rail, which is controlled by the hot plug controller.

2.13.9 Hot Plug Interrupts

2.13.9.1 MSI and Pin Interrupts

SHPC in the Intel® 6702PXH 64-bit PCI Hub can either be enabled to generate an MSI interrupt or can generate an interrupt to the internal I/OxAPIC to be routed through it to the MCH. The SHPC interrupt is routed to interrupt input 23 of the I/OxAPIC. These two interrupts are mutually exclusive. The message for MSI comes from the message address and data registers in the Intel® 6702PXH 64-bit PCI Hub’s MSI capability registers. The message enable bit in the message control register of the capability registers either enables MSI or interrupt routing through I/OxAPIC.

2.13.9.2 ACPI Support

On platforms where the platform ACPI-compliant firmware controls the SHPC rather than having native-OS support for the SHPC, the SHPC interrupts need to be converted to an ACPI interrupt (that goes to an SCI interrupt to the processor). In the presence of native OS-support, this interrupt steering is not needed. In previous platforms where hot plug was firmware controlled, this was done by converting the hot plug interrupt into a side-band pin interrupt which was then directly routed to the GPE# pin in the ICH. In Intel® 6702PXH 64-bit PCI Hub systems, an in-band message is generated via the PCI Express interface. The interrupt steering is controlled through a

BIOS-specific bit SGME (bit 5 in CNF). This bit programs the hot plug controller to generate an SCI message to MCH instead of an MSI or a pin interrupt to the internal I/OxAPIC. This SCI message is ultimately routed by MCH to the ICH via the GPE# pin. On assertion of the GPE# pin to the ICH, the ICH pulls the SCI pin to the processor, which in turn wakes up the ACPI handler.

All logic in the SHPC function is the same as for normal MSI or pin interrupts.

2.13.10 Error Handling

The standard hot-plug controller can detect a variety of error conditions (refer to the *PCI Standard Hot-Plug Controller and Subsystem Specification*, Revision 1.0 for details) and it can be programmed to either send an error message on the PCI Express interface or raise an interrupt.

2.13.11 Assumptions and Intel® 6702PXH 64-bit PCI Hub Requirements

2.13.11.1 MRL Opening during the Sequence

While executing an enable or disable sequence, if the MRL of one of the cards is opened then the Intel® 6702PXH 64-bit PCI Hub performs the auto power down for that slot after executing the current enable/disable operation. As the maximum time required to enable is disable is 319 ms, the maximum delay between MRL open and auto-power down would be less than 320 ms.

2.13.11.2 Power Fault

The power controller/slot control logic is responsible for removing power from the slot and isolating the card in the event of a power fault. The Intel® 6702PXH 64-bit PCI Hub would notify software in the event of a power fault and wait for the slot disable command from the software to disable the appropriate slot.

2.14 Addressing

2.14.1 I/O Window Addressing

I/O accesses from the PCI Express bus always target the PCI bus. No I/O accesses are allowed from PCI to PCI Express and nor are any I/O accesses to internal devices (APIC, CSR, SHPC) allowed.

2.14.1.1 Mode I/O Access

One I/O window can be set up for forwarding I/O transactions from the PCI Express to the PCI bus. No I/O transactions can be forwarded from the PCI to the PCI Express bus. The registers and register bits listed below define the setup and control of this I/O window:

- I/O Base and Limit Address Registers
- I/O Enable bit in the Command Register
- Enable 1-Kbyte granularity in the Intel® 6702PXH 64-bit PCI Hub Configuration Register

To enable outbound I/O transactions, the I/O Enable bit (bit 0) must be set in the PD_CMD Register in the Intel® 6702PXH 64-bit PCI Hub configuration space (offset 04–05h). If the I/O Enable bit is not set, all I/O transactions initiated on the PCI Express interface will receive a master abort completion. No inbound I/O transactions may cross the bridge and are therefore master aborted.

The Intel® 6702PXH 64-bit PCI Hub implements one set of I/O Base and Limit Address Registers in configuration space that define an I/O address range for the bridge. PCI Express interface I/O transactions with addresses that fall inside the range defined by the I/O Base and Limit Address Registers are forwarded to PCI, and PCI I/O transactions with addresses that fall outside this range are master aborted.

Setting the base address to a value greater than that of the limit address turns off the I/O range. When the I/O range is turned off, no I/O transactions are forwarded to the PCI bus even if the I/O enable bit is set. The I/O range has a minimum granularity of 4 Kbytes and is aligned on a 4-Kbyte boundary. The maximum I/O range is 64 Kbytes. This range may be lowered to 1 KB granularity by setting the EN1K bit in the Intel® 6702PXH 64-bit PCI Hub Configuration Register at offset 40h.

The base register consists of an 8-bit field at configuration address 1Ch, and a 16-bit field at address 30h. The top 4 bits of the 8-bit field define bits [15:12] of the I/O base address. The bottom 4 bits are read only; returning value 0h to indicate that the Intel® 6702PXH 64-bit PCI Hub supports 16-bit I/O addressing. Bits [1:0] of the base address are assumed to be 0,which naturally aligns the base address to a 4-Kbyte boundary. The I/O base upper 16 bits register at offset 30h is Reserved. Reset initializes the value of the I/O base address to 0000h.

The I/O limit register consists of an 8-bit field at offset 1Dh and a16-bit field at offset 32h. The top 4 bits of the 8-bit field define bits [15:12] of the I/O limit address. The bottom 4 bits are read only, returning value 0h to indicate that 16-bit I/O addressing is supported. Bits [11:0] of the limit address are assumed to be FFFh, which naturally aligns the limit address to the top of a 4-Kbyte I/O address block. The 16 bits contained in the I/O limit upper 16 bits register at offset 32h are Reserved. Reset initializes the value of the I/O limit address to 0FFFh.

Note: If the EN1K bit is set in the Intel® 6702PXH 64-bit PCI Hub Configuration Register, the Base and Limit Registers are changed such that the top 6 bits of the 8-bit field define bits [15:10] of the I/O base/limit address, and the bottom 2 bits read only as 0h to indicate support for 16-bit I/O addressing. Bits [9:0] are assumed to be 0 (for the base register) and 1 (for the limit register), which naturally aligns the address to a 1-Kbyte boundary.

2.14.2 Memory Window Addressing

2.14.2.1 Mode Memory Access

2.14.2.1.15 Memory Access from the PCI to the PCI Express Bus

Two memory windows can be set up for forwarding memory transactions from the PCI Express to the PCI bus. These windows are defined as part of the standard bridge configuration space. Inverse decoding is used for forwarding transactions from PCI to PCI Express.

This section describes the memory windows that can be set up in the bridge. The register bits listed below also modify the Intel® 6702PXH 64-bit PCI Hub response to memory transactions:

- Memory-mapped I/O Base and Limit Registers
- Prefetchable Memory Base and Limit Registers
- Prefetchable Memory Base and Limit Upper 32 bits Register
- Memory Enable bit in the Command Register
- Master Enable bit in the Command register

To enable outbound memory transactions, the Memory Space Enable bit (bit 1) in the PD_CMD Register must be set (offset 04–05h). To enable inbound memory transactions, the Master Enable bit (bit 2) in the PD_CMD Register must be set (offset 04–05h). The Intel® 6702PXH 64-bit PCI Hub will not prefetch data from PCI devices. The Intel® 6702PXH 64-bit PCI Hub supports 64 bits of addressing (DAC cycles) on both interfaces.

2.14.2.1.16 Memory Base and Limit Address Registers

The Memory Base Address and Memory Limit Address Registers define an address range that the Intel® 6702PXH 64-bit PCI Hub uses to determine when to forward memory commands. The Intel® 6702PXH 64-bit PCI Hub forwards a memory transaction from the PCI Express interface to the PCI bus if the address falls within the range, and forwards it from the PCI bus to the PCI Express interface (or the peer bridge for Intel® 6702PXH 64-bit PCI Hub) if the address is outside the range (provided that they do not fall into the prefetchable memory range. This memory range supports 32-bit addressing only (addresses 4 Gbytes) and supports 1-Mbyte granularity and alignment.

This range is defined by a 16-bit base address register at offset 20h in configuration space and a 16-bit limit address register at offset 22h. The top 12 bits of each of these registers correspond to bits [31:20] of the memory address. The low 4 bits are hardwired to ground. The low 20 bits of the base address are assumed to be all 0s, which results in a natural alignment to a 1-Mbyte boundary. The low 20 bits of the limit address are assumed to be all 1s, which results in an alignment to the top of a 1-Mbyte block.

Note: Setting the base to a value greater than that of the limit turns off the memory range.

2.14.2.1.17 Prefetchable Memory Base and Limit Address Registers, Upper 32-bit Registers

The prefetchable memory base and address registers, along with their upper 32-bit counterparts, define an additional address range that the Intel® 6702PXH 64-bit PCI Hub uses to forward accesses. The Intel® 6702PXH 64-bit PCI Hub forwards a memory transaction from the PCI Express interface to PCI if the address falls within the range, and forwards transactions from PCI to the PCI Express interface (or the peer bridge) if the address is outside the range and do not fall into the regular memory range. This memory range supports 64-bit addressing, and supports 1-Mbyte granularity and alignment.

This lower 32-bits of the range are defined by a 16-bit base register at offset 24h in configuration space and a 16-bit limit register at offset 28h. The top 12 bits of each of these registers correspond to bits [31:20] of the memory address. The low 4 bits are hardwired to VCC, indicating 64-bit address support. The low 20 bits of the base address are assumed to be all 0s, which results in a natural alignment to a 1-Mbyte boundary. The low 20 bits of the limit address are assumed to be all 1s, which results in an alignment to the top of a 1-Mbyte block.

The upper 32-bits of the range are defined by a 32-bit base register at offset 28h in configuration space, and a 32-bit limit register at offset 2Ch.

Note: Setting the entire base (with upper 32-bits) to a value greater than that of the limit turns off the memory range.

2.14.2.1.18 Memory Accesses to I/OxAPIC and SHPC Memory Space

Memory accesses to I/OxAPIC memory space are handled through two address ranges and an access enable bit in I/OxAPIC configuration space, as follows:

- A 32-bit BAR (MBAR)
- An alternate 32-bit BAR (ABAR)
- Memory space enable bit (MSE) in the Command register

Refer to the chapter on I/OxAPIC for more details about these BARs. Memory accesses to SHPC memory space are handled through a 64-bit and an access enable bit:

- A 64-bit BAR (SHPC_BAR)
- Memory space enable bit (MSE) in the Command register

2.14.3 VGA Addressing

2.14.3.1 Mode Access Mechanism

When a VGA-compatible device exists behind a Intel® 6702PXH 64-bit PCI Hub bridge, the VGA Enable bit (bit 3) in the Bridge Control Register must be set (offset 3E–3Fh). If this bit is set, the Intel® 6702PXH 64-bit PCI Hub forwards all transactions addressing the VGA frame buffer memory and VGA I/O registers from the PCI Express interface to PCI, regardless of the values of the Intel® 6702PXH 64-bit PCI Hub base and limit address registers. The Intel® 6702PXH 64-bit PCI Hub will not forward VGA frame buffer memory accesses to the PCI Express interface regardless of the values of the memory address ranges. However, the I/O Enable and Memory Enable bits in the PD_CMD Register must still be set. When the bit is cleared, the Intel® 6702PXH 64-bit PCI Hub forwards transactions addressing the VGA frame buffer memory and VGA I/O

registers from PCI Express to PCI if the defined memory address ranges enable forwarding. All accesses to the VGA frame buffer memory are forwarded from the PCI bus to the PCI Express interface if the defined memory address ranges enable forwarding. However, the master enable bit must still be set. The VGA I/O addresses are never forwarded to the PCI Express interface.

The VGA frame buffer consists of the following memory address range: 000A 0000h–00B FFFFh

The VGA I/O addresses consist of the I/O addresses 3B0h–3BBh and 3C0h–3DFh. These I/O addresses are aliased every 1 Kbyte throughout the first 64 Kbytes of I/O space. This means that address bits [9:0] (3B0h–3BBh and 3C0h–3DFh) are decoded, [15:10] are not decoded and can be any value, and address bits [31:16] must be all 0s.

2.15 Transaction Ordering

2.15.1 Intel® 6702PXH 64-bit PCI Hub Transaction Ordering

The Intel® 6702PXH 64-bit PCI Hub follows the producer-consumer model of a standard PCI Express-PCI bridge. Based on this model, the Intel® 6702PXH 64-bit PCI Hub implements a set of ordering rules in the inbound and outbound directions. The ordering plane covered by these rules spans the transaction domain covered by PCI Express. The Intel® 6702PXH 64-bit PCI Hub uses a single PCI Express virtual channel to communicate with the MCH.

Accesses to the internal Intel® 6702PXH 64-bit PCI Hub configuration registers, which includes the bridge configuration registers and the CSR memory registers, follow no ordering relationship with respect to transactions moving to and from the PCI and PCI Express buses. Outbound memory/configuration transactions to the internal register space could complete out of order with respect to transactions pending in the outbound queues towards the PCI bus. Software must be aware that any semaphore mechanism implemented through the internal Intel® 6702PXH 64-bit PCI Hub register space requires a dummy read to PCI or PCI Express space to push the writes that could be pending in the Intel® 6702PXH 64-bit PCI Hub queues in either direction. The ordering tables in the next two sections do not consider these transactions.

2.15.1.1 Inbound Transaction Ordering

Table 2-28 lists the combined set of ordering rules in the inbound path of the Intel® 6702PXH 64-bit PCI Hub.

Table 2-28. Inbound Transaction Ordering

Row pass Column	Posted Write	Delayed/Split Read Request	Delayed/Split Read Completion	Delayed/Split Write Completion
Posted Write	No	Yes	No	No
Delayed/Split Read Request	No	Yes	Yes	No
Delayed/Split IO Write Request	No	Yes	Yes	No
Delayed/Split Read Completion	No	Yes	Yes	No
Delayed/Split Write Completion	No	Yes	Yes	No

2.15.1.2 Outbound Transaction Ordering

Table 2-29 lists the combined set of ordering rules in the outbound path of the Intel® 6702PXH 64-bit PCI Hub.

Table 2-29. Outbound Transaction Ordering

Row pass Column	Posted Write	Delayed (Split) Read Request	Delayed (Split) Read Completion	Delayed (Split) Write Completion
Posted Write	No	Yes	Yes	Yes
Delayed/Split Read Request	No	Yes[1]	Yes	Yes
Delayed/Split Write Request	No	Yes	Yes	Yes
Delayed/Split IO Write Completion	No	Yes	Yes	Yes
Delayed/Split Read Completion	No	Yes	Yes	Yes

NOTE: The Intel® 6702PXH 64-bit PCI Hub supports two outbound completion required requests per PCI segment. Outbound delayed/split read requests can pass each other when issued on the PCI bus.

2.16 I/OxAPIC Interrupt Controller (Functions 1)

The Intel® 6702PXH 64-bit PCI Hub contains one I/OxAPIC controller, which reside on the primary bus. The intended use of the controller on the Intel® 6702PXH 64-bit PCI Hub is to have the interrupts from PCI bus A connected to the interrupt controller on function 1.

2.16.1 Interrupt Support

The Intel® 6702PXH 64-bit PCI Hub behaves as a normal peer-to-peer bridge and can handle PCI IRQ# and PCI MSI system interrupt mechanisms.

2.16.1.1 PCI IRQ# Interrupts

The Intel® 6702PXH 64-bit PCI Hub can manage 16 pin interrupts, and has 16 pins (PAIRQ#) for these interrupts. Interrupts delivered by a pin can be either in level or edge mode, and may be either active high or active low. Since this I/OxAPIC is connected to a PCI bus, its most likely configuration will be as active low level, which will match the PCI pin polarity and functionality. Each pin is collected by the Intel® 6702PXH 64-bit PCI Hub, synchronized into the PCI clock domain, and scheduled for delivery if it is unmasked.

The Intel® 6702PXH 64-bit PCI Hub only has 16 interrupt pins per PCI segment. These pins are connected to I/OxAPIC redirection table entries 15 – 0 (of 24 entries). The standard hot plug controller is hard-wired to redirection table entry 23 of the I/OxAPIC. All other interrupts are only addressable through the PCI virtual wire mechanism. If PAIRQ[12:11]# are unused, they must be pulled up to VCC33 to ensure the boot interrupt works correctly. All other IRQ pins are terminated on-die.

2.16.1.2 PCI Message Signaled Interrupts (MSI)

These interrupts which appear on the PCI bus as inbound memory writes are decoded by the Intel® 6702PXH 64-bit PCI Hub in the PCI bridge inverse decode window and passed upstream without any modifications. BIOS would setup the PCI bridge decode register such that 0xFEEx_xxxx falls in the inverse decode window of the Intel® 6702PXH 64-bit PCI Hub.

2.16.2 PCI Express Legacy INTx Support and Boot Interrupt

The Intel® 6702PXH 64-bit PCI Hub has the capability to generate an in-band interrupt request on the PCI Express bus when the APIC is disabled. This in-band interrupt mechanism is necessary for systems that do not support the APIC and for boot. The PCI Express protocol describes an in-band legacy wire-interrupt INTx mechanism for I/O devices to signal PCI-style level interrupts. The Intel® 6702PXH 64-bit PCI Hub generates a PCI Express INTx message as follows: each interrupt pin input (16 interrupt pins) and INT[23]# is compared with its mask (bit 16 in the redirection table low, RDL register). If the interrupt is masked in the Intel® 6702PXH 64-bit PCI Hub APIC, that interrupt needs to cause an INTx message over the PCI Express bus whenever asserted. If the interrupt is not masked, then that interrupt is being used by the Intel® 6702PXH 64-bit PCI Hub APIC and should not cause an INTx message on the PCI Express bus.

In the PCI Express protocol, boot interrupts are virtualized using a pair of ASSERT and DEASSERT messages. This then gives a way to preserve the level-sensitive semantics of the PCI interrupts on the PCI Express bus. The ASSERT message will capture the asserting edge of the signal that represents the logical OR of all of the Intel® 6702PXH 64-bit PCI Hub's interrupt pins. The logical OR'ing includes both PCI sides A and B for the Intel® 6702PXH 64-bit PCI Hub. The DEASSERT message captures the deasserting edge of the signal that represents the logical OR of all of the Intel® 6702PXH 64-bit PCI Hub's interrupt pins.

Table 2-30. Intel® 6702PXH 64-bit PCI Hub INTx Routing

PCI Interrupt Pins	Internal Interrupts	PCI Express* INTx Message
0, 4, 8, 12	SHPC A (IRQ[23])	INTA
1, 5, 9, 13	SHPC B	INTB
2, 6, 10, 14	-	INTC
3, 7, 11, 15	-	INTD

2.16.3 Buffer Flushing

The Intel® 6702PXH 64-bit PCI Hub does not implement any buffer flushing features. When the Intel® 6702PXH 64-bit PCI Hub receives an interrupt on its interrupt pin, it does not flush its posted write buffers in the inbound direction in the PCI interface. This is not required from the Intel® 6702PXH 64-bit PCI Hub because PCI device drivers ultimately have to guarantee that all posted writes from the device to the memory are all flushed before executing the interrupt service routine.

2.16.4 EOI Special Cycles

The Intel® 6702PXH 64-bit PCI Hub can receive EOI special cycles over PCI Express in the IA-32 processor system bus mode. This is the result of the MCH broadcasting the IA-32 processor system bus EOI cycle. Both I/OxAPICs in the Intel® 6702PXH 64-bit PCI Hub would compare the vector

number in the EOI data field with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit for that I/O Redirection Entry in the I/OxAPIC will be cleared. The Intel® 6702PXH 64-bit PCI Hub does not forward the EOI to the PCI bus.

Note: If multiple I/O Redirection entries, for any reason, assign the same vector for more than one interrupt input, each of those entries will have the Remote_IRR bit reset to '0'.

2.16.5 Interrupt Delivery

The Intel® 6702PXH 64-bit PCI Hub I/OxAPIC can deliver interrupts to the processor through the system bus (via the PCI Express interface).

When an interrupt message needs to be sent over the PCI Express bus, i.e. when the IRR bit is set for an interrupt, the Intel® 6702PXH 64-bit PCI Hub will perform a memory write on the PCI Express bus, as seen in Table 2-31 and Table 2-32.

Table 2-31. System Bus Delivery Address Format

Bit	Description
31:20	FEEh
19:12	**Destination ID:** This will be the same as bits [63:56] of the I/O Redirection Table entry for the interrupt associated with this message.
11:4	**Enhanced Destination ID:** This will be the same as bits 55:48 of the I/O Redirection Table entry for the interrupt associated with this message.
3	**Redirection Hint:** This bit is used by the processor host bridge (system bus) to allow the interrupt message to be redirected. 0 = The message will be delivered to the agent (processor) listed in bits 19:4. 1 = The message will be delivered to an agent with a lower interrupt priority The Redirection Hint bit will be a 1 if bits 10:8 in the Delivery Mode field associated with corresponding interrupt are encoded as 001 (Lowest Priority). Otherwise, the Redirection Hint bit will be 0.
2	**Destination Mode:** This bit is used only the Redirection Hint bit is set to 1. If the Redirection Hint bit and the Destination Mode bit are both set to 1, the logical destination mode is used, and the redirection is limited only to those processors that are part of the logical group as based on the logical ID.
1:0	00

Table 2-32. System Bus Delivery Data Format (Sheet 1 of 2)

Bit	Description
31:16	0000h
15	**Trigger Mode:** 1 = Level, 0 = Edge. Same as the corresponding bit in the I/O Redirection Table for that interrupt.
14	**Delivery Status:** 1 = Assert, 0 = Deassert. If using edge-triggered interrupts, then bit will always be 1, since only the assertion is sent. If using level-triggered interrupts, then this bit indicates the state of the interrupt input.
13:12	00
11	**Destination Mode:** 1 = Logical, 0 = Physical. Same as the corresponding bit in the Redirection Table

Table 2-32. System Bus Delivery Data Format (Sheet 2 of 2)

Bit	Description
10:8	**Delivery Mode:** This is the same as the corresponding bits in the I/O Redirection Table for that interrupt.
7:0	**Vector:** This is the same as the corresponding bits in the I/O Redirection Table for that interrupt.

2.17 SMBus Interface

The SMBus address is set upon PWROK by sampling SMBUS[5] and SMBUS[3:1]. When the pins are sampled, the resulting Intel® 6702PXH 64-bit PCI Hub SMBus address is shown in Table 2-33.

Table 2-33. SMBus Address Configuration

Bit	Value
7	1
6	1
5	SMBUS[5]
4	0
3	SMBUS[3]
2	SMBUS[2]
1	SMBUS[1]

The SMBus controller has access to all internal registers in the Intel® 6702PXH 64-bit PCI Hub. It can perform reads and writes from all registers through the particular interface's configuration or memory space. I/OxAPIC memory space is accessible through its configuration space. SHPC memory space is directly accessible from the SMBus controller via the SMBus memory command.

2.17.1 SMBus Commands

The Intel® 6702PXH 64-bit PCI Hub supports six SMBus commands:

- Block Write
- Block Read
- Word Write
- Word Read
- Byte Write
- Byte Read

Sequencing these commands will initiate internal accesses to Intel® 6702PXH 64-bit PCI Hub's configuration and memory registers. For high reliability, Intel® 6702PXH 64-bit PCI Hub also supports the optional Packet Error Checking feature (CRC-8) and is enabled or disabled with each transaction.

Every configuration and memory read or write first consists of an SMBus write *sequence* which initializes the Bus Number, Device, function number, memory address offset etc. The term *sequence* is used since these variables can be initialized by the SMBus master with a single block write or multiple word or byte writes. The last write in the sequence that completes the initialization performs the internal configuration/memory read or write. The SMBus master can then initiate a read sequence which returns the status of the internal read or write command and also the data in case of a read.

Each SMBus transaction has an 8-bit command driven by the master. The command encodes information as shown in Table 2-34.

Table 2-34. SMBus Command Encoding

Bit	Description
7	**Begin:** When set, this bit indicates the first transaction of the read or write sequence.
6	**End:** When set, this bit indicates the last transaction of the read or write sequence.
5	**Memory/Configuration:** This bit indicates whether memory or configuration space is being accessed in this SMBus sequence. 1 = Memory Space 0 = Configuration Space
4	**PEC Enable:** When set, indicates PEC is enabled for the sequence. When enabled, each transaction in the sequence ends with an extra CRC byte. The Intel® 6702PXH 64-bit PCI Hub checks for CRC bytes on writes and generates CRC on reads.
3:2	**Internal Command:** 00 = Read DWord 01 = Write Byte 10 = Write Word 11 = Write DWord All accesses are naturally aligned to the access width. This field specifies the internal command to be issued by the SMBus slave logic to the Intel® 6702PXH 64-bit PCI Hub core.
1:0	**SMBus Command:** 00 = Byte 01 = Word 10 = Block 11 = Reserved This field indicates the SMBus command to be issued on the SMBus interface. It is used as an indication of the length of the transfer so that the slave knows when to expect the PEC packet (if enabled).

2.17.2 Initialization Sequence

All Configuration and memory read and writes are accomplished through SMBus write(s) and later followed by an SMBus read (for a read command). The SMBus write sequence is used to initialize the:

- Bus Number,
- Device/Function and
- 12-bit Register Number (in 2 separate bytes on SMBus)

for the configuration access. Each of the parameters above is sent on SMBus in separate bytes. The register number parameter is initialized with two bytes and Intel® 6702PXH 64-bit PCI Hub ignores the most significant 4 bits of the second byte that initializes the register number. For memory reads and writes, the write sequence initializes the:

- Destination memory
- 24-bit memory address offset (in 3 separate bytes on SMBus)

The destination memory is a byte of information that indicates the internal memory space to access in the Intel® 6702PXH 64-bit PCI Hub. The 24-bit address offset is used to address any internal memory with up to an offset of 24 bits. The Intel® 6702PXH 64-bit PCI Hub only uses 12 bits of address, and ignores the most significant 12 bits of the 24-bit address. The Intel® 6702PXH 64-bit PCI Hub slave interface always expects 24 bits of address from the SMBus master though it uses only 12 bits.

The initialization of the information can be accomplished through any combination of the supported SMBus write commands (Block, Word or Byte). The Internal Command field for each write should specify the same internal command ***every time*** (read or write). After all the information is set up, the last write (End bit is set) initiates an internal read or write command. On an internal read if the data is not available before the slave interface acknowledges this last write command (ACK), the slave will “clock stretch” until the data returns to the SMBus interface unit. On a internal write, if the write is not complete before the slave interface acknowledges this last write command (ACK), the salve will “clock stretch” until the write completes internally. If an error occurs (internal timeout, target or master abort on the internal switch) during the internal access, the last write command will receive a NACK.

2.17.3 Configuration And Memory Reads

Intel® 6702PXH 64-bit PCI Hub supports only read dword to internal register space. All Configuration and memory reads are accomplished through an SMBus write(s) and later followed by an SMBus read to read the status and the read data. For SMBus read transactions, the last byte of data (or the PEC byte if enabled) is NACK’d by the master to indicate the end of the transaction. The SMBus memory read command returns the status of the previous internal command and the data associated previous internal read command. The status field encoding is shown in Table 2-35.

Table 2-35. SMBus Status Byte Encoding

Bit	Description
7	Internal Timeout: This bit is set if an SMBus request is not completed in 2 ms internally.
6	Reserved.
5	Internal Master Abort.
4	Internal Target Abort.
3:1	Reserved
0	Successful.

Examples of configuration and memory reads are shown in Figure 2-1 to Figure 2-6. For the definition of the diagram conventions below, refer to the *SMBus Specification*, Revision 2.0.

Figure 2-1. DWord Configuration Read Protocol (SMBus Block Write/Block Read, PEC Enabled)

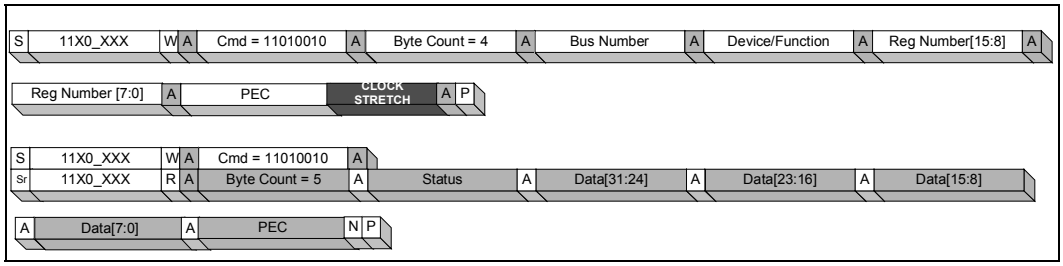


Figure 2-2. DWord Memory Read Protocol (SMBus Block Write/Block Read, PEC Enabled)

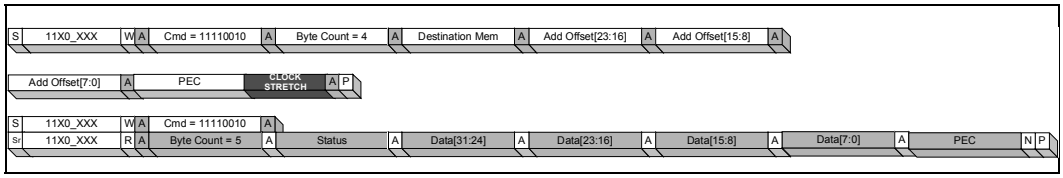


Figure 2-3. DWord Configuration Read Protocol (SMBus Word Write/Word Read, PEC Enabled)

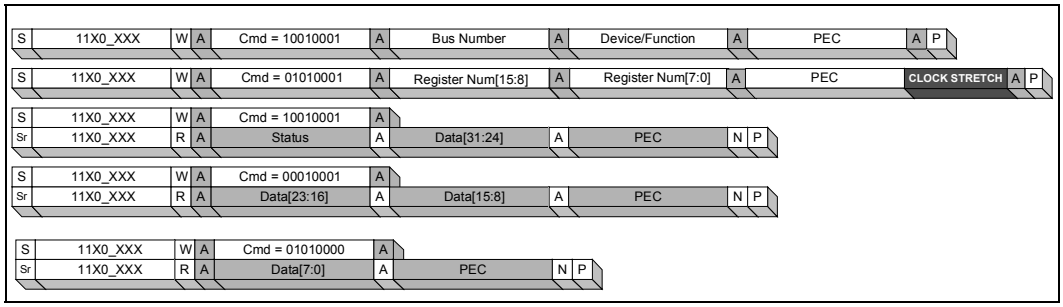


Figure 2-4. DWord Configuration Read Protocol (SMBus Block Write/Block Read, PEC Disabled)

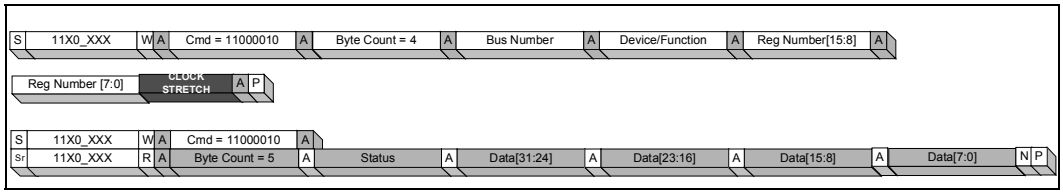


Figure 2-5. DWord Memory Read Protocol (SMBus Block Write/Block Read, PEC Disabled)

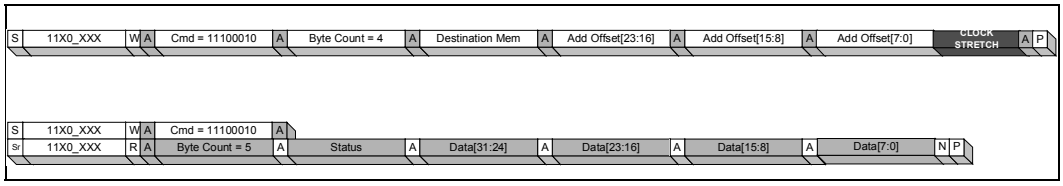
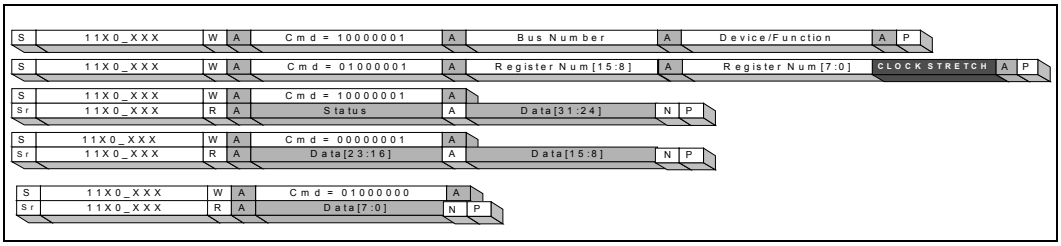


Figure 2-6. DWord Configuration Read Protocol (SMBus Word Write/Word Read, PEC Disabled)



2.17.4 Configuration and Memory Writes

Configuration and memory writes are accomplished through a series of SMBus writes. As with reads, a write sequence is first used to initialize the Bus Number, Device, Function, and Register Number for the configuration access and the destination memory, address offset for the memory write. The writing of this information can be accomplished through any combination of the supported SMBus write commands (Block, Word or Byte).

Note: On SMBus, there is no concept of byte enables. Therefore, the Register Number written to the slave is assumed to be aligned to the length of the Internal Command. In other words, for a Write Byte internal command, the Register Number specifies the byte address. For a Write DWord internal command, the two least-significant bits of the Register Number are ignored. This is different from PCI where the byte enables are used to indicate the byte of interest.

After all the information is set up, the SMBus master initiates one or more writes which sets up the data to be written. The final write (*End* bit is set) initiates an internal configuration or memory write. The slave interface could potentially clock stretch the last data write until the write completes without error. If an error occurred, the SMBus interface NACKs the last write operation just before the stop bit.

Examples of configuration writes are illustrated in Figure 2-7 to Figure 2-11. All the figures are with PEC Enabled. When PEC is disabled, there is no PEC byte in any of the sequences and the PEC enable bit in the command field is 0. For the definition of the diagram conventions below, refer to the *SMBus Specification*, Revision 2.0.

Figure 2-7. DWord Configuration Write Protocol (SMBus Block Write, PEC Enabled)

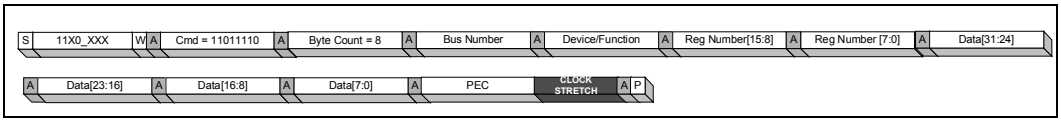


Figure 2-8. DWord Memory Write Protocol (SMBus Word Write, PEC Enabled)

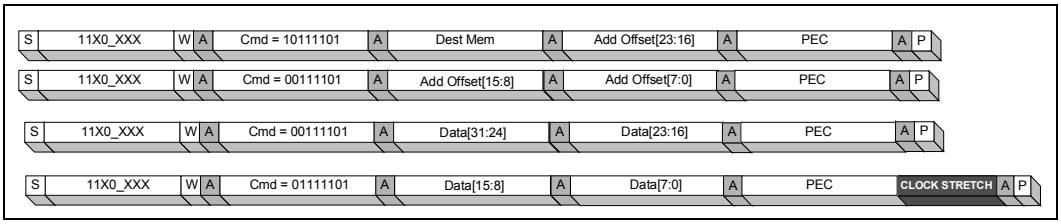


Figure 2-9. Word Configuration Write Protocol (SMBus Byte Write, PEC Enabled)

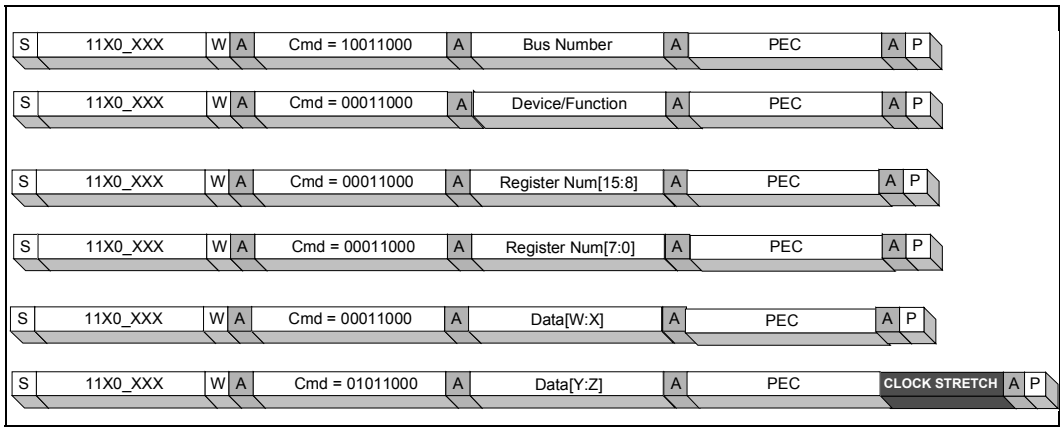


Figure 2-10. DWord Memory Read Protocol (SMBus Word Write/(Word, Byte) Read, PEC Enabled)

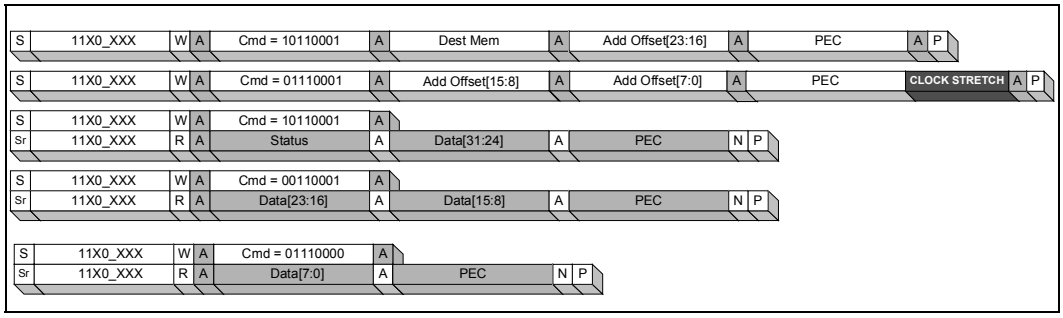
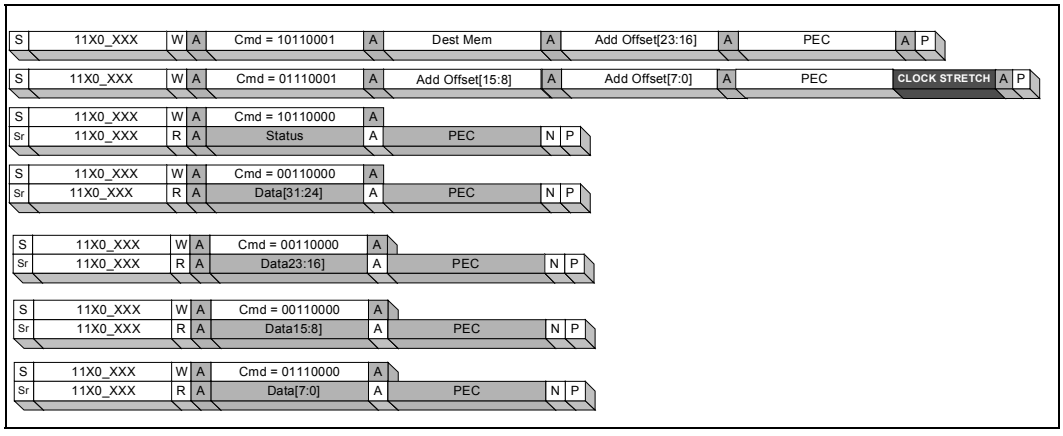


Figure 2-11. DWord Memory Read Protocol (SMBus Word Write/Byte Read, PEC Enabled)



2.17.5 Error Handling

The SMBus slave interface handles two types of errors: internal and PEC. Internal errors can occur for example when the SMBus tries to access the APIC or SHPC config/memory space and these units in Intel® 6702PXH 64-bit PCI Hub are stuck servicing a PCI Express interface which is broken. Intel® 6702PXH 64-bit PCI Hub internally times out in such a case and this error manifests itself as a Not-Acknowledge (NACK) for the read or write command (*End* bit is set). Other internal errors include the read or write command receiving a master or target abort on the internal interface. If the master receives a NACK, the entire transaction should be reattempted.

If the master supports packet error checking (PEC) and the PEC enable bit in the command is set, then the PEC byte is checked in the slave interface. If the check indicates a failure, then the slave will NACK the PEC packet and not issue the command on the internal interface.

Note: An SMBus master must either do PEC on all transactions in a sequence or not do it at all i.e. it cannot turn on PEC in the middle of a sequence.

Note: A PEC error in the middle of a sequence must be re-started from the beginning of the sequence i.e. the begin bit set.

2.17.6 SMBus Interface Reset

The master can reset the slave interface state machine in Intel® 6702PXH 64-bit PCI Hub in two ways:

- The master holds SCL low for 25 ms cumulative. Cumulative in this case means that all the “low time” for SCL is counted between the Start and Stop bit. If this totals 25 ms before reaching the Stop bit, the interface is reset.
- The master holds SCL continuously high for 50 ms.

Besides these, the SMBus interface in Intel® 6702PXH 64-bit PCI Hub is also reset on a PWROK, RSTIN# or an in-band warm reset from PCI Express.

2.17.7 Configuration Access Arbitration

If the CPU is currently accessing a unit, SM Bus cannot access it. Whoever gets in first wins arbitration. The other agent is stalled until the first agent finishes. The micro-architecture of this area is critical. The reason for the SM Bus interface is to access registers when the system may be unstable or locked, which can result with broken queues. Any register access through SM Bus must be able to proceed while the system is stuck.

2.18 System Setup

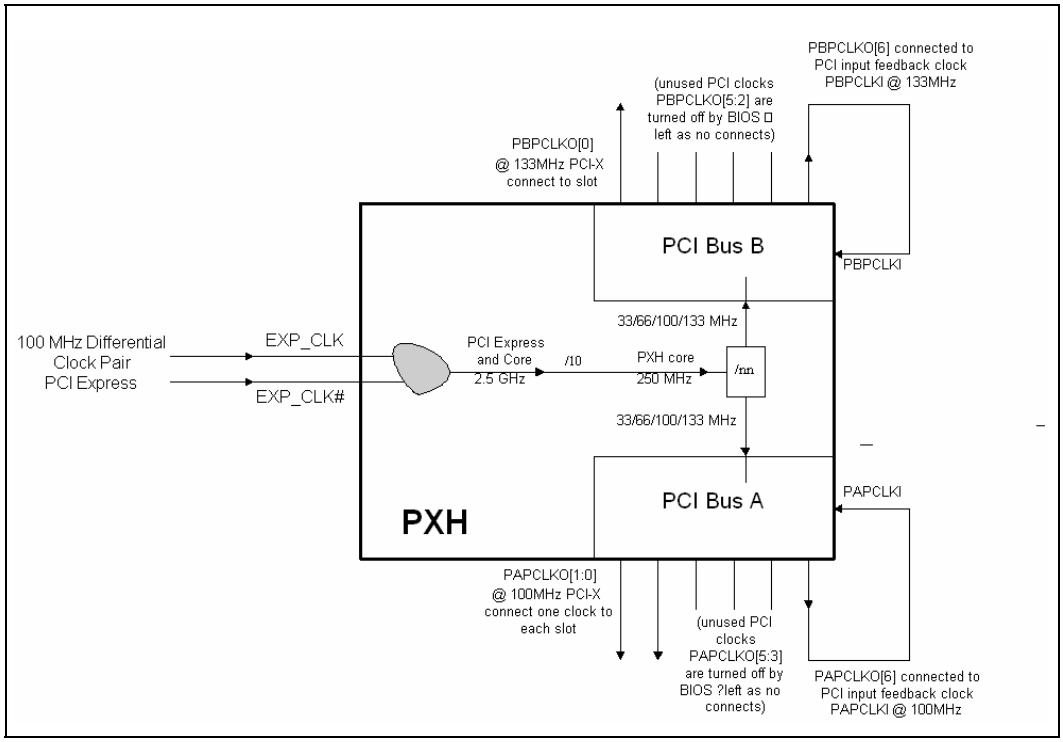
2.18.1 Clocking

In addition to 33-MHz and 66-MHz PCI output clocking, the Intel® 6702PXH 64-bit PCI Hub requires 100-MHz and 133-MHz outputs to support PCI-X. Table 2-36 shows the Intel® 6702PXH 64-bit PCI Hub clock domains.

Table 2-36. Intel® 6702PXH 64-bit PCI Hub Clocking

Clock Domain	Frequency	Source	Usage
PCI Express*	100 MHz Differential	External	PCI Express* differential clocks.
PCI	133/100/66/33 MHz	Internal	PCI Bus. These only go to the external PCI Bus.
SMBus	10-100KHz	Source Synchronous	This pin is controlled by the driver of the SMBus interface, and will run between 10 and 100 kHz.
TCK	0-16 MHz	External	JTAG clock.

Figure 2-12. Intel® 6702PXH 64-bit PCI Hub Clocking Diagram



The Intel® 6702PXH 64-bit PCI Hub component uses a 100-MHz differential pair clock inputs to generate all of its core and PCI clocks. The differential clock inputs EXP_CLK and EXP_CLK# are part of the PCI Express interface. Board design must insure that all voltages supplying the Intel® 6702PXH 64-bit PCI Hub (VCC, VCCEXP, VCC33 and VCC15) are valid before these PCI Express clocks begin running.

These clocks are fed into internal logic contained within the Intel® 6702PXH 64-bit PCI Hub to generate a 2.5 GHz clock that runs the PCI Express interface and the Intel® 6702PXH 64-bit PCI Hub core. This 2.5 GHz clock is then fed into additional internal logic that converts the clock frequency to one of the PCI/PCI-X supported frequencies (33/66/100/133 MHz for PCI or PCI-X Mode 1).

Intel® 6702PXH 64-bit PCI Hub PCI Bus segment supports 7 PCI output clocks, called PAPCLKO[6:0]. The PAPCLKO[6] output clock is connected to the PCI feedback clock input PAPCLKI.

2.18.2 Component Reset

There are five types of reset that can be performed on the Intel® 6702PXH 64-bit PCI Hub. These are listed from highest level of reset to the lowest level reset:

- **PWROK** – this signal indicates stable power when high and causes an asynchronous reset of the entire Intel® 6702PXH 64-bit PCI Hub chip when low.
- **RSTIN#** – this is also an asynchronous reset to the Intel® 6702PXH 64-bit PCI Hub and can be used for resetting the Intel® 6702PXH 64-bit PCI Hub for the front panel reset.
- **PCI Express Reset** – this is message coming on the PCI Express interface and is not a physical signal.
- **Software PCI Reset** – this reset is initiated by writing to bridge control register of the PCI configuration space. This reset is specific to the particular bridge that the software wishes to reset. This is also commonly referred to as the SBR (secondary bus reset).
- **Hot plug Reset** – This reset is caused by the act of writing to the command register with a frequency change command.

2.18.2.1 PWROK Mechanism

All the voltage sources in the system are tracked by a system component that asserts the PWROK signal only after all the voltages have been stable for some predetermined time. The Intel® 6702PXH 64-bit PCI Hub receives the PWROK signal as an asynchronous input, meaning that there is no assumed relationship between the assertion or the de-assertion of PWROK and the reference clock. While the PWROK is de-asserted the Intel® 6702PXH 64-bit PCI Hub will hold all logic in reset.

The PWROK reset will clear all internal state machines and logic, and initialize all registers to their default states including ‘sticky’ error bits that are persistent through all other reset classes. To eliminate potential system reliability problems, all devices are also required to either tristate their outputs or to drive them to safe levels during such a power on reset.

The PWROK signal is used to indicate when the power supply is within its specified voltage tolerance and is stable. It also initializes the Intel® 6702PXH 64-bit PCI Hub’s state machines and other logic once power supplies stabilize. On power up, the assertion of PWROK is delayed 100ms (T_{PVPERL}) from the power rails achieving specified operating limits. Also, within this time, the reference clocks (PCI Express clocks) become stable at least $T_{PWROK-CLK}$ (100 µS) before PWROK is asserted. Refer to the PCI Express specification for details of the relationship between PWROK assertion and the clocks and power being stable at the input of the Intel® 6702PXH 64-bit PCI Hub.

For the Intel® 6702PXH 64-bit PCI Hub in PCI-X Mode 1, PAPCIRST# is asserted for 2 ms after PWROK goes high.

2.18.2.2 RSTIN# Mechanism

Once the system is up and running, a full system reset may be required to recover from system error conditions related to various device or subsystem failures. This hot reset mechanism is provided to accomplish this recovery without clearing the 'sticky' error status bits useful to track the cause of the device or subsystem error conditions.

A hot reset can be initiated by asserting the RSTIN# signal. This signal is treated as an asynchronous input to the Intel® 6702PXH 64-bit PCI Hub, meaning that there is no assumed relationship between the assertion or the de-assertion of RSTIN# and the host reference clock.

2.18.2.3 PCI Express Reset Mechanism

There is no reset signal on the PCI Express bus, as all reset communication is in-band. The north PCI Express device (such as an MCH) communicates the fact that it is entering and coming out of a reset using messages. The Intel® 6702PXH 64-bit PCI Hub will respond by also going through a reset. This incoming message by nature of the PCI Express protocol is asynchronous to the reference clock. However, when the Intel® 6702PXH 64-bit PCI Hub goes through a reset for its own reasons (PWROK, RSTIN#) the link goes down, which will be inferred by the north device and handled with a hot plug reset (if hot plug is enabled).

2.18.2.4 Software PCI Reset (or SBR - Secondary Bus Reset)

Commonly referred to as the Secondary Bus Reset (SBR), this reset is initiated by a write to the bridge control register and resets only the particular PCI segment, thus this reset is not applicable to the Intel® 6702PXH 64-bit PCI Hub. This reset can be used for various reasons in including recovering from error conditions on the secondary bus, redoing enumeration, changing the operating frequency of the bus (33/66/100/133 MHz), changing the operating mode of the bus (PCI or PCI-X), etc. This reset is synchronous to the PCI clock domain in which it is used. SBR is strictly restricted to the particular PCI segment and affects neither the other PCI segment nor the rest of the Intel® 6702PXH 64-bit PCI Hub logic. Writes to the bridge control register with a new frequency etc., will have no effect until the SBR happens. The power up frequency of the PCI bus is shown in Table 2-37. When hot plug is enabled the bus always powers up in PCI 33 MHz mode. With hot plug disabled the frequency depends on the PAM66EN, PA133EN, PAPCIXCAP and HPA_SOC pins.

Table 2-37. Power-On Frequency of Intel® 6702PXH 64-bit PCI Hub

PCI Capability	PCI-X Capability	M66EN	133EN	PCIXCAP (on the card)
33 MHz	Not Capable	GND	X	GND
66 MHz	Not Capable	1k-10kΩ pull-up	X	GND
33 MHz	PCI-X 66 MHz	GND	X	Pull-down 10 kΩ ±5%
66 MHz	PCI-X 66 MHz	No Connect	X	Pull-down 10 kΩ ±5%
33 MHz	PCI-X 100 MHz	GND	Pull-down	0.01 µF capacitor to GND
66 MHz	PCI-X 100 MHz	No Connect	Pull-down	0.01 µF capacitor to GND
33 MHz	PCI-X 133 MHz	GND	Pull-up	0.01 µF capacitor to GND
66 MHz	PCI-X 133 MHz	No Connect	Pull-up	0.01 µF capacitor to GND

2.18.2.5 Hot Plug Reset

This reset is initiated by a write to the hot plug command register with the change frequency command. Note that a write to this register might do any of the following:

- Change the frequency (33/66/100/133 MHz).
- Change the mode (PCI or PCI-X).
- Change nothing but rewrite the present settings.

Any write (doing any of the three above) will cause a reset of the particular PCI segment to reset. This reset is asynchronous by nature to the PCI clock as the hot plug logic runs off of an internal clock that 'may' be asynchronous to the PCI clock. This reset will cause the any newly written frequency or PCI mode information to take effect. The Intel® 6702PXH 64-bit PCI Hub will support all changes in mode because of hot plug events including switching from PCI to PCI-X protocols or changing the frequency.

2.19 Reliability, Availability, and Serviceability (RAS)

The Intel® 6702PXH 64-bit PCI Hub provides the RAS features listed below to serve the needs of enterprise class servers and telecommunication blade applications.

2.19.1 PCI Express Error Handling

The PCI Express link in the Intel® 6702PXH 64-bit PCI Hub is 32-bit CRC protected providing for very high reliability. With a target bit error rate of 10^{-12} the 32-bit CRC combined with the 8b/10b encoding on the serial link, provides for greater than 10 years in MTBF (mean time between failure). The smaller link packets will utilize a 16-bit CRC scheme. PCI Express also provides for a software-transparent recovery from temporary link failures. When received packets are in error, hardware could automatically retransmit the packet. In case of permanent link failure, the link can reconfigure itself for a narrower width and for a lower performance operation. The Intel® 6702PXH 64-bit PCI Hub supports this downgraded operation from x8 to x4.

2.19.2 PCI Error Protection

PCI buses are parity protected. Upper and lower 32 bits on the PCI bus are separately parity protected.

2.19.3 PCI Standard Hot Plug Controller

The Intel® 6702PXH 64-bit PCI Hub supports the *PCI Standard Hot-Plug Controller and Subsystem Specification*, Revision 1.0, which allows PCI cards to be hot added or removed without bringing down the system.

2.19.4 SMBus

The Intel® 6702PXH 64-bit PCI Hub supports full access to the Intel® 6702PXH 64-bit PCI Hub configuration and memory space from the SMBus for system debug and management.

2.20 Error Handling

When integrity errors occur on the PCI or PCI Express buses, the Intel® 6702PXH 64-bit PCI Hub implements the specified error logging and escalation actions as per the interface rules. For example, errors encountered on the PCI interface follow the logging and escalation rules of the PCI protocol. Beyond the set of escalation and error logging mandated by the interface specifications, the Intel® 6702PXH 64-bit PCI Hub also implements some chipset-specific error logging and escalation mechanisms to aid system software/driver in a more graceful error recovery and also for system debug.

The error escalation mechanism implemented by the Intel® 6702PXH 64-bit PCI Hub can be fully masked. This provides the platform software with the ability to pick and choose what it wants to do on any of the error conditions. All Intel® 6702PXH 64-bit PCI Hub-specific logging registers are sticky, that is, these registers retain their values through any chip reset other than a power cycle reset.

2.20.1 PCI Express Errors

PCI Express errors are classified as either correctable errors or uncorrectable errors. Correctable errors are those where hardware exists to correct the errors. Uncorrectable errors are errors where hardware does not exist to correct the errors. Uncorrectable errors are further classified into fatal and non-fatal errors, with non-fatal errors indicating an unreliable link. PCI Express supports three different error messages to support these error classes – ERR_COR, ERR_UNC and ERR_FATAL. Refer to the *PCI Express Base Specification*, Revision 1.0a for details of the various PCI Express errors and how they are signaled and escalated.

PCI Express error logging specifies a set of advanced transaction logging registers as an added capability.

2.20.2 PCI Errors

PCI and PCI-X protocol errors include several sources of error, such as address and data parity errors, split completion errors, master aborts and target aborts. Some of these are fatal and some are non-fatal. The PCI-X specification specifies a set of rules on how a bridge must behave on a variety of error conditions that could happen on the bus. The Intel® 6702PXH 64-bit PCI Hub implements those rules on the PCI bus along with the Intel® 6702PXH 64-bit PCI Hub-specific error logging and routing control to aid the system software/driver in error recovery and debug

2.20.2.1 Error Types

PCI errors are classified into two categories, those that are considered fatal and those that are considered non-fatal. Fatal errors are those that have the potential to cause data corruption and hence software must be careful to contain and escalate these errors (if needed). Non-fatal errors are those errors that do not cause any data corruption, and include driver errors such as master aborts on the PCI bus and target errors such as target abort. All errors on the PCI bus are uncorrectable and will be forwarded to the PCI Express bus as such.

The non-fatal class of errors is:

- Target Aborts on the PCI bus
- Master Aborts on the PCI bus

The fatal class of errors is:

- Data parity errors on the PCI bus
- Address and attribute parity errors on the PCI bus

2.20.2.2 Error Logging

The Intel® 6702PXH 64-bit PCI Hub provides error logging which may be used for system debug and/or recovery. This logic logs the first fatal error that occurs, as well as subsequent fatal errors.

The log of the first error includes a status bit and transaction information, whereas the log of the next error carries only status information. This first/next error mechanism applies only to the fatal error class. Once the first fatal error is detected, it is logged using a status bit and a set of transaction-log registers. All subsequent errors are logged using a next-error bit, until the first error is cleared. Additionally, if a non-fatal error occurs on the PCI bus, and is followed later by a fatal error on that same PCI bus, the fatal error overrides the non-fatal error, i.e. the transaction log registers are overridden with the transaction log information for the fatal error, and the fatal error is logged. However, a non-fatal error cannot override a previous fatal error. Note also that there is a single set of transaction-log registers that are shared between the non-fatal and first-error-fatal errors.

The Intel® 6702PXH 64-bit PCI Hub can signal a message on the PCI Express bus for any of the first or next error conditions. Software (either from platform BIOS or a system management controller using SMBus) must deal with fatal errors that override non-fatal errors. The following algorithm is suggested:

- Check the non-fatal status bits in the first error register (RAS_FEPCI) to see if it is a non-fatal error.
- If one of these bits is set, set a variable to remember that this error could be overridden. Hardware will ensure that only one of these bits is set.
- Check the fatal status bits (in RAS_FEPCI) to see if it is a fatal error.
- If one of these bits is set, clear the “could be overridden” variable. This implies that between the time software read the non-fatal status bits and the fatal status bits, a fatal error occurred that overrode the non-fatal error. Hardware will ensure that only one of these bits is set.
- Read the RAS registers to determine the address and data of the error, based upon the status bits.
- If the “could be overridden” status bit is set, read the fatal error status bits again. If one of these is now set, it means between the time software started reading the RAS registers and now, a fatal error occurred, and the RAS registers cannot be trusted because they could have been overwritten. Re-read the RAS registers.
- Clear the status bit that caused the failure by writing a ‘1’.
- If the first error register is all clear (neither fatal nor non-fatal), then check the next error register (RAS_NEPCI).
- If one of the fatal or non-fatal bits is set, then clear the error by writing a 1. There is no log register that can be read for next error beyond the status bits.

RAS logging is simplified into three rules, and two terms. The terms are:

- **Context Data:** The address/data of the cycle that caused the error. For example, on a cycle that is split, the context address is the address of the cycle on the original request, not on the completion.

- **Live Data:** The value of the pins (address, data, byte enables, header) that caused the error.

The rules are:

- **Cycle Errors:** Target Abort and Master Abort are cycle errors. In these types of errors, the context data is stored along with the error indication. This is stored as opposed to live data because there is nothing fundamentally wrong with the live data – it is the context data that resulted in the error.
- **Address Parity Errors:** Live data is stored in these types of errors, because the Intel® 6702PXH 64-bit PCI Hub does not have enough information as to what the intended address was supposed to be, and the live data is needed to decode the parity error.
- **Data Parity Errors:** Live data is stored for the erroneous data, and context address is stored for the address. The live data is needed to decode the parity error, and the context address is needed in case software can recover.

The Intel® 6702PXH 64-bit PCI Hub only logs errors for cycles where it will do work. For example, if a PCI cycle had an address parity error, and the Intel® 6702PXH 64-bit PCI Hub does not assert PADEVSEL# for that cycle, then that would not be logged as an error. Also, error transaction logging on the PCI bus is decoupled from the error transaction logging on the PCI Express bus and this is possible because transaction error logging for a transaction that transits the Intel® 6702PXH 64-bit PCI Hub, happens only once at the originating interface.

2.20.2.3 Error Escalation

To support error reporting on the PCI bus, the Intel® 6702PXH 64-bit PCI Hub implements PAPERR# and PASERR# signals. Also to escalate the PCI errors on to PCI Express, the Intel® 6702PXH 64-bit PCI Hub supports the ERR_COR, ERR_UNC, ERR_FATAL messages on the PCI Express bus.

2.20.3 SHPC Errors

Refer to the *Standard Hot-Plug Controller and Subsystem Specification*, Revision 1.0 for details of SHPC error logging and reporting implemented by the Intel® 6702PXH 64-bit PCI Hub. In addition, the Intel® 6702PXH 64-bit PCI Hub provides for a way to route all SHPC interrupts to platform firmware instead of to the OS, via a vendor-specific message on the PCI Express bus.

2.20.4 Core Errors

Core errors in the Intel® 6702PXH 64-bit PCI Hub are SRAM soft errors. Data errors because of SRAM errors are forwarded with poisoned data to the appropriate end point. If the end-point is an internal device, then the data is dropped and an error message/completion (if required) signaled. If the end point is on either the PCI or PCI Express buses, the data is forwarded to the bus with the data poisoned. This allows for the PCI/PCI Express bus endpoints to determine the severity of the error and deal with it appropriately. SRAM soft errors resulting in address parity errors are far more severe. These transactions will be dropped and error message/completion generated.

Core errors will be logged with a single bit in the RAS_STS register for status. There will be a RAS_IQE register to capture individual SRAM errors from various units.

2.20.5 Global Error Register

RAS_STS register captures status of all the first and next errors signaled from the PCI Express bus, PCI bus and core SRAM errors. Signaled errors correspond to only uncorrectable errors. For both the first and next error groups, there is one bit for the PCI Express bus, one for the PC bus(es) and one for all core SRAM errors.

§

3 Register Description

The Intel® 6702PXH 64-bit PCI Hub contains registers for its PCI Express to PCI bridge(s), Standard Hot Plug Controller, I/OxAPIC controllers, and SMBus interfaces. This chapter describes these registers. A detailed bit description is also provided.

There are two functions as seen from PCI Express—one I/OxAPIC functions and one PCI bridge function. All of the functions have the same device number of 0, but with different function number.

3.1 PCI Configuration Registers

The PCI Express interface is the logical primary bus and for the Intel® 6702PXH 64-bit PCI Hub the PCI bus segment is a secondary bus with a PCI Express-to-PCI bridge corresponding to Function 0. The Standard Hot -Plug Controller (SHPC) associated with each PCI bus segment appears as a capability of the PCI Express-to-PCI Bridge. The I/OxAPIC controllers reside as separate PCI function (Function 1 for the Intel® 6702PXH 64-bit PCI Hub).

- **PCI Express-to-PCI Bridge (F0).** This portion of the Intel® 6702PXH 64-bit PCI Hub implements the buffering and control logic between the PCI and the PCI Express buses. The PCI bus arbitration is handled by these PCI devices. The PCI decoder in this device must decode the ranges for PCI Express to the MCH. This register set also provides support for Reliability, Availability, and Serviceability (RAS). Function 0 is intended for the PCI Express to PCI A Bridge.
- **I/OxAPIC Devices (F1).** There is one I/OxAPIC device on the Intel® 6702PXH 64-bit PCI Hub. They reside on the primary bus. Function 1 is intended to be used with interrupts from PCI Bus A.
- **Standard Hot Plug Controller.** The Intel® 6702PXH 64-bit PCI Hub supports a single SHPC controller. These Standard Hot Plug Controllers appear as a capability of its associated PCI Express-to-PCI Bridge.

3.2 Memory-Mapped Registers

- **I/OxAPIC.** In addition to the PCI Configuration Registers mentioned above, the I/OxAPIC memory-mapped registers are located in the processor memory space located by the MBAR Register (PCI offset 10h) and ABAR Register (PCI offset 40h). MBAR and ABAR are located in the I/OxAPIC PCI Configuration space.
- **Standard Hot Plug Controller.** In addition to the PCI Configuration Registers mentioned above, the hot plug controller memory-mapped registers are located in the processor memory space located by the MBAR Register (PCI offset 10h). MBAR is located in the hot plug controller PCI Configuration space.

3.3 SMBus Port Registers

The SMBus does not have any PCI configuration registers. SMBus fields are only accessible via the SMBus port (see Section 2.17).

3.4 Register Nomenclature and Access Attributes

Symbol	Description
RO	**Read Only.** If a register is read only, writes to this register have no effect.
ROS	**Read-Only Sticky**. Register bits are read-only and cannot be altered by software. Bits are not cleared by reset and can only be reset with the PWROK reset condition.
RW	**Read/Write.** A register with this attribute can be read and written.
RWC	**Read/Write Clear.** A register bit with this attribute can be read and written. However, a write of a 1 clears (sets to 0) the corresponding bit and a write of a 0 has no effect.
RWCS	**Read and Write One to Clear and Sticky.** through reset. Software needs to write a 1 to this bit to clear it when set. Write of 0 has no effect on this bit. Only a PWROK reset can reset this bit.
RWO	**Read/Write Once.** A register bit with this attribute can be written to only once after power up. After the first write, the bit becomes read only.
RWS	**Read-Write and Sticky.** Software can read and write from this bit and only a PWROK reset can reset this bit.
Reserved Bits	Some of the Intel® 6702PXH 64-bit PCI Hub registers described in this section contain reserved bits. These bits are labeled "Reserved". Software must deal correctly with fields that are Reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, and write operations for the configuration address register.
Reserved Registers	In addition to reserved bits within a register, the Intel® 6702PXH 64-bit PCI Hub contains address locations in the configuration space that are marked "Reserved". When a "Reserved" register location is read, a random value can be returned. ("Reserved" registers can be 8-, 16-, or 32-bit in size). Registers that are marked as "Reserved" must not be modified by system software. Writes to "Reserved" registers may cause system failure.

Symbol	Description
Default Value Upon Reset	Upon a Full Reset, the Intel® 6702PXH 64-bit PCI Hub sets its internal configuration registers to predetermined **default** states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the operating parameters and optional system features that are applicable, and to program the Intel® 6702PXH 64-bit PCI Hub registers accordingly.

3.5 PCI Express-to-PCI Bridges (D0:F0, F2)

3.5.1 Configuration Registers

The bridge configuration space follows the standard PCI-to-PCI bridge configuration space format. Table 3-1 shows the Intel® 6702PXH 64-bit PCI Hub configuration registers and their address byte offset values.

Note: Registers that are not shown should be treated as Reserved.

Table 3-1. Configuration Register Summary (Sheet 1 of 4)

Address Offset	Symbol	Register Name	Default	Access
00–01h	VID	Vendor ID Register	8086h	RO
02–03h	DID	Device ID Register	Intel® 6702PXH 64-bit PCI Hub: • 032Ch (Fn 0)	RO
04–05h	CMD	Command Register	0000h	RW, RO
06–07h	STS	Status Register	0010h	RWC, RO
08h	REVID	Revision ID Register	00h	RO
09–0Bh	CC	Class Code Register	060400h	RO
0Ch	CLS	Cache Line Size Register	00h	RW
0Dh	MLT	Master Latency Timer Register	00h	RW
0Eh	HEADTYP	Header Type Register	81h	RO
10–17h	SHPC_BAR	SHPC Base Address Register	00000008h	RW, RO
18h	PBN	Primary Bus Number Register	00h	RW
19h	SCBN	Secondary Bus Number Register	00h	RW
1Ah	SBBN	Subordinate Bus Number Register	00h	RW
1Bh	SLT	Secondary Latency Timer Register	00h (PCI) 40h (PCI-X)	RW
1Ch	IOB	I/O Base Register	00h	RW, RO
1Dh	IOL	I/O Limit Register	00h	RW, RO
1E–1Fh	SECSTS	Secondary Status Register	02A0h	RWC,RO
20–21h	MB	Memory Base Register	0000h	RW
22–23h	ML	Memory Limit Register	0000h	RW

Table 3-1. Configuration Register Summary (Sheet 2 of 4)

Address Offset	Symbol	Register Name	Default	Access
24–25h	PMB	Prefetchable Memory Base Register	0001h	RW, RO
26–27h	PML	Prefetchable Memory Limit Register	0001h	RW, RO
28–2Bh	PB_UPPER	Prefetchable Base Upper 32 Bits Register	00000000h	RW
2C–2Fh	PL_UPPER	Prefetchable Limit Upper 32 Bits Register	00000000h	RW
30–31h	IOLU16	I/O Limit Upper 16 Bits Register	0000h	RO
32–33h	IOBU16	I/O Base Upper 16 Bits Register	0000h	RO
34h	CAPP	Capabilities Pointer Register	44h	RO
3Ch	INTRL	Interrupt Line Information Register	0100h (Fn 0) 0200h (Fn 2)	RW
3Dh	INTRP	Interrupt Pin Information Register	0100h (Fn 0) 0200h (Fn 2)	RO
3E–3Fh	BRIDGE_CNT	Bridge Control Register	0000h	RW, RWC, RO
40–41h	CNF	Intel® 6702PXH 64-bit PCI Hub Configuration Register	0080h	RW, RWS, RO
42h	MTT	Multi-Transaction Timer Register	00h	RW, RO
43h	PCLKC	PCI Clock Control Register	FFh	RW, RO
44h	EXP_CAPID	PCI Express* Capability Identifier Register	01h	RO
45h	EXP_NXTP	PCI Express Next Item Pointer Register	5Ch	RO
46–47h	EXP_CAP	PCI Express Capability Register	0030h	RO
48–4Bh	EXP_DEVCAP	PCI Express Device Capabilities Register	00000001h	RO
4C–4Dh	EXP_DEVCNTL	PCI Express Link Device Control Register	0000h	RW, RO
4E–4Fh	EXP_DSTS	PCI Express Device Status Register	0000h	RWC, RO
50–53h	EXP_LCAP	PCI Express Link Capabilities Register	000B0211h	RO
54–55h	EXP_LCNTL	PCI Express Link Control Register	0000h	RW, RO
56–57h	EXP_LSTS	PCI Express Link Status Register	0000h (X1) 0040h (X4) 0080h (X8)	RO
5Ch	MSI_CAPID	PCI Express MSI Capability Identifier Register	05h	RO
5Dh	MSI_NXTP	PCI Express MSI Next Item Pointer Register	6Ch	RO
5E–5Fh	MSI_MC	PCI Express MSI Message Control Register	0080h	RW, RO
60–67h	MSI_MA	PCI Express MSI Message Address Register	00000000h	RW, RO

Table 3-1. Configuration Register Summary (Sheet 3 of 4)

Address Offset	Symbol	Register Name	Default	Access
68–69h	MSI_MD	PCI Express MSI Message Data Register	0000h	RW
6C–6Fh	EXP_CAPSTR	PCI Express Power Management Capability Structure Register	000002xxh	RO
70–73h	EXP_PMSTSCNTL	PCI Express Power Management Status and Control Register	xx000000h	RWCS, RWS, RW, RO
78h	SHPC_CAPID	SHPC Capability Identifier Register	0Ch	RO
79h	SHPC_NXTP	SHPC Next Item Pointer Register	00h	RO
7Ah	SHPC_DWSEL	SHPC DWord Select Register	00h	RO
7Bh	SHPC_STS	SHPC Status Register	00h	RO
7C–7Fh	SHPC_DWORD	SHPC Data Register	00000000h	RW
D8h	PA_CAPID	PCI-X Capability Identifier Register	07h	RO
D9h	PA_NXTP	PCI-X Next Capability Pointer Register	00h	RO
DA–DBh	PA_SSTS	PCI-X Secondary Status Register	0003h	RWC, RO
DC–DFh	PA_BSTS	PCI-X Bridge Status Register	00030000h (Function 0) 00030002h (Function 2)	RO
EC–EFh	PA_ECCFA	Bridge ECC Error First Address Register	00000000h	ROS
F0–F3h	PA_ECCSA	Bridge ECC Error Second Address Register	00000000h	ROS
F4–FBhh	PA_ECCATTR	Bridge ECC Error Attribute Register	00000000h	ROS
100–103h	ENH_CAP	PCI Express Advanced Error Capability Identifier Register	30010001h	RO
104–107h	ERRUNC_STS	PCI Express Uncorrectable Error Status Register	00000000h	RWCS, RO
108–10Bh	ERRUNC_MSK	PCI Express Uncorrectable Error Mask Register	00030010h	RWS, RO
10C–10Fh	ERRUNC_SEV	PCI Express Uncorrectable Error Severity Register	00000000h	RWCS, RO
110–113h	ERRCOR_STS	PCI Express Correctable Error Status Register	00000000h	RWCS, RO
114–117h	ERRCOR_MSK	PCI Express Correctable Error Mask Register	00000000h	RWCS, RO
118–11Bh	ADVERR_CNTL	Advanced Error Capabilities and Control Register	00000000h	ROS, RO
11C–12Bh	EXP_TXNHDLOG	PCI Express Transaction Header Log	00h (128 bits)	ROS
12C–12Fh	UNC_PAERRSTS	Uncorrectable PCI/PCI-X Error Status	0000h	RO, RWCS
130–133h	UNC_PAERRMSK	Uncorrectable PCI/PCI-X Error Mask	17A8h	RO, RWS

Table 3-1. Configuration Register Summary (Sheet 4 of 4)

Address Offset	Symbol	Register Name	Default	Access
134–137h	UNC_PAERRSEV	Uncorrectable PCI/PCI-X Error Severity	1340h	RO, RWS
138–13Bh	UNC_PAERRPTR	Uncorrectable PCI/PCI-X Error Pointer	0000h	RO, ROS
13C–14Bh	PATXN_HDLOG	Uncorrectable PCI/PCI-X Header Log	00h (128 bits)	RO, ROS
14C–153h	PA_DERRLOG	PCI/PCI-X Uncorrectable Data Error Log	00000000h	ROS
154–16Fh	PA_MISCERRLOG	Other PCI/PCI-X Error Logs and Control	0000h	RO, ROS, RWCS
170–173h	PXH_STPSTS	Intel® 6702PXH 64-bit PCI Hub Strap Status	xxxxh	RO

3.5.1.1 Offset 00h: VID—Vendor ID Register (D0:F0, F2)

Offset: 00–01h **Attribute:** RO
Default Value: 8086h **Size:** 16 bits

Bits	Type	Reset	Description
15:00	RO	8086h	**Vendor ID (VID):** 16-bit vendor ID assigned to Intel VID=8086h.

3.5.1.2 Offset 02h: DID—Device ID Register (D0:F0, F2)

Offset: 02–03h **Attribute:** RO
Default Value: 0329h or 032Ch (Function 0) **Size:** 16 bits
032Ah (Function 2)

Bits	Type	Reset	Description
15:0	RO	Intel® 6702PXH 64-bit PCI Hub Function 0 – 0329h Intel® 6702PXH 64-bit PCI Hub Function 2 – 032Ah Intel® 6702PXH 64-bit PCI Hub Function 0 – 032Ch	**Device ID (DID):** Device number of the Intel® 6702PXH 64-bit PCI Hub.

3.5.1.3 Offset 04h: PCICMD—PCI Command Register (D0:F0, F2)

Offset: 04–05h **Attribute:** RW, RO
Default Value: 0000h **Size:** 16 bits

Bits	Type	Reset	Description
15:11	RO	0	Reserved.
10	RW	0	**Interrupt Mask (INTMASK):** This bit disables the SHPC from asserting IRQ[23]# wired to the I/OxAPIC. This bit is valid only when the MSI is disabled; i.e., the MSI enable bit (bit 0) in the MSC_MC register (offset 5Eh) is a zero. A value of 0 for this bit enables the assertion of its IRQ[23]# signal to the I/OxAPIC. A value of 1 disables the assertion of its IRQ[23]# signal. If IRQ[23]# is already asserted when this bit is set, it must be de-asserted.

Bits	Type	Reset	Description
9	RO	0	**Fast Back-to-Back Transactions Enable (FBTE):** This bit has no meaning on the PCI Express* interface. It is hardwired to '0'.
8	RW	0	**SERR Enable (SEE):** Controls the enable for PCI-compatible SERR reporting on the PCI Express interface (along with the Status Register (STS REG, offset 06h, bit 14). 0 = Disable SERR reporting 1 = Enable SERR reporting Note that this bit does not affect the setting of the PCI Express error bits in the PCI Express Capability Structure.
7	RO	0	**Wait Cycle Control (WCC):** Reserved.
6	RW	0	**Parity Error Response (PER):** Controls the Intel® 6702PXH 64-bit PCI Hub response to data parity errors forwarded from the PCI Express interface and peer PCI on read completions. 0 = Disable. The Intel® 6702PXH 64-bit PCI Hub ignores these errors on the PCI Express interface and the peer PCI interface. 1 = Enable. The Intel® 6702PXH 64-bit PCI Hub reports read completion data parity errors on the PCI Express interface and sets the Master Data Parity Detected (MDPD) bit in the status register. Note that this bit does not affect the setting of the PCI Express error bits in the PCI Express Capability Structure.
5	RO	0	**VGA Palette Snoop (VGA_PS):** Reserved.
4	RO	0	**Memory Write and Invalidate (MWI):** The Intel® 6702PXH 64-bit PCI Hub does not generate memory write and invalidate transactions, as the PCI Express interface does not have a corresponding transfer type.
3	RO	0	**Special Cycle Enable (SCE):** Reserved.
2	RW	0	**Bus Master Enable (BME):** Controls the Intel® 6702PXH 64-bit PCI Hub's ability to issue memory and I/O read/write requests. 0 = Disable. The Intel® 6702PXH 64-bit PCI Hub cannot issue or I/O read/write requests respond to any memory issue memory and I/O read/write requests. 1 = Enable. The Intel® 6702PXH 64-bit PCI Hub can issue or I/O read/write requests respond to any memory issue memory and I/O read/write requests.
1	RW	0	**Memory Space Enable (MSE):** Controls the Intel® 6702PXH 64-bit PCI Hub's response as a target to memory accesses on the PCI Express interface that address a device behind the Intel® 6702PXH 64-bit PCI Hub or the SHPC memory space. 0 = These transactions are master aborted on the PCI Express interface. 1 = The Intel® 6702PXH 64-bit PCI Hub is allowed to accept cycles from PCI to be passed to the PCI Express interface.
0	RW	0	**I/O Space Enable (IOSE):** Controls the Intel® 6702PXH 64-bit PCI Hub's response as a target to I/O transactions on the PCI Express interface that addresses a device that resides behind the Intel® 6702PXH 64-bit PCI Hub. 0 = These transactions are master aborted on the PCI Express interface. 1 = Enables the Intel® 6702PXH 64-bit PCI Hub to respond to I/O transaction initiated on the PCI Express interface.

3.5.1.4 Offset 06h: STS—Status Register (D0:F0, F2)

Offset: 06–07h **Attribute:** RWC, RO
Default Value: 0010h **Size:** 16 bits

Bits	Type	Reset	Description
15	RWC	0	**Detected Parity Error (DPE):** 0 = Software clears this bit by writing a 1 to it. 1 = Intel® 6702PXH 64-bit PCI Hub detected a data parity error on the PCI Express bus interface or peer PCI segment. This bit gets set even if the Parity Error Response (bit 6 of the command register) is not set. Indicates that a parity error was detected on cycles targeting the I/OxAPIC.
14	RWC	0	**Signaled System Error (SSE):** This bit is used for PCI-compatible error signaling on the PCI Express* bus. 0 = Software clears this bit by writing a 1 to it. 1 = SERR# is reported to the PCI Express interface.
13	RWC	0	**Received Master-Abort (RMA):** 0 = Software clears this bit by writing a 1 to it. 1 = Intel® 6702PXH 64-bit PCI Hub is acting as master on the PCI Express interface and receives a completion packet with master abort status.
12	RWC	0	**Received Target-Abort (RTA):** 0 = Software clears this bit by writing a 1 to it. 1 = Intel® 6702PXH 64-bit PCI Hub is acting as master on the PCI Express interface and receives a completion packet with target abort status.
11	RWC	0	**1 = Signaled Target Abort (STA):** This bit reports the signaling of a Target-Abort termination by the Intel® 6702PXH 64-bit PCI Hub when it responds as the target of a transaction on the PCI/PCI-X interface or when the Intel® 6702PXH 64-bit PCI Hub signals a PCI-X Split Completion Message with Target Abort. 0 = Target Abort not signaled on the PCI/PCI-X interface. 1 = Target Abort signaled on the PCI/PCI-X interface. Software clears this bit by writing a 1 to it.
10:9	RO	0	**DEVSEL# Timing (DVT):** These bits have no meaning on the PCI Express interface. Hardwired to 0.
8	RWC	0	**Master Data Parity Error (MDP):** 0 = Software clears this bit by writing a 1 to it. 1 = Intel® 6702PXH 64-bit PCI Hub receives a completion packet from the PCI Express interface from a previous request, and detects a data parity error, and the Parity Error Response (PER) bit in the Command Register (offset 04h, bit 6) is set.
7	RO	0	**Fast Back-to-Back Transactions Capable (FBC):** Does not apply to PCI Express. Hardwired to 0.
6	RO	0	Reserved.
5	RO	0	**66 MHz Enable (66EN):** Does not apply to PCI Express. Hardwired to 0.
4	RO	1	**Capabilities List (CAPL):** Indicates that the Intel® 6702PXH 64-bit PCI Hub contains the capabilities pointer in the bridge. Offset 34h (Capabilities List Pointer - CAPP) indicates the offset for the first entry in the linked list of capabilities. Default = 1.

Bits	Type	Reset	Description
3	RO	0	**Interrupt Status (INTSTS):** This bit reflects the state of the SHPC interrupt, when the interrupt is generated via the IRQ[23]# wire (not via MSI). Only when the INTx mask bit in the command register is a 0 and this Interrupt Status bit is a 1, and MSI is disabled will the SHPC assert the IRQ[23]# signal to the I/OxAPIC. Setting the INTx mask bit to a 1 has no effect on the setting of this bit.
2:0	RO	0	Reserved.

3.5.1.5 Offset 08h: REVID—Revision ID Register (D0:F0, F2)

Offset: 08h **Attribute:** RO
Default Value: 09h **Size:** 8 bits

Bits	Type	Reset	Description
7:0	RO	0	**Revision ID (REVID):** This indicates the stepping of the Intel® 6702PXH 64-bit PCI Hub: 09h = C1 stepping.

3.5.1.6 Offset 09h: CC—Class Code Register (D0:F0, F2)

Offset: 09–0Bh **Attribute:** RO
Default Value: 060400h **Size:** 24 bits

This contains the class code, sub class code, and programming interface for the device.

Bits	Type	Reset	Description
23:16	RO	06h	**Base Class Code (BCC):** The value of "06h" indicates that this is a bridge device.
15:8	RO	04h	**Sub Class Code (SCC):** 8-bit value that indicates this is of type PCI-to-PCI bridge.
7:0	RO	0	**Programming Interface (PIF):** Indicates that this is standard (non-subtractive) PCI-to-PCI bridge.

3.5.1.7 Offset 0Ch: CLS—Cache Line Size Register (D0:F0, F2)

Offset: 0Ch **Attribute:** RW
Default Value: 00h **Size:** 8 bits

This indicates the cache line size of the system.

Bits	Type	Reset	Description
7:0	RW	0	**Cache Line Size (CLS):** This field is implemented by PCI Express devices as a RW field for legacy compatibility purposes but has no impact on any PCI Express* device functionality.

3.5.1.8 Offset 0Dh: MLT—Master Latency Timer Register (D0:F0, F2)

Offset: 0Dh **Attribute:** RW
Default Value: 00h **Size:** 8 bits

This register does not apply to the PCI Express interface and is maintained as RW for software compatibility.

Bits	Type	Reset	Description
7:3	RW	0	**Time Value (TV):** RW used for software compatibility only.
2:0	RO	0	Reserved.

3.5.1.9 Offset 0Eh: HEADTYP—Header Type Register (D0:F0, F2)

Offset: 0Eh **Attribute:** RO
Default Value: 81h **Size:** 8 bits

This register is used to indicate the layout for bytes 10h through 3Fh of the device's configuration space.

Bits	Type	Reset	Description
7	RO	1	**Multi-Function Device (MFD):** Reserved as '1' to indicate the bridge is a multi-function device.
6:0	RO	01h	**Header Type (HTYPE):** Defines the layout of addresses 10h through 3Fh in configuration space. Reads as 01h to indicate that the register layout conforms to the standard PCI Express-to-PCI/PCI-X bridge layout.

3.5.1.10 Offset 10h: SHPC_BAR—SHPC 64-bit Base Address Register (D0:F0, F2)

Offset: 10-17h **Attribute:** RW, RO
Default Value: 00000008h **Size:** 64 bits

This register is used to access the SHPC working register set.

Note: When hot plug is disabled (HPA_SLOT[3] = 0), this register is RESERVED and set to 0h.

Bits	Type	Reset	Description
63:12	RW	0	**Base Address (BA):** These bits are used by BIOS to understand that SHPC needs 4 Kbytes of memory space and then write a valid 4Kbyte aligned base address.
11:4	RO	0	Reserved.
3	RO	0	**Prefetchable (PF_SHPC):** This bit is a read-only 0 to indicate that this register needs to be mapped into the non-prefetchable space.
2:1	RO	10b	**Type (TYP_SHPC):** These bits are read-only with a reset default of 10b, indicating that this register can map anywhere in the 64-bit memory space.
0	RO	0	**Memory Space Indicator (MEMSI):** This bit is a read-only 0 indicating that this Base Address Register maps into memory space.

3.5.1.11 Offset 18h: PBN—Primary Bus Number Register (D0:F0, F2)

Offset: 18h
Attribute: RW
Default Value: 00h
Size: 8 bits

This register is used to record the bus number of the logical PCI bus segment to which the primary interface of the bridge is connected.

Bits	Type	Reset	Description
7:0	RW	0	**Primary Bus Number (PBN):** This field indicates the bus number of the PCI Express* interface. Configuration software programs the value in this register. Any type 1 configuration cycle with a bus number less than this number will not be accepted by this portion of the Intel® 6702PXH 64-bit PCI Hub.

3.5.1.12 Offset 19h: SCBN—Secondary Bus Number Register (D0:F0, F2)

Offset: 19h
Attribute: RW
Default Value: 00h
Size: 8 bits

This register is used to record the bus number of the PCI bus segment to which the secondary interface of the bridge is connected.

Bits	Type	Reset	Description
7:0	RW	0	**Secondary Bus Number (SCBN):** This field indicates the bus number of PCI to which the secondary interface is connected. Any type 1 configuration cycle matching this bus number will be translated to a type 0 configuration cycle and run on the PCI bus.

3.5.1.13 Offset 1Ah: SBBN—Subordinate Bus Number Register (D0:F0, F2)

Offset: 1Ah
Attribute: RW
Default Value: 00h
Size: 8 bits

This register is used to record the bus number of the highest numbered PCI bus segment which is downstream of (or subordinate to) the bridge (Intel® 6702PXH 64-bit PCI Hub).

Bits	Type	Reset	Description
7:0	RW	0	**Subordinate Bus Number (SBBN):** This field indicates the highest PCI bus number below this bridge. Any type 1 configuration cycle on the PCI Express* interface whose bus number is greater than the secondary bus number and less than or equal to the subordinate bus number will be run as a type 1 configuration cycle on the PCI bus.

3.5.1.14 Offset 1Bh: SLT—Secondary Latency Timer (D0:F0, F2)

Offset: 1Bh
Attribute: RW, RO
Default Value: 00h (PCI)
40h (PCI-X)
Size: 8 bits

This timer controls the amount of time that the Intel® 6702PXH 64-bit PCI Hub will continue to burst data on its secondary interface. The counter starts counting down from the assertion of PAFRAME#. If the grant is removed, the expiration of this counter will result in the de-assertion of PAFRAME#. If the grant has not been removed, then the Intel® 6702PXH 64-bit PCI Hub may

continue ownership of the bus. Secondary latency timer's default value should be 64 in PCI-X mode (Refer to Section 1.12.2 of the PCI-X Protocol Addendum to the PCI Local Bus Specification, Revision 2.0a, Rule 11).

Bits	Type	Reset	Description
7:3	RW	PCI – 00h PCI-X – 40h	**Secondary Latency Timer (SLT):** This 5-bit value indicates the number of PCI clocks, in 8-clock increments, that the Intel® 6702PXH 64-bit PCI Hub remains as a master of the PCI bus if another master is requesting use of the PCI bus. Bit 6 defaults to 1 on reset when in PCI-X mode.
2:0	RO	0	Reserved.

3.5.1.15 Offset 1Ch: IOB—I/O Base Register (D0:F0, F2)

Offset: 1Ch **Attribute:** RW, RO
Default Value: 00h **Size:** 8 bits

This register defines the base and limit (aligned to a 4-Kbyte boundary) of the I/O area of the bridge. Accesses from the PCI Express interface that are within the ranges specified in this register will be sent to PCI if the I/O space enable bit is set. Accesses from PCI that are outside the ranges specified will master abort.

Bits	Type	Reset	Description
7:4	RW	0	**I/O Base Address Bits [15:12] (IOBA):** This field defines the bottom address of an address range to determine when to forward I/O transactions from one interface to the other. These bits correspond to address lines 15:12 for 4 KB alignment. Bits 11:0 are assumed to be 000h.
3:2	RW RO	0	**I/O Base Address Bits [11:10] (IOBA1K):** When the EN1K bit is set in the Intel® 6702PXH 64-bit PCI Hub Configuration register (CNF), these bits become read/write and are compared with I/O address bits [11:10] to determine the 1 KB base address. When the EN1K bit is cleared, this field becomes Read Only.
1:0	RO	0	**I/O Base Addressing Capability (IOBC):** These are hardwired to '0', indicating support for only 16-bit I/O addressing.

3.5.1.16 Offset 1Dh: IOL—I/O Limit Register (D0:F0, F2)

Offset: 1Dh **Attribute:** RW, RO
Default Value: 00h **Size:** 8 bits

This register defines the limit (aligned to a 4-Kbyte boundary) of the I/O area of the bridge. Accesses from the PCI Express interface that are within the ranges specified in this register will be sent to PCI if the I/O space enable bit is set. Accesses from PCI that are outside the ranges specified will master abort.

Bits	Type	Reset	Description
7:4	RW	0	**I/O Limit Address Bits [15:12] (IOLA):** Defines the top address of an address range to determine when to forward I/O transactions from PCI Express* to PCI. These bits correspond to address lines 15:12 for 4 KB alignment. Bits [11:0] are assumed to be FFFh.

Bits	Type	Reset	Description
3:2	RW RO	0	**I/O Limit Address Bits [11:10] (IOLA1K):** When the EN1K bit is set in the Intel® 6702PXH 64-bit PCI Hub Configuration register (CNF), these bits become read/write and are compared with I/O address bits [11:10] to determine the 1 KB limit address. When the EN1K bit is cleared, this field becomes Read Only.
1:0	RO	0	**I/O Limit Addressing Capability (IOLC):** These bits are hardwired to '0', indicating support for only 16-bit I/O addressing.

3.5.1.17 Offset 1Eh: SECSTS—Secondary Status Register (D0:F0, F2)

Offset: 1E–1Fh **Attribute:** RWC, RO
Default Value: 02A0h **Size:** 16 bits

Bits	Type	Reset	Description
15	RWC	0	**Detected Parity Error (DPE):** This bit reports the detection of an uncorrectable address, attribute or data error by the Intel® 6702PXH 64-bit PCI Hub's PCI/PCI-X interface. This bit is set when any one of the following three conditions are true: • The Intel® 6702PXH 64-bit PCI Hub detects an uncorrectable address or attribute error as a potential target. • The Intel® 6702PXH 64-bit PCI Hub detects an uncorrectable data error when the target of a write transaction or a PCI-X Split Completion. • The Intel® 6702PXH 64-bit PCI Hub detects an uncorrectable data error when the master of a read transaction (immediate read data or PCI-X Split Response) This bit gets set even if the Parity Error Response Enable bit (bit 0 of offset 3E–3Fh) of the Bridge Control Register. 0 = Uncorrectable address, attribute or data error not detected on the PCI/PCI-X interface. 1 = Uncorrectable address, attribute or data error detected on the PCI/PCI-X interface. Software clears this bit by writing a 1 to it.
14	RWC	0	**Received System Error (RSE):** This bit reports the detection of a SERR# assertion on the PCI/PCI-X interface. 0 = SERR# assertion on the PCI/PCI-X interface has not been detected. 1 = SERR# assertion on the PCI/PCI-X interface has been detected. Software clears this bit by writing a 1 to it.
13	RWC	0	Received Master Abort (RMA): This bit reports the detection of a Master-Abort termination when the Intel® 6702PXH 64-bit PCI Hub is acting as a PCI/PCI-X master or when the Intel® 6702PXH 64-bit PCI Hub receives a PCI-X Split Completion Message indicating Master Abort. 0 = Master-Abort not detected on the PCI/PCI-X interface. 1 = Master-Abort detected on the PCI/PCI-X interface Software clears this bit by writing a 1 to it.

Bits	Type	Reset	Description
12	RWC	0	Received Target Abort (RTA): This bit reports the detection of a Target-Abort termination when the Intel® 6702PXH 64-bit PCI Hub is acting as a PCI/PCI-X master or when the Intel® 6702PXH 64-bit PCI Hub signals a PCI-X Split Completion Message indicating Target Abort. 0 = Target-Abort not detected on the PCI/PCI-X interface. 1 = Target-Abort detected on the PCI/PCI-X interface Software clears this bit by writing a 1 to it.
11	RWC	0	Signaled Target Abort (STA): This bit reports the signaling of a Target-Abort termination by the Intel® 6702PXH 64-bit PCI Hub when it responds as the target of a transaction on the PCI/PCI-X interface or when the Intel® 6702PXH 64-bit PCI Hub signals a PCI-X Split Completion Message with Target Abort. 0 = Target-Abort not signaled on the PCI/PCI-X interface. 1 = Target-Abort signaled on the PCI/PCI-X interface. Software clears this bit by writing a 1 to it.
10:9	RO	01b	**DEVSEL# Timing (DVT):** This field indicates that the Intel® 6702PXH 64-bit PCI Hub responds in medium decode time to all cycles targeting the PCI Express* interface.
8	RWC	0	**Master Data Parity Error (MDP):** This bit is used to report the detection of an uncorrectable data error. This Bit is set if the Intel® 6702PXH 64-bit PCI Hub is the bus master of the transaction on the PCI/PCI-X interface, the Parity Error Response bit in the Bridge Control register is set, and either of the following two conditions occur: • The Intel® 6702PXH 64-bit PCI Hub asserts PERR# on a read transaction • The Intel® 6702PXH 64-bit PCI Hub detects PERR# asserted on a write transaction In addition, when in PCI-X mode, this bit is set if either of the following occur: • The Intel® 6702PXH 64-bit PCI Hub detects an uncorrectable data error in a Split Completion or Split Completion Message. • The Intel® 6702PXH 64-bit PCI Hub receives a Split Completion Message for a non-posted write indicating an Uncorrectable (Split) Write Data Error. 0 = No uncorrectable data error detected on the PCI/PCI-X interface. 1 = Uncorrectable data error detected on the PCI/PCI-X interface. Once set, this bit remains set until it is reset by writing a 1 to this bit location. If the Parity Error Response bit is cleared, this bit is never set.
7	RO	1	**Fast Back-to-Back Transactions Capable (FBTC):** Indicates that the secondary interface of the Intel® 6702PXH 64-bit PCI Hub can receive fast back-to-back cycles.
6	RO	0	Reserved.
5	RO	1	**66 MHz Capable (C66):** Indicates the secondary interface of the bridge is 66 MHz capable.
4:0	RO	0	Reserved.

3.5.1.18 Offset 20h: MB—Memory Base Register (D0:F0, F2)

Offset: 20–21h **Attribute:** RW, RO
Default Value: 0000h **Size:** 16 bits

This register defines the base (aligned to a 1-Mbyte boundary) of the prefetchable memory area of the bridge. Accesses from the PCI Express interface that are within the range specified in this register will be sent to PCI if the memory space enable bit is set.

Accesses from PCI that are outside the range specified will be forwarded to the PCI Express interface if the bus master enable bit is set.

Bits	Type	Reset	Description
15:4	RW	0	**Memory Base (MB):** These bits are compared with bits [31:20] of the incoming address to determine the lower 1 MB aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value.
3:0	RO	0	Reserved.

3.5.1.19 Offset 22h: ML—Memory Limit Register (D0:F0, F2)

Offset: 22–23h **Attribute:** RW, RO
Default Value: 0000h **Size:** 16 bits

This register defines the limit (aligned to a 1MByte boundary) of the prefetchable memory area of the bridge. Accesses from the PCI Express interface that are within the range specified in this register will be sent to PCI if the memory space enable bit is set.

Accesses from PCI that are outside the range specified will be forwarded to the PCI Express interface if the bus master enable bit is set.

Bits	Type	Reset	Description
15:4	RW	0	**Memory Limit (ML):** These bits are compared with bits [31:20] of the incoming address to determine the upper 1MByte aligned value (exclusive) of the range. The incoming address must be less than this value.
3:0	RO	0	Reserved.

3.5.1.20 Offset 24h: PMB—Prefetchable Memory Base Register (D0:F0, F2)

Offset: 24–25h **Attribute:** RW, RO
Default Value: 0001h **Size:** 16 bits

Defines the base (aligned to a 1MByte boundary) of the prefetchable memory area of the bridge. Accesses from the PCI Express interface that are within the ranges specified in this register will be sent to PCI if the memory space enable bit is set.

Accesses from PCI that are outside the ranges specified will be forwarded to the PCI Express interface if the bus master enable bit is set.

Note that even though this register specifies a valid prefetchable memory window, the Intel® 6702PXH 64-bit PCI Hub never prefetches through this window in the outbound direction (reads from PCI Express to PCI). In the inbound direction, prefetchability through this window is controlled through the Intel® 6702PXH 64-bit PCI Hub configuration register bits 4:3, at offset 40h.

Bits	Type	Reset	Description
15:4	RW	0	**Prefetchable Memory Base (PMB):** These bits are compared with bits [31:20] of the incoming address to determine the lower 1 MB aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value.
3:0	RO	1	**64-bit Indicator (IS64B):** Indicates that 64-bit addressing is supported for the limit. This value must be in agreement with the IS64L field.

3.5.1.21 Offset 26h: PML—Prefetchable Memory Limit Register (D0:F0, F2)

Offset: 26–27h **Attribute:** RW, RO
Default Value: 0001h **Size:** 16 bits

Defines the limit (aligned to a 1MByte boundary) of the prefetchable memory area of the bridge. Accesses from the PCI Express interface that are within the ranges specified in this register will be sent to PCI if the memory space enable bit is set.

Accesses from PCI that are outside the ranges specified will be forwarded to the PCI Express interface if the bus master enable bit is set.

Note that even though this register specifies a valid prefetchable memory window, the Intel® 6702PXH 64-bit PCI Hub never prefetches through this window in the outbound direction (reads from PCI Express to PCI). In the inbound direction, prefetchability through this window is controlled through the Intel® 6702PXH 64-bit PCI Hub configuration register bits 4:3, at offset 40h.

Bits	Type	Reset	Description
15:4	RW	0	**Prefetchable Memory Limit (PML):** These bits are compared with bits [31:20] of the incoming address to determine the upper 1MByte aligned value (exclusive) of the range. The incoming address must be less than this value.
3:0	RO	1	**64-bit Indicator (IS64L):** Indicates that 64-bit addressing is supported for the limit. This value must be in agreement with the IS64B field.

3.5.1.22 Offset 28h: PMB_UPPER—Prefetchable Base Upper 32 Bits Register (D0:F0, F2)

Offset: 28–2Bh **Attribute:** RW, RO
Default Value: 00000000h **Size:** 32 bits

This defines the upper 32 bits of the prefetchable address base register.

Bits	Type	Reset	Description
31:0	RW	0	**Prefetchable Memory Base Upper Portion (PMBU):** All bits are read/writeable; the Intel® 6702PXH 64-bit PCI Hub supports full 64-bit addressing.

3.5.1.23 Offset 2Ch: PML_UPPER—Prefetchable Limit Upper 32 Bits Register (D0:F0, F2)

Offset: 2C–2Fh **Attribute:** RW
Default Value: 00000000h **Size:** 32 bits

This defines the upper 32 bits of the prefetchable address limit register.

Bits	Type	Reset	Description
31:0	RW	0	**Prefetchable Memory Limit Upper Portion (PMLU):** All bits are read/writeable; the Intel® 6702PXH 64-bit PCI Hub supports full 64-bit addressing.

3.5.1.24 Offset 30h: IOLU16—I/O Limit Upper 16 Bits Register (D0:F0, F2)

Offset: 30–31h **Attribute:** RO
Default Value: 0000h **Size:** 16 bits

Since I/O is limited to 64 Kbytes, this register is reserved and not used.

Bits	Type	Reset	Description
15:0	RO	0	**I/O Limit High 16 Bits (IOLH):** Reserved.

3.5.1.25 Offset 32h: IOBU16—I/O Base Upper 16 Bits Register (D0:F0, F2)

Offset: 32–33h **Attribute:** RO
Default Value: 0000h **Size:** 16 bits

Since I/O is limited to 64 Kbytes, this register is reserved and not used.

Bits	Type	Reset	Description
15:0	RO	0	**I/O Base High 16 Bits (IOBH):** Reserved.

3.5.1.26 Offset 34h: CAPP—Capabilities Pointer Register (D0:F0, F2)

Offset: 34h **Attribute:** RO
Default Value: 44h **Size:** 8 bits

This register is used to point to a linked list of additional capabilities implemented by the Intel® 6702PXH 64-bit PCI Hub.

Bits	Type	Reset	Description
7:0	RO	44h	**Capabilities Pointer (PTR):** This field indicates that the pointer for the first entry in the PCI Express* Capability List is at offset 44h in configuration space.

3.5.1.27 Offset 3Ch: INTRL—Interrupt Line Register (D0:F0, F2)

Offset: 3Ch **Attribute:** RW
Default Value: 00h **Size:** 8 bits

This register communicates interrupt line routing information.

Bits	Type	Reset	Description
7:0	RW	0	**Interrupt Line (INTRL):** This register is used to convey the interrupt line routing information between the initialization code and the device driver. This is not used by the Intel® 6702PXH 64-bit PCI Hub.

3.5.1.28 Offset 3Dh: INTRP—Interrupt Pin Register (D0:F0, F2)

Offset: 3Dh **Attribute:** RW
Default Value: 01h (Function 0) **Size:** 8 bits
02h (Function 2)

This register is used to indicate which interrupt virtual wires, if any, the Intel® 6702PXH 64-bit PCI Hub uses on behalf of internal sources.

Bits	Type	Reset	Description
7:0	RO	Function 0: 01h Function 2: 02h	**Interrupt Pin (INTR):** The Intel® 6702PXH 64-bit PCI Hub has an integrated standard hot plug controller, which is a source of interrupts. The logical primary bus interrupt pin is INTA# for Function 0, with a corresponding register value of 01h. The interrupt pin is INTB# for Function 2, with a corresponding register value of 02h. Note that the hot plug interrupt is routed internally to IRQ#[23] of the corresponding I/OxAPIC.

3.5.1.29 Offset 3Eh: BRIDGE_CNT—Bridge Control Register (D0:F0, F2)

Offset: 3E–3Fh **Attribute:** RW, RWC; RO
Default Value: 0000h **Size:** 16 bits

This register provides extensions to the Command register that are specific to a bridge. The Bridge Control register provides many of the same controls for the secondary interface that are provided by the Command register for the primary interface. Some bits affect operation of both interfaces of the bridge.

Bits	Type	Reset	Description
15:12	RO	0	Reserved.
11	RW	0	**Discard Timer SERR Enable (DTSE):** Controls the generation of ERR_UNC on the primary interface in response to a timer discard on the secondary interface. 0 = Do not generate ERR_UNC on a secondary timer discard 1 = Generate ERR_UNC in response to a secondary timer discard
10	RWC	0	**Discard Timer Status (DTS):** Software clears this bit by writing a 1 to it. 1 = Secondary discard timer expires (there is no discard timer for the primary interface)

Bits	Type	Reset	Description
9	RW	0	**Secondary Discard Timer (SDT):** Sets the maximum number of PCI clock cycles that the Intel® 6702PXH 64-bit PCI Hub waits for an initiator on the PCI bus to repeat a delayed transaction request. The counter starts once the delayed transaction completion is at the head of the queue. If the master has not repeated the transaction at least once before the counter expires, the Intel® 6702PXH 64-bit PCI Hub discards the transaction from its queues. 0 = The PCI master timeout value is between 2^{15} and 2^{16} PCI clocks. 1 = The PCI master timeout value is between 2^{10} and 2^{11} PCI clocks.
8	RW	0	**Primary Discard Timer (PDT):** Not relevant to the PCI Express* interface. This bit is RW for software compatibility only.
7	RO	0	**Fast Back-to-Back Enable (FBE):** The Intel® 6702PXH 64-bit PCI Hub cannot generate fast back-to-back cycles on the PCI bus from PCI Express interface initiated transactions.
6	RW	0	**Secondary** Bus Reset (SBR): Controls PAPCIRST# assertion on the PCI bus. 0 = Intel® 6702PXH 64-bit PCI Hub deasserts PAPCIRST#. 1 = Intel® 6702PXH 64-bit PCI Hub asserts PAPCIRST#. When PAPCIRST# is asserted, the data buffers between the PCI Express interface and PCI and the PCI bus interface logic are initialized back to reset conditions. The PCI Express interface logic and the Intel® 6702PXH 64-bit PCI Hub configuration registers are not affected. SHPC interface logic, SHPC working space registers, I/OxAPIC interface logic and I/OxAPIC registers are not reset on this bit being set. Note that once this bit is set, the Intel® 6702PXH 64-bit PCI Hub will complete the currently running transaction on the PCI bus and then reset the bus. It is the responsibility of software to make sure that all pending transactions with the bus segment are complete before setting this bit.
5	RW	0	**Master Abort Mode (MAM):** Controls the Intel® 6702PXH 64-bit PCI Hub's behavior when a master abort occurs on either interface. **Master Abort on the PCI Express interface (Memory reads only):** 0 = The Intel® 6702PXH 64-bit PCI Hub asserts PATRDY# on the PCI/PCI-X bus. It drives all '1's for reads. 1 = The Intel® 6702PXH 64-bit PCI Hub returns a target abort on the PCI/PCI-X bus. **Master Abort PCI (Completion required packets only):** 0 = Normal completion status will be returned on the PCI Express interface. 1 = Target abort completion status will be returned on the PCI Express interface.
4	RW	0	**VGA 16-bit Decode (V16D):** This bit enables the bridge to provide 16-bit decoding of the VGA I/O address precluding the decode of VGA alias addresses every 1 KB. This bit requires the VGA enable bit (bit 3 of this register) to be set to 1. 0 = Disable 1 = Enable

Bits	Type	Reset	Description
3	RW	0	**VGA Enable (VGAE):** Modifies the Intel® 6702PXH 64-bit PCI Hub's response to VGA compatible address. 1 = Intel® 6702PXH 64-bit PCI Hub forwards the following transactions from the PCI Express* interface to PCI regardless of the value of the I/O base and I/O limit registers. The transactions are qualified by the memory enable and I/O enable in the command register. Memory addresses: 000A0000h–000BFFFFh I/O addresses: 3B0h–3BBh and 3C0h-3DFh. For the I/O addresses, bits [63:16] of the address must be '0', and bits [15:10] of the address are ignored (i.e., aliased). 0 = The same holds true from secondary accesses to the primary interface in reverse. That is, when the bit is 0, memory and I/O addresses on the secondary interface between the above ranges will be forwarded to the PCI Express interface.
2	RW	0	**ISA Enable (IE):** Modifies the response by the bridge to ISA I/O addresses. This only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of PCI I/O space. 0 = Disable. 1 = Enable. The bridge will block any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1 KB block (offsets 100h to 3FFh). This bit has no effect on transfers originating on the secondary bus as the Intel® 6702PXH 64-bit PCI Hub does not forward I/O transactions across the bridge.
1	RW	0	**SERR Enable (SE):** Controls the forwarding of secondary interface SERR# assertions on the primary interface. 0 = Disable. 1 = Enable. The Intel® 6702PXH 64-bit PCI Hub will send a PCI Express interface SERR cycle when all of the following are true: SERR# is asserted on the secondary interface This bit is set The SERR Enable bit in the Command Register is set
0	RW	0	**Parity Error Response Enable (PERE):** Controls the Intel® 6702PXH 64-bit PCI Hub's response to address and data parity errors on the secondary interface. 0 = The bridge must ignore any parity errors that it detects and continue normal operation. The Intel® 6702PXH 64-bit PCI Hub must generate parity even if parity error reporting is disabled. 1 = Intel® 6702PXH 64-bit PCI Hub will report parity errors.

3.5.1.30 Offset 40h: CNF—Intel® 6702PXH 64-bit PCI Hub Configuration Register (D0:F0, F2)

Offset: 40–41h **Attribute:** RW, RWS, RO
Default Value: 0080h **Size:** 16 bits

This register contains Intel® 6702PXH 64-bit PCI Hub specific control bits.

Bits	Type	Reset	Description
15:14	RW	x	**PCI Mode (PMODE):** Determines the mode of operation of the PCI bus. These bits both reflect the status of the current PCI bus mode at power up and also lets software change the mode by writing to these bits. **Bits Mode** **00 Conventional PCI Mode** **01 PCI-X Mode 1** **10 Reserved** **11 Reserved** **Note: These bits are provided for debug purposes only. When hot plug is enabled, software must use the Standard Hot Plug commands to change the PCI bus mode and frequency. Modifying these bits while hot plug is enabled may incur undesirable results.** **When hot plug is disabled, the Intel® 6702PXH 64-bit PCI Hub checks the software-requested frequency and mode to be consistent with the slot's and bug segment's capabilities. If the requested frequency/mode is greater than the capabilities of the slot/bus segment, then the Intel® 6702PXH 64-bit PCI Hub aliases the command to 33 MHz PCI.**
13	RWS	1	**I/OxAPIC Config Space Disable (ICSD):** 0 = I/OxAPIC configuration space is enabled. 1 = Intel® 6702PXH 64-bit PCI Hub disables all configuration accesses to I/OxAPIC configuration space from PCI Express*. All configuration accesses from PCI Express to I/OxAPIC are master aborted. This bit has no affect on the SMBus or memory accesses to I/OxAPIC configuration space.
12	RW	0	**Enable I/O Space to 1 KB Granularity (EN1K):** 0 = Disable. 1 = Enable. I/O space is decoded to 1 KB instead of the 4 KB limit that currently exists in the I/O base and I/O limit registers. It does this by redefining bits [11:10] and bits [3:2] of the IOB and IOL registers at offset 1Ch and 1Dh to be read/write, and enables them to be compared with I/O address bits [11:10] to determine if they are within the bridge's I/O range.
11	RO	0	Reserved.
10:9	RW	0	**PCI Frequency (PFREQ):** Determines the frequency at which the PCI bus operates. After software determines the bus' capabilities, it sets this value and the PMODE (bits 14 and 15 of this register) to the desired frequency and resets the PCI bus. The values are encoded as follows: 00 = 33 MHz 01 = 66 MHz 10 = 100 MHz 11 = 133 MHz Invalid combinations should not be written by software. Results will be indeterminate.
8	RO	0	Reserved.

Bits	Type	Reset	Description
7	RW	0	**Peer Memory Read Enable (PMRE):** 0 = Normal operation. Peer memory reads are not allowed and all memory reads from the PCI bridge will be sent to PCI Express regardless of the address. 1 = Normal + Peer-to-Peer mode of operation. Intel® 6702PXH 64-bit PCI Hub supports full Peer-to-Peer read/write but it's not performance optimized.
6	RO	0	Reserved.
5	RW	0	**SHPC GPE Message Enable (SGME):** Enable Redirection of hot plug interrupts to Assert/Deassert_GPE Messages on the PCI Express bus.
4:0	RO	0	Reserved.

3.5.1.31 Offset 42h: MTT—Multi-Transaction Timer Register (D0:F0, F2)

Offset: 42h **Attribute:** RW, RO
Default Value: 00h **Size:** 8 bits

This register controls the amount of time that the Intel® 6702PXH 64-bit PCI Hub's arbiter allows a PCI initiator to perform multiple back-to-back transactions on the PCI bus. The number of clocks programmed in the Multi-Transition Timer represents the guaranteed time slice (measured in PCI clocks) allotted to the current agent, after which the arbiter will grant another agent that is requesting the bus.

Bits	Type	Reset	Description
7:3	RW	0	**Timer Count Value (MTC):** This field specifies the amount of time that grant remains asserted to a master continuously asserting its request for multiple transfers. This field specifies the count in an 8-clock (PCI clock) granularity.
2:0	RO	0	Reserved.

3.5.1.32 Offset 43h: PCLKC—PCI Clock Control Register (D0:F0, F2)

Offset: 43h **Attribute:** RW, RO
Default Value: FFh **Size:** 8 bits

This register controls the enable or disable of the Intel® 6702PXH 64-bit PCI Hub PCI clock outputs PAPCLKO[6:0].

Bits	Type	Reset	Description
7	RO	1	Reserved.
6:0	RW	1111111b	**PCI Clock Control (PCLKC):** These bits enable the PCI clock output buffers, when 1. Otherwise the buffers are tri-stated. Bit 6 corresponds to PAPCLKO[6], bit 5 corresponds to PAPCLKO[5], etc.

3.5.1.33 Offset 44h: EXP_CAPID—PCI Express Capability Identifier Register (D0:F0, F2)

Offset: 44h **Attribute:** RO
Default Value: 10h **Size:** 8 bits

Bits	Type	Reset	Description
7:0	RO	10h	**PCI Express* Capability Identifier (PCIECAPI):** Indicates PCI Express capability.

3.5.1.34 Offset 45h: EXP_NXTP—PCI Express Next Pointer Register (D0:F0, F2)

Offset: 45h **Attribute:** RO
Default Value: 5Ch **Size:** 8 bits

Bits	Type	Reset	Description
7:0	RO	5Ch	**Next Pointer (MNPTR):** Points to the next capabilities list pointer, which is the MSI capability.

3.5.1.35 Offset 46h: EXP_CAP—PCI Express Capability Register (D0:F0, F2)

Offset: 46 - 47h **Attribute:** RO
Default Value: 0030h **Size:** 16 bits

Bits	Type	Reset	Description
15:8	RO	0	Reserved.
7:4	RO	7h	**Device/Port Type(DEVPORT):** Indicates the type of PCI Express* logical device. Value of 7h indicates that this is a PCI/PCI-X to PCI Express* Bridge.
3:0	RO	1h	**Capability Version (CAPVER):** Indicates PCI-SIG defined PCI Express capability structure version number. Must be 1h for this version.

3.5.1.36 Offset 48h: EXP_DEVCAP—PCI Express Device Capabilities Register (D0:F0, F2)

Offset: 48 – 4Bh **Attribute:** RO
Default Value: 00000001h **Size:** 32 bits

This register contains information about the PCI Express link capabilities.

Bits	Type	Reset	Description
31:12	RO	0	Reserved.
11:9	RO	0	**Endpoint L1 Acceptable Latency (L1AL):** The Intel® 6702PXH 64-bit PCI Hub does not support L1 Link State Power Management (LSPM).
8:6	RO	0	**Endpoint L0s Acceptable Latency (L0AL):** The Intel® 6702PXH 64-bit PCI Hub wants the least possible latency out of L0s.

Bits	Type	Reset	Description
5	RO	0	**Extended Tag Field Supported (ETFS):** This field indicates the maximum supported size of the Tag Field. Defined encodings are: 0 = 5-bit Tag field supported 1 = 8-bit Tag field supported The Intel® 6702PXH 64-bit PCI Hub only supports a 5-bit tag.
4:3	RO	0	Reserved.
2:0	RO	1	**Supported Maximum Payload Size (SMPS):** The Intel® 6702PXH 64-bit PCI Hub supports a max payload size of 256 byte packets.

3.5.1.37 Offset 4Ch: EXP_DEVCNTL—PCI Express Device Control Register (D0:F0, F2)

Offset: 4C – 4Dh **Attribute:** RW, RO
Default Value: 0000h **Size:** 16 bits

This register contains command bits that control the Intel® 6702PXH 64-bit PCI Hub behavior on the PCI Express bus.

Bits	Type	Reset	Description
15	RW	0	**Bridge Configuration Retry Enable (BCRE):** When set, the Intel® 6702PXH 64-bit PCI Hub is enabled to return a configuration retry response on the PCI Express* bus for a configuration transaction to PCI/PCI-X.
14:12	RW	2h	**Max_Read_Request Size (MRRS):** Applies to the bridge segment when the segment is in the PCI mode only. When in PCI-X mode, this does not apply (branch predict). The Intel® 6702PXH 64-bit PCI Hub cannot send requests greater than the size indicated by this field. Encodings are: Value Request Size 000b 128 bytes 001b 256 bytes 010b 512 bytes 011b 1024 bytes 100b 2048 bytes 101b 4096 bytes 110b Alias 101b 111b Alias 101b
11	RO	0	**Enable No Snoop (ENS):** This does not apply to the Intel® 6702PXH 64-bit PCI Hub since it does not set the No Snoop bit on MSI transactions it generates.
10	RO	0	**Auxiliary (AUX) Power PM Enable (AUXPWRPM_EN):** The Intel® 6702PXH 64-bit PCI Hub ignores this since it does not support Aux Power.
9	RO	0	**Phantom Function Enable (PFE):** The Intel® 6702PXH 64-bit PCI Hub ignores this since it does not support Phantom functions.
8	RO	0	**Extended Tag Field Enable (ETFE):** Always a 0 since the Intel® 6702PXH 64-bit PCI Hub only supports a 5-bit tag.
7:5	RW	0	**Maximum Payload Size (MPS):** For Intel® 6702PXH 64-bit PCI Hub this must be programmed to either 000 (128B) or 001(256B). Any other value will default to a behavior of 128B.
4	RW	0	Reserved.

Bits	Type	Reset	Description
3	RO	0	**Unsupported Request Reporting Enable (URRE):** Enables reporting of unsupported requests.
2	RW	0	**Fatal Error Reporting Enabled (FERE):** Controls reporting of fatal errors. 0 = Disable. 1 = Intel® 6702PXH 64-bit PCI Hub will report fatal errors.
1	RW	0	**Non-Fatal Error Reporting Enabled (NFERE):** Controls reporting of non-fatal errors. 0 = Disable. 1 = Intel® 6702PXH 64-bit PCI Hub will report uncorrectable errors.
0	RW	0	**Correctable Error Reporting Enable (CERE):** Controls reporting of correctable errors. 0 = Disable. 1 = Intel® 6702PXH 64-bit PCI Hub will report correctable errors.

3.5.1.38 Offset 4Eh: EXP_DSTS—PCI Express Device Status Register (D0:F0, F2)

Offset: 4E – 4Fh **Attribute:** RWC; RO
Default Value: 0000h **Size:** 16 bits

This register contains information on the PCI Express device status.

Bits	Type	Reset	Description
15:6	RO	0	Reserved.
5	RO	0	**Transactions Pending (TP):** When this bit is set, the Intel® 6702PXH 64-bit PCI Hub has issued Non-Posted Requests which have not been completed. The Intel® 6702PXH 64-bit PCI Hub reports this bit cleared only when all completions for any outstanding Non-Posted Request have been received. Note that this is a dynamic bit; i.e., this bit could go on and off based on traffic through the Intel® 6702PXH 64-bit PCI Hub.
4	RO	0	**Aux Power Detected (APD):** The Intel® 6702PXH 64-bit PCI Hub does not support aux power and hence this bit is reserved.
3	RWC	0	**Unsupported Request Detected URD):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when any unsupported request from PCI Express* is received. This includes requests that are not claimed by any functions within the Intel® 6702PXH 64-bit PCI Hub, but does NOT include any request that is forwarded to the PCI interface with completions returned with an unsupported request status.
2	RWC	0	**Fatal Error Detected (FERRD):** When set, a fatal error has been detected (regardless of whether an error message was generated or not). This bit remains set until software writes a 1 to clear it.
1	RWC	0	**Non-Fatal Error Detected (NFERRD):** When set, a nonfatal error has been detected (regardless of whether the mask bit was set in advanced error capability or not). This bit remains set until software writes a 1 to clear it.
0	RWC	0	**Correctable Error Detected (CERRD):** When set, a correctable error has been detected (regardless of whether an error message was generated). This bit remains set until software writes a 1 to clear it.

3.5.1.39 Offset 50h: EXP_LCAP—PCI Express Link Capabilities Register (D0:F0, F2)

Offset: 50 – 53h **Attribute:** RO
Default Value: 000B0211h **Size:** 32 bits

This register identifies PCI Express Link specific capabilities.

Bits	Type	Reset	Description
31:18	RO	0	Reserved.
17:15	RO	111b	**L1 Exit Latency (L1EL):** L1 transition is not supported by the Intel® 6702PXH 64-bit PCI Hub.
14:12	RO	110b	**L0s Exit Latency (L0EL):** The value in these bits is influenced by bit 6 in the link control register. Note that software could write the bit 6 in link control register to either a 1 or 0 and these bits should change accordingly. The mapping is shown below: Bit 6 PCI Express Link Control Link Capabilities Bits 14:12 0 110b = 2-4 us 1 010b = 128 ms to less than 256 ms
11:10	RO	1h	**Active State Link PM Support (ASLPMS):** Intel® 6702PXH 64-bit PCI Hub only supports Active State L0s.
9:4	RO	08h	**Maximum Link Width (MLW):** The Intel® 6702PXH 64-bit PCI Hub supports a X8 link maximum.
3:0	RO	1h	**Maximum Link Speed (MLS):** The Intel® 6702PXH 64-bit PCI Hub supports 2.5 Gbps.

3.5.1.40 Offset 54h: EXP_LCNTL – PCI Express Link Control Register (D0:F0, F2)

Offset: 54 – 55h **Attribute:** RW, RO
Default Value: 0000h **Size:** 16 bits

This register controls PCI Express Link specific parameters.

Bits	Type	Reset	Description
15:8	RO	0	Reserved.
7	RW	0	**Extended Synch (EXTS):** This bit when set forces extended transmission of 4096 fast training sequence (FTS) ordered sets in FTS and an extra 1024 training sequence one (TS1) at exit from L1 prior to entering L0. This mode provides external devices monitoring the link time to achieve bit and symbol lock before the link enters L0 state and resumes communication. Default value for this bit is 0.
6	RW	0	**Common Clock Configuration (CCC):** This bit when set indicates that Intel® 6702PXH 64-bit PCI Hub and the component at the opposite end of this Link are operating with a distributed common reference clock. A value of 0 indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. Note that this bit is used to reflect the proper L0s exit latency value in the EXP_LSTS register. Components utilize this common clock configuration information.
5:2	RO	0	Reserved.

Bits	Type	Reset	Description
1:0	RW	0	**Active State Link PM Control (ASLPMC):** Enables Intel® 6702PXH 64-bit PCI Hub to enter L0s, not used by I/OxAPIC in normal operation. 00 L0s entry disabled 01 Intel® 6702PXH 64-bit PCI Hub enters L0s per the specification requirements for L0s entry. 10 L0s entry disabled 11 Intel® 6702PXH 64-bit PCI Hub enters L0s per the specification requirements for L0s entry.

3.5.1.41 Offset 56h: EXP_LSTS – PCI Express* Link Status Register (D0:F0, F2)

Offset: 56 – 57h
Default Value: 0001h (X1 link)
0041h (x4 link)
0081h (X8 link)
Attribute: RO
Size: 16 bits

This register provides information about PCI Express Link specific parameters.

Bits	Type	Reset	Description
15:10	RO	0	Reserved.
9:4	RO	0h (X1) 4h (X4) 8h (X8)	**Negotiated Link Width (NLW):** This field indicates the negotiated width of PCI Express* Link. Defined encodings are: 000000b X1 000100b X4 001000b X8
3:0	RO	0001b	**Link Speed (LS):** This field indicates the negotiated Link speed of the PCI Express Link. The Intel® 6702PXH 64-bit PCI Hub supports only 2.5 Gbps.

3.5.1.42 Offset 5Ch: MSI_CAPID— PCI Express MSI Capability Identifier Register (D0:F0, F2)

Offset: 5Ch
Default Value: 05h
Attribute: RO
Size: 8 bits

This register identifies whether the function is MSI capable.

Bits	Type	Reset	Description
7:0	RO	05h	**Capability ID (CAP_ID):** The value of 05h in this field identifies the function as Message Signaled Interrupt capable.

3.5.1.43 Offset 5Dh: MSI_NXTPTR—PCI Express MSI Next Pointer Register (D0:F0, F2)

Offset: 5Dh **Attribute:** RO
Default Value: 6Ch **Size:** 8 bits

Bits	Type	Reset	Description
7:0	RO	6Ch	**Next Pointer (NXT_PTR):** Pointer to the next item in the capabilities list. Must be NULL for the final item in the list.

3.5.1.44 Offset 5Eh: MSI_MCNTL—PCI Express MSI Message Control Register (D0:F0, F2)

Offset: 5E – 5Fh **Attribute:** RW; RO
Default Value: 0080h **Size:** 16 bits

Bits	Type	Reset	Description
15:8	RO	0	Reserved.
7	RO	1	**64Bit Address Capable (64CAP):** The Intel® 6702PXH 64-bit PCI Hub is capable of generating a 64-bit message address.
6:4	RW	0	**Multiple Message Enable (MMEN):** These bits are RW for software compatibility, but only one message is ever sent by the Intel® 6702PXH 64-bit PCI Hub.
3:1	RO	0	**Multiple Message Capable (MMCAP):** Intel® 6702PXH 64-bit PCI Hub supports only one message.
0	RW	0	**MSI Enable (MSIEN):** If set to a 1, the Intel® 6702PXH 64-bit PCI Hub is permitted to use MSI to request service and is prohibited from using its INTx# pin. Thus MSI would be enabled and SHPC would not use the IRQ[23]# wired to the internal I/OxAPIC to generate interrupts. If set to a 0, the Intel® 6702PXH 64-bit PCI Hub is prohibited from using MSI to request service.

3.5.1.45 Offset 60h: MSI_MA—PCI Express MSI Message Address Register (D0:F0, F2)

Offset: 60 – 63h **Attribute:** RW, RO
Default Value: 00000000h **Size:** 32 bits

Bits	Type	Reset	Description
31:2	RW	0	**Message Address (MESADDR):** Lower 32 bits of the system specified message address, always DWord aligned.
1:0	RO	0	Reserved.

3.5.1.46 Offset 64h: MSI_MUA—PCI Express MSI Message Upper Address Register (D0:F0, F2)

Offset: 64 – 67h **Attribute:** RW, RO
Default Value: 00000000h **Size:** 32 bits

Bits	Type	Reset	Description
31:2	RW	0	**Message Address (MESADDR):** Upper 32 bits of the system specified message address, always DWord aligned.
1:0	RO	0	Reserved.

3.5.1.47 Offset 68h: MSI_MD—PCI Express MSI Message Data Register (D0:F0, F2)

Offset: 68 – 69h **Attribute:** RW
Default Value: 0000h **Size:** 16 bits

Bits	Type	Reset	Description
15:0	RW	0	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (D[15:0]) of the MSI memory write transaction.

3.5.1.48 Offset 6Ch: EXP_CAPSTR – PCI Express Power Management Capability Structure Register (D0:F0, F2)

Offset: 6C – 6Fh **Attribute:** RO
Default Value: 000002xxh **Size:** 32 bits

This register identifies specific PCI Express Power Management capabilities.

Bits	Type	Reset	Description
31:27	RO	19h	**PME_Support (PMES):** The Intel® 6702PXH 64-bit PCI Hub supports PME assertion on behalf of the SHPC when in the **D3**hot state. The Intel® 6702PXH 64-bit PCI Hub does not generate PME from the **D3**cold state.
26	RO	0	**D2 Support (D2S):** The Intel® 6702PXH 64-bit PCI Hub does not support the **D2** device state.
25	RO	0	**D1 Support (D1S):** The Intel® 6702PXH 64-bit PCI Hub does not support the **D1** device state.
24:22	RO	0	**Aux Current (AUXC):** The Intel® 6702PXH 64-bit PCI Hub does not support Aux power.
21	RO	0	**Device Specific Initialization (DSI):** The Intel® 6702PXH 64-bit PCI Hub does not require device specific initialization when transitioned to D0 from D3hot state, so this bit is zero.
20	RO	0	Reserved.
19	RO	0	**PME Clock (PMECLK):** This is not applicable to PCI Express* and hence hardwired to 0.
18:16	RO	02h	**Version (VERS):** The Intel® 6702PXH 64-bit PCI Hub PM Implementation is compliant with the *PCI Power Management Interface Specification,* Revision 1.1.

Bits	Type	Reset	Description
15:8	RO	78h or D8h	**Next Capability Pointer (NCPTR):** Points to the next capability item. Default is 78h when SHPC is enabled (HPA_SLOT[3] = 1), and D8h when SHPC is disabled (HPA_SLOT[3] = 0).
7:0	RO	01h	**Capability ID (CAPID):** Capability ID indicates PCI compatible Power Management.

3.5.1.49 Offset 70h: EXP_PMSTSCNTL – PCI Express Power Management Status and Control Register (D0:F0, F2)

Offset: 70– 73h **Attribute:** RWCS, RWS, RW, RO
Default Value: xx000000h **Size:** 32 bits

Bits	Type	Reset	Description
31:24	RO	0	**Data (DAT):** The Intel® 6702PXH 64-bit PCI Hub does not support this data register.
23:16	RO	0	Reserved.
15	RWCS	0	**PME Status (PMEST):** This bit is set when the Intel® 6702PXH 64-bit PCI Hub would have normally sent a PME request on behalf of SHPC, independent of the state of the **PME_En** bit. The SHPC requests a PME message when the Intel® 6702PXH 64-bit PCI Hub is in the **D3**hot state and a hot plug operation is requested. Refer to the SHPC specification for the details of PME generation.
14:13	RO	0	**Data Scale (DATS):** The Intel® 6702PXH 64-bit PCI Hub does not implement the Data register and hence these two bits are “0.”
12:9	RO	0	**Data Select (DATSEL):** Reserved since the Data register is not implemented.
8	RWS	0	**PME Enable (PME_EN):** Gates assertion of the PME message on behalf of the SHPC.
7:2	RO	0	Reserved.
1:0	RW	00b	**Power State (PWR_ST):** This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The Intel® 6702PXH 64-bit PCI Hub supported field values are given below: 00b – **D0** 01b – Reserved 10b – Reserved 11b – **D3**hot If software attempts to write an unsupported reserved state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.

3.5.1.50 Offset 78h: SHPC_CAPID—SHPC Capability Identifier Register (D0:F0, F2)

Offset: 78h **Attribute:** RO
Default Value: 0Ch **Size:** 8 bits

Note: When hot plug is disabled (HPA_SLOT[3] = 0), this register is RESERVED.

Bits	Type	Reset	Description
7:0	RO	0Ch	**SHPC Capability ID (CAPID):** Used to detect the presence of an SHPC integrated with a PCI-to-PCI bridge. The SHPC Capability ID must be set to 0Ch.

3.5.1.51 Offset 79h: SHPC_NXTP—SHPC Next Item Pointer Register (D0:F0, F2)

Offset: 79h **Attribute:** RO
Default Value: 00h **Size:** 8 bits

Note: When hot plug is disabled (HPA_SLOT[3] = 0), this register is RESERVED.

Bits	Type	Reset	Description
7:0	RO	D8h	**Next Capability Pointer (NXTCP):** The offset of the next capabilities list item if not 0.

3.5.1.52 Offset 7Ah: SHPC_DWSEL—SHPC DWORD Select Register (D0:F0, F2)

Offset: 7Ah **Attribute:** RW/RO
Default Value: 00h **Size:** 8 bits

This register is used to select the DWORD offset in the SHPC working register set for read and write by the SHPC software.

Note: When hot plug is disabled (HPA_SLOT[3] = 0), this register is RESERVED.

Bits	Type	Reset	Description
7:0	RW	0	**DWORD Select (DWS):** Selects the DWORD from the SHPC Working Register set that is accessible through the DWORD Data register. Accesses to the DWORD Data register have no effect on the DWORD Select field. A value of 0 selects the first DWORD of the SHPC Working set. A value of 1 selects the second DWORD, and so on. This field has a default value of 0.

3.5.1.53 Offset 7Bh: SHPC_STS—SHPC Status Register (D0:F0, F2)

Offset: 7Bh **Attribute:** RO
Default Value: x0h **Size:** 8 bits

Note: When hot plug is disabled (HPA_SLOT[3] = 0), this register is RESERVED.

Bits	Type	Reset	Description
7	RO	x	**Controller Interrupt Pending (CIP):** This bit is set when one or more bits are set in the Interrupt Locator register in the SHPC working register set. This bit is cleared when no bits are set in the Interrupt Locator register.
6	RO	x	**Controller System Error Pending (CSP):** This bit is set when one or more bits are set in the SERR Locator register in the SHPC working register set. This bit is cleared when no bits are set in the SERR Locator register.
5:0	RO	0	Reserved.

3.5.1.54 Offset 7Ch: SHPC_DWORD—SHPC Data Register (D0:F0, F2)

Offset: 7C – 7Fh **Attribute:** RW/RO
Default Value: 00000000h **Size:** 32 bits

Note: When hot plug is disabled (HPA_SLOT[3] = 0), this register is RESERVED.

Bits	Type	Reset	Description
31:0	RW	0	**DWORD Data (DWD):** This field allows software to access the SHPC Working Register set via the Capabilities List Item in Configuration Space. The DWORD Select field selects the SHPC Working Register set DWORD that is accessed by reads and writes to this register. Accessing SHPC Working Register set registers through this field behaves the same as accessing them through memory-mapped accesses. Multiple accesses to the DWORD Data register continue to affect the same DWORD if the DWORD Select field is unchanged. If the PCI-to-PCI bridge integrated with the SHPC is not in the D0 power management state, reads from this register must complete successfully but the returned value is undefined and the behavior of writes is undefined.

3.5.1.55 Offset D8h: PA_CAPID—PCI-X Capability Identifier Register (D0:F0, F2)

Offset: D8h **Attribute:** RO
Default Value: 07h **Size:** 8 bits

This register identifies this item in the Capabilities list as a PCI-X register set. It returns 07h when read.

Bits	Type	Reset	Description
7:0	RO	07h	**Capability Identifier (CAPID):** A value of 07h in this field indicates this is a PCI-X capabilities list.

3.5.1.56 Offset D9h: PA_NXTCP—PCI-X Next Capabilities Pointer Register (D0:F0, F2)

Offset: D9h **Attribute:** RO
Default Value: 00h **Size:** 8 bits

This register points to the next item in the Capabilities List, as required by the PCI 2.3 Specification.

Bits	Type	Reset	Description
7:0	RO	0h	**Next Capabilities Pointer (NCPTR):** This is the last capability structure for Intel® 6702PXH 64-bit PCI Hub, so it is hardwired to 0.

3.5.1.57 Offset DAh: PA_SSTS—PCI-X Secondary Status Register (D0:F0, F2)

Offset: DA–DBh **Attribute:** RWC, RO
Default Value: 0003h **Size:** 16 bits

This register controls various modes and features of the PCI-X device.

Bits	Type	Reset	Description
15:9	RO	0	Reserved.
8:6	RO	x	**Secondary Clock Frequency (SCF):** This field is set with the frequency of the secondary bus. The values are: **Bits Max Frequency Clock Period** 000 PCI Mode N/A 001 66 PCI-X Mode 1 15 010 100 PCI-X Mode 1 10 011 133 PCI-X Mode 17.5 1xx Reserved
5	RO	0	**Split Request Delayed. (SRD):** The Intel® 6702PXH 64-bit PCI Hub will never set this bit.
4	RO	0	**Split Completion Overrun (SCO):** The Intel® 6702PXH 64-bit PCI Hub will never set this bit.
3	RWC	0	**Unexpected Split Completion (USC):** 0 = This bit is cleared by writing a 1 to it. 1 = This bit is set if an unexpected split completion with a requester ID equal to the Intel® 6702PXH 64-bit PCI Hub PCI/PCI-X secondary bus number is received on the PCI/PCI-X interface.
2	RWC	0	**Split Completion Discarded (SCD):** 0 = This bit is cleared by writing a 1 to it. 1 = Intel® 6702PXH 64-bit PCI Hub discarded a split completion moving toward the secondary bus because the requester would not accept it.
1	RO	1	**133 MHz Capable (C133):** Hardwired to 1; indicates that the Intel® 6702PXH 64-bit PCI Hub's PCI/PCI-X interface is capable of 133 MHz operation in PCI-X mode.
0	RO	1	**64-bit Device (D64):** Hardwired to 1; indicates the width of the PCI/PCI-X bus is 64 bits.

3.5.1.58 Offset DCh: PA_BSTS—PCI-X Bridge Status Register (D0:F0, F2)

Offset: DC – DFh **Attribute:** RWC, RO
Default Value: 00030000h (PCI Bus A) **Size:** 32 bits

Bits	Type	Reset	Description
31	RO	0	**Reserved**.
30	RO	0	**Reserved**.
29	RO	0	**Device ID Messaging Capable (DIDMC):** The Intel® 6702PXH 64-bit PCI Hub is not capable of forwarding DIM transactions. Hardwired to 0.
28:22	RO	0	Reserved.
21	RWC	0	**Split Request Delayed (SRD):** Hardwired to 0. This bit is not supported by the Intel® 6702PXH 64-bit PCI Hub, because it will never be in a position where it cannot issue a request.
20	RO	0	**Split Completion Overrun (SCO):** Hardwired to 0. This bit is not set by the Intel® 6702PXH 64-bit PCI Hub because the Intel® 6702PXH 64-bit PCI Hub never requests on the PCI Express* interface more data than it has room to receive.
19	RO	0	**Unexpected Split Completion (USC):** The Intel® 6702PXH 64-bit PCI Hub sets this field when a completion on the PCI Express bus is destined to one of the PCI bus segment (either A or B) but the tag does not match.
18	RO	0	**Split Completion Discarded (SCD):** Hardwired to 0. This does not apply to the PCI Express interface.
17	RO	1	**133 MHz Capable (C133):** Hardwired to 1. This field does not apply to PCI Express.
16	RO	1	**64-bit Device (D64):** This field really does not apply to the PCI Express interface, but is set to '1' to be software-compatible.
15:8	RO	0	**Bus Number (BNUM):** This field is an alias to the PBN field of the BNUM register at offset 18h.
7:3	RO	0	**Device Number (DNUM):** The device number is 0 for both Intel® 6702PXH 64-bit PCI Hub bridge segments.
2:0	RO	Bus A – 0h	Function Number (FNUM): 0h for PCI segment A.

3.5.1.59 Offset ECh: PA_ECCFA – Bridge ECC Error First Address Register (D0:F0, F2)

Offset: EC – EFh **Attribute:** ROS
Default Value: 00000000h **Size:** 32 bits

Least significant address bits of the failing transaction.

Bits	Type	Reset	Description
31:0	ROS	0	**ECC First Address (ECC_FA):** If the ECC Error Phase register is non-zero (indicating that an error has been captured), this register indicates the contents of the AD[31::00] bus for the address phase of the transaction that included the error. If the ECC Error Phase is zero, the contents of this register are undefined. This register always records the least significant 32 bits of the address, regardless of the type or length of the transaction, or the phase in which the error occurred. The Intel® 6702PXH 64-bit PCI Hub stores information from the failing transaction directly from the bus (***uncorrected***), even if correction of the error is possible.

3.5.1.60 Offset F0h: PA_ECCSA – Bridge ECC Error Second Address Register (D0:F0, F2)

Offset: F0 – F3h **Attribute:** ROS
Default Value: 00000000h **Size:** 32 bits

Most significant address bits of the failing transaction.

Bits	Type	Reset	Description
31:0	ROS	0	**ECC Second Address (ECC_SA):** If the ECC Error Phase register is non-zero (indicating that an error has been captured), this register indicates the contents of the AD[63::32] bus for the address phase of the transaction that included the error. If the ECC Error Phase is zero, the contents of this register are undefined. This register always records the most significant 32 bits of the address, regardless of the type or length of the transaction, or the phase in which the error occurred. The Intel® 6702PXH 64-bit PCI Hub stores information from the failing transaction directly from the bus (uncorrected), even if correction of the error is possible.

3.5.1.61 Offset F4h: BG_ECCATTR — Bridge ECC Attribute Register (D0:F0, F2)

Offset: F4 – F7h **Attribute:** ROS
Default Value: 00000000h **Size:** 32 bits

Describes the attributes of the ECC.

Bits	Type	Reset	Description
31:0	ROS	0	**ECC Attribute (ECC_AT):** If the ECC Error Phase register bits are non-zero (indicating that an error has been captured), the ECC Attribute register indicates the contents of the AD[31::00] bus for the attribute phase of the transaction that included the error. If the ECC Error Phase registers is zero, the contents of this register are undefined. This register records the contents of the bus during the attribute phase, regardless of the type or length of the transaction, or the phase in which the error occurred. The Intel® 6702PXH 64-bit PCI Hub stores information in this register from the failing transaction directly from the bus (uncorrected), even if correction of the error is possible.

3.6 PCI Express to PCI Bridges (D0:F0, F2) Enhanced

The enhanced PCI Express configuration access mechanism utilizes a flat memory-mapped address space to access device configuration registers. In this case, the memory address determines the configuration register accessed and the memory data returns the contents of the addressed register. Refer to the Section 7.9 in the *PCI Express Base Specification*, Revision 1.0a for details.

3.6.1 Configuration Registers

3.6.1.1 Offset 100h: ENH_CAP – PCI Express Enhanced Capability Register (D0:F0, F2)

Offset: 100 – 103h **Attribute:** RO
Default Value: 30010001h **Size:** 32 bits

All PCI Express extended capabilities must begin with a PCI Express Enhanced Capabilities Register.

Bits	Type	Reset	Description
31:20	RO	300h	**Next Capability Offset (NCO):** Contains the offset to the next PCI Express* Capability Structure, which in this case is power budgeting capability.
19:16	RO	1h	**Capability Version (CAP_VER):** PCI-SIG defined PCI Express Advanced Error Reporting Extended Capability Version Number.
15:0	RO	1h	**PCI Express Extended Capability ID (EXP_XCAPID):** PCI-SIG defined PCI Express Extended Capability ID indicating Advanced Error Reporting Capability.

3.6.1.2 Offset 104h: ERRUNC_STS – PCI Express Uncorrectable Error Status Register (D0:F0, F2)

Offset: 104 – 107h **Attribute:** RWCS, RO
Default Value: 00000000h **Size:** 32 bits

This register reports error status of individual uncorrectable error sources. An individual error status bit that is set to "1" indicates that a particular error occurred; software may clear an error status by writing a 1 to the respective bit. Refer to Section 6.2 of the *PCI Express Base Specification*, Revision 1.0a for details.

Bits	Type	Reset	Description
31:21	RO	0	Reserved.
20	RWCS	0	**Unsupported Request Error Status (URE_STS):** Set by the Intel® 6702PXH 64-bit PCI Hub whenever an unsupported request is detected on the PCI Express* interface including those signaled by the SHPC (on write data parity errors – configuration and memory).
19	RWCS	0	**ECRC Error Status (ECRC_STS):** The Intel® 6702PXH 64-bit PCI Hub does not do ECRC check and this bit is never set.
18	RWCS	0	**Malformed TLP Status (MTLP_STS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when it receives a malformed TLP. Header logging is done.
17	RWCS	0	**Receiver Overflow Status (RO_STS):** The Intel® 6702PXH 64-bit PCI Hub would set this if the PCI Express interface received buffers overflow.

Bits	Type	Reset	Description
16	RWCS	0	**Unexpected Completion Status (EC_STS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit whenever it receives a completion with a requestor ID that does not match either bus segment A or B, or when it receives a completion with a matching requestor ID but an unexpected tag field. The Intel® 6702PXH 64-bit PCI Hub logs the header of the unexpected completion.
15	RWCS	0	**Completer Abort Status (CA_STS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit and logs the header associated with the request when the SHPC signals a completer abort. The Intel® 6702PXH 64-bit PCI Hub logs the header.
14	RWCS	0	**Completion Timeout Status (CT_STS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when inbound memory, configuration, or I/O reads do not receive completions within 16-32ms.
13	RWCS	0	**Flow Control Protocol Error Status (FCP_STS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when there is a flow control protocol error detected.
12	RWCS	0	**Poisoned TLP Status (PTLP_STS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when a poisoned TLP is received from PCI Express. The Intel® 6702PXH 64-bit PCI Hub logs the header of the poisoned TLP packet.
11:5	RO	0	Reserved.
4	RWCS	0	**Data Link Protocol Error Status (DLP_STS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when there is a data link protocol error detected.
3:1	RO	0	Reserved.
0	RO	0	**Training Error (TE):** The Intel® 6702PXH 64-bit PCI Hub does not set this bit.

3.6.1.3 Offset 108h: ERRUNC_MSK – PCI Express Uncorrectable Error Mask Register (D0:F0, F2)

Offset: 108 – 10Bh **Attribute:** RWS, RO
Default Value: 00000000h **Size:** 32 bits

This register controls reporting of individual uncorrectable errors by the Intel® 6702PXH 64-bit PCI Hub to the host bridge via a PCI Express error message and also the logging of the header. Refer to the *PCI Express Base Specification*, Revision 1.0a for details of how the mask bits function. A masked error, a respective bit set to 1 in the mask register, is **not** reported to the host bridge by the Intel® 6702PXH 64-bit PCI Hub, and is not logged in the Header Log register (offset 11Ch - status bits unaffected by the mask bit) and does not update the First Error Pointer (FEPTR, offset 118h, bit 4). There is a mask bit per error bit of the Uncorrectable Error Status register (offset 104h). Refer to Section 6.2 of the *PCI Express Base Specification*, Revision 1.0a for details.

Bits	Type	Reset	Description
31:21	RO	0	Reserved.
20	RWS	0	Unsupported Request Error Mask (UREM)
19	RO	0	**ECRC Error Mask (EEM):** Not applicable to the Intel® 6702PXH 64-bit PCI Hub.
18	RWS	0	Malformed TLP Mask (MTLPM)
17	RWS	0	Receiver Overflow Mask (ROFM)
16	RWS	0	Unexpected Completion Mask (UCM)
15	RWS	0	Completer Abort Mask (CAM)
14	RWS	0	Completion Timeout Mask (CTM)
13	RWS	0	Flow Control Protocol Error Mask (FCPEM)

Bits	Type	Reset	Description
12	RWS	0	Poisoned TLP Mask (PTLPM)
11:5	RO	0	Reserved.
4	RWS	0	Data Link Protocol Error Mask (DLPEM)
3:1	RO	0	Reserved.
0	RO	0	**Training Error Mask (TEM):** Not applicable to the Intel® 6702PXH 64-bit PCI Hub.

3.6.1.4 Offset 10Ch: ERRUNC_SEV – PCI Express Uncorrectable Error Severity Register (D0:F0, F2)

Offset: 10C – 10Fh **Attribute:** RWS, RO
Default Value: 00030010h **Size:** 32 bits

This register controls whether an individual uncorrectable error is reported as a fatal or non-fatal error. An uncorrectable error is reported as fatal (ERR_FATAL) when the corresponding error bit in this register is set to 1. If the bit is cleared, the corresponding error is considered non-fatal (ERR_NONFATAL). Refer to Section 6.2 of the *PCI Express Base Specification*, Revision 1.0a for details.

Bits	Type	Reset	Description
31:21	RO	0	Reserved.
20	RWS	0	**Unsupported Request Error Severity (URES)**
19	RO	0	**ECRC Error Severity (EES):** Not applicable to the Intel® 6702PXH 64-bit PCI Hub.
18	RWS	1	**Malformed TLP Severity (MTLPS)**
17	RWS	1	**Receiver Overflow Error Severity (ROFES)**
16	RWS	0	**Unexpected Completion Error Severity (UCES)**
15	RWS	0	**Completer Abort Error Mask (CAEM)**
14	RWS	0	**Completion Timeout Error Severity (CTES)**
13	RWS	0	**Flow Control Protocol Error Severity (FCPES)**
12	RWS	0	**Poisoned TLP Received (PTLPR)**
11:5	RO	0	Reserved.
4	RWS	1	**Data Link Protocol Error Severity (DLPES)**
3:1	RO	0	Reserved.
0	RO	0	**Training Error Severity (TES):** Not applicable to the Intel® 6702PXH 64-bit PCI Hub.

3.6.1.5 Offset 110h: ERRCOR_STS – PCI Express Correctable Error Status Register (D0:F0, F2)

Offset: 110 – 113Fh **Attribute:** RWCS, RO
Default Value: 00000000h **Size:** 32 bits

This register reports the error status of individual correctable error sources in the Intel® 6702PXH 64-bit PCI Hub. When an individual error status bit is set to a "1", it indicates that a particular error occurred; software may clear an error status by writing a 1 to the respective bit. Refer to Section 6.2 of the *PCI Express Base Specification*, Revision 1.0a for details.

Bits	Type	Reset	Description
31:13	RO	0	Reserved.
12	RWCS	0	**Replay Timer Timeout Status (RTT_STS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit if a replay timer timeout happened.
11:9	RO	0	Reserved.
8	RWCS	0	**REPLAY_NUM Rollover Status (RNR_STS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when the replay number rolls over from 11 to 00.
7	RWCS	0	**Bad DLLP Status (BD_STS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit on CRC errors on Data Link Layer Packets (DLLP).
6	RWCS	0	**Bad TLP Status (BT_STS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit on CRC errors on Transaction Layer Packet (TLP).
5:1	RO	0	Reserved.
0	RWCS	0	**Receiver Error Status (RE_STS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when the physical layer detects a receiver error.

3.6.1.6 Offset 114h: ERRCOR_MSK – PCI Express Correctable Error Mask Register (D0:F0, F2)

Offset: 114 – 117h **Attribute:** RWS, RO
Default Value: 00000000h **Size:** 32 bits

This register controls reporting of individual correctable errors via the ERR_COR message. A masked error (respective bit set in the mask register) is **not** reported to the host bridge by the Intel® 6702PXH 64-bit PCI Hub. There is a mask bit per error in the Correctable Error Status register (offset 110h). Refer to Section 6.2 of the *PCI Express Base Specification*, Revision 1.0a for details.

Bits	Type	Reset	Description
31:13	RO	0	Reserved.
12	RWS	0	**Replay Timer Timeout Mask (RTTM):** The Intel® 6702PXH 64-bit PCI Hub sets this bit if a replay timer timeout happened.
11:9	RO	0	Reserved.
8	RWS	0	**Replay Number Rollover Mask (RNRM):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when the replay number rolls over from 11 to 00.
7	RWS	0	**Bad DLLP Mask (BDM):** The Intel® 6702PXH 64-bit PCI Hub sets this bit on CRC errors on a DLLP.
6	RWS	0	**Bad TLP Mask (BTM):** The Intel® 6702PXH 64-bit PCI Hub sets this bit on CRC errors on a TLP.

Bits	Type	Reset	Description
5:1	RO	0	Reserved.
0	RWS	0	**Receiver Error Mask (REM):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when the physical layer detects a receiver error.

3.6.1.7 Offset 118h: ADVERR_CNTL – Advanced Error Capabilities and Control Register (D0:F0, F2)

Offset: 118 – 11Bh **Attribute:** ROS, RO
Default Value: 00000000h **Size:** 32 bits

The register gives the status and control for ECRC checks and also the pointer to the first uncorrectable error that happened.

Bits	Type	Reset	Description
31:9	RO	0	Reserved.
8	RO	0	**ECRC Check Enable (ECR):** The Intel® 6702PXH 64-bit PCI Hub does not support ECRC check and this bit is reserved.
7	RO	0	**ECRC Check Capable (ECCAP):** The Intel® 6702PXH 64-bit PCI Hub is not ECRC check capable.
6	RO	0	**ECRC Generation Enable (EGE):** The Intel® 6702PXH 64-bit PCI Hub cannot generate an ECRC and this bit is ignored by the Intel® 6702PXH 64-bit PCI Hub.
5	RO	0	**ECRC Generation Capable (EGC):** The Intel® 6702PXH 64-bit PCI Hub cannot generate an ECRC.
4:0	ROS	0	**First Error Pointer (FEPTR):** Identifies the bit position of the first error reported in the Uncorrectable Error Status register. This register re-arms itself (but does not change in value) once the error status bit pointed to by the pointer is cleared by software by writing a 1 to that status bit.

3.6.1.8 Offset 11Ch: EXP_TXNHDLOG – PCI Express Transaction Header Log Register (D0:F0, F2)

Offset: 11C – 11Fh **Attribute:** ROS
Default Value: 0 **Size:** 128 bits

This is a transaction header log for PCI Express errors. Captures the header for the TLP corresponding to a detected error. Refer to Section 6.2 of the *PCI Express Base Specification*, Revision 1.0a for details.

Bits	Type	Reset	Description
127:0	ROS	0	Header of the TLP associated with the error. Once an error is logged in this register, it remains locked for further error loggings until such time software clears the status bit, which re-enables logging of the next error event.

3.6.1.9 Offset 12Ch: UNC_PAERRSTS – Uncorrectable PCI/PCI-X Error Status Register (D0:F0, F2)

Offset: 12C – 12Dh **Attribute:** RWCS, RO
Default Value: 0000h **Size:** 16 bits

This register reports error status of individual errors generated on the PCI or PCI-X secondary bus interface. An individual error status bit that is set to a 1 indicates that a particular error occurred; software may clear an error status by writing a 1 to the respective bit. Refer to Chapter 10 of the *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0 for more details.

Bits	Type	Reset	Description
15:14	RO	0	Reserved.
13	RWCS	0	**Internal Bridge Error (IBERR):** Accounts for internal data errors in the Intel® 6702PXH 64-bit PCI Hub's data queues in either direction. The Intel® 6702PXH 64-bit PCI Hub does NOT log any headers for this error.
12	RWCS	0	**SERR# Assertion Detected (SERRAD):** The Intel® 6702PXH 64-bit PCI Hub sets this bit whenever it detects the PCI PASERR# pin is asserted. There is no header logging associated with the setting of this bit.
11	RWCS	0	**PERR# Assertion Detected (PERRAD):** The Intel® 6702PXH 64-bit PCI Hub sets this bit whenever it detects the PCI bus PAPERR# pin asserted when it is mastering a write (memory, I/O or configuration) or a split/delayed read completion on the PCI bus. The Intel® 6702PXH 64-bit PCI Hub logs the header of the transaction in which the PAPERR# was detected (regardless of the data phase in which it is detected), in the PCI-X header log register. Note that this status bit and also the associated header log are always done irrespective of whether the PAPERR# detected was because of a PCI bus error or because of a forwarded poisoned data. But error message escalation to PCI Express* is done only if the PAPERR# detected and was a NOT because of forwarded poisoned data.
10	RWCS	0	**Delayed Transaction Timer Expired (DTTE):** This bit is set by the Intel® 6702PXH 64-bit PCI Hub if it detects that a DT timeout has happened on a hard DT read stream or on an inbound I/O or configuration transaction. No header is logged.
9	RWCS	0	**Uncorrectable Address Error Detected (UADED):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when it is the target of an inbound transaction and an address parity error was detected by the Intel® 6702PXH 64-bit PCI Hub (regardless of whether the bus mode is PCI or PCI-X Mode 1). The Intel® 6702PXH 64-bit PCI Hub logs the header of the transaction in which it detected the address/attribute parity error in the PCI-X header log register.
8	RWCS	0	**Uncorrectable Attribute Error Detected (UATED):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when it is the target of an inbound transaction and an attribute parity error was detected by the Intel® 6702PXH 64-bit PCI Hub (regardless of whether the bus mode is PCI-X Mode 1). The Intel® 6702PXH 64-bit PCI Hub logs the header of the transaction in which it detected the address/attribute parity error in the PCI-X header log register.
7	RWCS	0	**Uncorrectable Data Error Detected (UDED):** The Intel® 6702PXH 64-bit PCI Hub sets this bit in all PCI modes (PCI, PCI-X Mode 1) when it is the target of an inbound transaction or when it is mastering a PCI delayed read with target sourcing data to the Intel® 6702PXH 64-bit PCI Hub, and a data parity error was detected by the Intel® 6702PXH 64-bit PCI Hub. The Intel® 6702PXH 64-bit PCI Hub logs the header of the transaction in which it detected the data parity error in the PCI-X header log register.
6	RWCS	0	**Uncorrectable Split Completion Message Data Error (USCMDE):** This bit is set when a split completion message is received with an uncorrectable data parity error.

Bits	Type	Reset	Description
5	RWCS	0	**Unexpected Split Completion Error (USCE):** This bit is set when a completion is received from PCI-X that matches the bus number range on the primary side of the Intel® 6702PXH 64-bit PCI Hub, but the RequestorID:tag combination does not match one of the non-posted transactions that Intel® 6702PXH 64-bit PCI Hub has outstanding on the PCI-X bus.
4	RO	0	Reserved.
3	RWCS	0	**Master-Abort Status (MAS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when it is the master of a request transaction on the PCI bus and it received a master abort. The header is logged for that transaction.
2	RWCS	0	**Received Target-Abort Status (RTAS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when it is the master of a request transaction on the PCI bus and it received a target abort. The header is logged for that transaction.
1	RWCS	0	**Master-Abort on Split Completion Status (MA_SCS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when a split completion it sends on the PCI-X bus master aborts. The Intel® 6702PXH 64-bit PCI Hub logs the header of the split completion.
0	RWCS	0	**Target-Abort on Split Completion Status (TA_SCS):** The Intel® 6702PXH 64-bit PCI Hub sets this bit when a split completion it sends on the PCI-X bus target aborts. The Intel® 6702PXH 64-bit PCI Hub logs the header.

3.6.1.10 Offset 130h: UNC_PAERRMSK – Uncorrectable PCI/PCI-X Error Mask Register (D0:F0, F2)

Offset: 130 – 133h **Attribute:** RWS, RO
Default Value: 000017A8h **Size:** 32 bits

This register masks the reporting of individual PCI-X uncorrectable errors via a PCI Express error message. There is one mask bit per error. Note that the status bits are set in the status register irrespective of whether the mask bit is on or off. The mask bit also affects the header log for the PCI-X transaction. If the mask bit is on, the header is not logged and no error message is generated on the PCI Express bus.

Bits	Type	Reset	Description
31:14	RO	0	Reserved.
13	RWS	0	**Internal Bridge Error (IBE)**
12	RWS	1	**SERR# Assertion Mask (SEAM)**
11	RWS	0	**PERR# Assertion Mask (PEAM)**
10	RWS	1	**Delayed Transaction Timer Expired Mask (DTTEM)**
9	RWS	1	**Uncorrectable Address Error Mask (UADDEM)**
8	RWS	1	**Uncorrectable Attribute Error Mask (UATTEM)**
7	RWS	1	**Uncorrectable Data Error Mask (UDEM)**
6	RWS	0	**Uncorrectable Split Completion Message Data Error (USCMDE)**
5	RWS	1	**Unexpected Split Completion Error (USCE)**
4	RO	0	Reserved.
3	RWS	1	**Master-Abort Mask (MAM)**
2	RWS	0	**Received Target-Abort Mask (RTAM)**

Bits	Type	Reset	Description
1	RWS	0	**Master-Abort on Split Completion Mask (MASCM)**
0	RWS	0	**Target-Abort on Split Completion Mask (TASCM)**

3.6.1.11 Offset 134h: UNC_PAERRSEV – Uncorrectable PCI/PCI-X Error Severity Register (D0:F0, F2)

Offset: 134 – 135h **Attribute:** RWS, RO
Default Value: 2340h **Size:** 16 bits

This register controls whether an individual PCI-X uncorrectable error is reported as a fatal or non-fatal error. A PCI-X uncorrectable error, if enabled, is reported as fatal (an ERR_FATAL message will be generated on the PCI Express bus) when the corresponding error bit in the severity register is set to a 1. If a bit is set to 0, then the corresponding error, if enabled, is considered non-fatal (and thus a ERR_NONFATAL message will be generated on the PCI Express bus). There is one mask bit per error.

Bits	Type	Reset	Description
15:14	RO	0	Reserved.
13	RWS	0	**Internal Bridge Error Severity (IBES)**
12	RWS	1	**SERR# Assertion Severity (SEAS)**
11	RWS	0	**PERR# Assertion Severity (PEAS)**
10	RWS	0	**Delayed Transaction Timer Expired Severity (DTTES)**
9	RWS	1	**Uncorrectable Address Error Severity (UADDES)**
8	RWS	1	**Uncorrectable Attribute Error Severity (UATTES)**
7	RWS	0	**Uncorrectable Data Error Severity (UDES)**
6	RWS	1	**Uncorrectable Split Completion Message Data Error Severity (USCMDES)**
5	RWS	0	**Unexpected Split Completion Error Severity (USCES)**
4	RWS	0	Reserved.
3	RWS	0	**Master-Abort Severity (MAS)**
2	RWS	0	**Received Target-Abort Severity (RTAS)**
1	RWS	0	**Master-Abort on Split Completion Severity (MASCS)**
0	RWS	0	**Target-Abort on Split Completion Severity (TASCS)**

3.6.1.12 Offset 138h: UNC_PAERRPTR – Uncorrectable PCI/PCI-X Error Pointer Register (D0:F0, F2)

Offset: 138 – 13Bh **Attribute:** ROS, RO
Default Value: 00000000h **Size:** 32 bits

This register points to the bit position of the first error reported in the Uncorrectable PCI/PCI-X Error Status register (offset 12Ch). This register is rearmed when the bit position pointed to is cleared in the associated status register. The pointer value is not updated when this register is rearmed.

Bits	Type	Reset	Description
31:5	RO	0	Reserved.
4:0	ROS	0	**Uncorrectable PCI/PCI-X First Error Pointer (UPFEP):** This register points to the first error that was logged in the Uncorrectable PCI/PCI-X Error Status register (offset 12Ch). This register rearms itself when the status bit corresponding to the error which this register is pointing to is cleared by software writing a 1 to the bit.

3.6.1.13 Offset 13Ch: PA_TXNHDLOG – PCI/PCI-X Uncorrectable Transaction Header Log (D0:F0, F2)

Offset: 13C – 143h **Attribute:** ROS
Default Value: 0h **Size:** 128 bits

The log in this register captures the header for the transaction that generated an error. Once an error is logged in this register, this register is locked from further error loggings, until software clears the status bit corresponding to the first uncorrectable error that occurred. When this bit is cleared by software, this register is rearmed for further header logs.

Bits	Type	Reset	Description
127:64	ROS	0	**Transaction Address (TXNAD):** These bits capture the 64-bit value transferred on PAAD[31:0] during the 1st and 2nd address phase of the transaction in which an error was detected. The 1st address phase is logged to bits 95:64 and the 2nd address phase is logged to bits 127:96. In case of a 32-bit address, bits 127:96 will be set to all zeros. The address is logged on all error conditions.
63:44	RO	0	Reserved.
43:40	ROS	0	**Transaction Command Upper (TXNCU):** This captures the value of PAC/BE[3:0]# during the 2nd address phase of a DAC transaction Contains the 4-bit value transferred on PAC/BE[3:0]# during the 2nd attribute phase of the transaction.
39:36	ROS	0	**Transaction Command Lower (TXNCL):** This captures the value of PAC/BE[3:0]# during the 1st address phase of the transaction. Contains the 4-bit value transferred on PAC/BE[3:0]# during the 1st attribute phase of the transaction.
35:0	ROS	0	**Transaction Attribute (TXNAT):** This carries the attribute of the transaction. Contains the 36-bit value transferred on PAC/BE[3:0]# and PAAD[31:0]) during the attribute phase of the transaction. When the bus is in PCI mode, these bits are all zeros.

3.6.1.14 Offset 14Ch: PA_DERRLOG – PCI-X Un/Correctable Data Error Log Register (D0:F0, F2)

Offset: 14C – 153h **Attribute:** ROS
Default Value: 0000000000000000h **Size:** 64 bits

This register is logged for all correctable or uncorrectable data parity errors.

Bits	Type	Reset	Description
63:0	ROS	0	**PCI-X Data Log (PDL):** This register is logged with the PCI data bus value whenever the Intel® 6702PXH 64-bit PCI Hub is the target of a data transfer and it detects a data parity error (correctable or uncorrectable). This register is not defined if the log valid bit in the error log and control register is not set. This register re-arms itself for loading again when software clears the log valid bit by writing a 1 to that bit. For 32-bit data transfers, only the lower 32 bits are logged.

3.6.1.15 Offset 154h: PA_MISCERRLOG – Other PCI-X Error Logs and Control Register (D0:F0, F2)

Offset: 154 – 155h **Attribute:** RWCS, ROS, RO
Default Value: 0000000000000000h **Size:** 32 bits

This register contains bits logged for uncorrectable data parity errors (in PCI or PCI-X Mode 1), uncorrectable address/attribute parity errors and PCI REQ# line of failure.

Bits	Type	Reset	Description
31:19	RO	0	Reserved.
18	ROS	0	**Data Log (DATA_LOG):** A “1” indicates the data log is from a correctable ECC data error. A 0 indicates the data log is from an uncorrectable ECC/parity error. This bit is logged along with the DLOG register and is rearmed when the log valid bit is cleared. This is also only valid when the log valid bit is set by the Intel® 6702PXH 64-bit PCI Hub.
17	ROS	0	**PCI-X Attribute Parity (PP)**: This bit indicates that parity was detected in the attribute phase of a request and completion. When the Intel® 6702PXH 64-bit PCI Hub is driving, it is the value driven. When the Intel® 6702PXH 64-bit PCI Hub is receiving, it is the value captured. This bit is only valid in PCI-X Mode 1 operation. This bit is logged along with the Secondary Header Log register (SEC_HDLOG, offset 13Ch) when there is an attribute parity error. This bit is not loaded for any other error conditions. This bit remains set until software clears the corresponding status bit in the Secondary Uncorrectable Error Status register (SEC_UNC_ERRSTS, offset 12Ch).
16	ROS	0	**PCI Address High (PAH):** This bit represents the parity detected in the 2nd phase (upper 32-bits) of a dual address cycle. This bit is forced to ‘0’ if the address was a single address cycle. When the Intel® 6702PXH 64-bit PCI Hub is driving, this bit contains the value driven. When the Intel® 6702PXH 64-bit PCI Hub is receiving, this bit contains the value captured. This is only valid in PCI-X Mode 1 operation. This bit is logged along with the Secondary Header Log register (SEC_HDLOG, offset 13Ch) when there is an address parity error (this bit is never loaded independently of the Secondary Header Log register). This bit is not loaded for any other error conditions. This bit remains set until software clears the corresponding status bit in the Secondary Uncorrectable Error Status register (SEC_UNC_ERRSTS, offset 12Ch).

Bits	Type	Reset	Description
15	ROS	0	**PCI Address Low (PAL):** For PCI-X requests and all PCI cycles, this bit represents the parity detected in the 1st phase (lower 32-bits) of a dual address cycle, or just the address of a regular address cycle. For PCI-X completions, this bit represents the 1st clock (requester attributes) driven in the completion cycle. When the Intel® 6702PXH 64-bit PCI Hub is driving, this bit contains the value driven. When the Intel® 6702PXH 64-bit PCI Hub is receiving, this bit contains the value captured. This is only valid in PCI-X Mode 1 operation. This bit is logged along with the Secondary Header Log register (SEC_HDLOG, offset 13Ch) when there is an address parity error (this bit is never loaded independently of the PCI-X Header Log register). This bit is not loaded for any other error conditions. This bit remains set until software clears the corresponding status bit in the Secondary Uncorrectable Error Status register (SEC_UNC_ERRSTS, offset 12Ch).
14	RWCS	0	**REQ# Log Valid (RLV):** This bit is set when REQ# log bits (bits 13:11 of this register) are valid. Clearing this bit will re-enable logging into the REQ# log register bits.
13:11	ROS	0	**REQ# Log (RL):** These bits capture the REQ# of the PCI agent mastering the transaction when the Intel® 6702PXH 64-bit PCI Hub detected a correctable or uncorrectable address, attribute or data parity error. That is, the REQ# log is valid when either of the three error conditions occur that cause either of bits 9:7 to be set or any errors occur that cause the error phase register bits in the Bridge ECC Control and Status register (BG_ECCSTS, offset E8h) to be non-zero. Once a log is made in the REQ# log, further logging of the REQ# log bits is stopped till the REQ# log valid bit (bit 14 of this register) is cleared. Note that this register is not dependent on the clearing of status bits in the Secondary Uncorrectable Error Status register (SEC_UNC_ERRSTS, offset 12Ch) or the Bridge ECC Attribute register (BG_ECCATTR, offset F4h), to rearm itself. 000 = REQ0 001 = REQ1 010 = REQ2 011 = REQ3 100 = REQ4: 101 = REQ5 110 = REQ6 111 = Reserved
10	RO	0	Reserved.
9	RWCS	0	**Log Valid (LOGV):** This is set by the Intel® 6702PXH 64-bit PCI Hub whenever it logs a value in the Data Log register (offset 14Ch) and also the byte enable log bits in this register (offset 154h, bits 7:0). Software clears this register by writing a 1, which will rearm the Data Log register (offset 14Ch) and enable the byte enable log register bits (bits 7:0 of this register) to start loading again.
8	ROS	0	**Data Bus Width (DBW):** This bit is set if the data logged in the Data Log register is 64 bits. Otherwise this bit is clear. When clear the upper 32 bits of the Data Log registers are invalid.
7:0	ROS	0	**PCI-X Byte Enable Log (PABEL):** This error is logged whenever the Intel® 6702PXH 64-bit PCI Hub is the target of a data transfer and it detects a data parity/ECC error (correctable or uncorrectable). This register is logged along with the Data Log register. This register is not defined if the log valid bit (bit 9 above) is not set. This register re-arms itself for loading again when software clears the log valid bit by writing a one to that bit.

3.6.1.16 Offset 170h: PXH_STPSTS – Intel® 6702PXH 64-bit PCI Hub Strap Status Register (D0:F0, F2)

Offset: 170 – 171h **Attribute:** RO
Default Value: xxxxh **Size:** 16 bits

This register indicates the status of various Power-On straps on the Intel® 6702PXH 64-bit PCI Hub.

Bits	Type	Reset	Description
15	RO	0	Reserved.
14	RO	Strap	**Reserved.**
13:12	RO	0	Reserved.
11:8	RO	Strap	**PCI Slot Count (PSC):** Reflects the value of the HPASLOT[3:0]# pins sampled at the rising edge of PWROK.
7:1	RO	Strap	**Manageability Address (MA):** These 7 bits represent the address the SMBus slave port will respond to when an access is attempted. This register will have the following value: **Bit Value** 7 '1' 6 '1' 5 SMBUS[7] 4 '0' 3 SMBUS[6] 2 SMBUS[5] 1 SMBUS[4]
0	RO	Strap	**P133EN Status (133EN_STS):** Reflects the status of the PA133EN pin sampled at rising edge of PWROK.

3.6.2 Power Management Registers

This configuration space follows the standard PCI-to-PCI bridge configuration space format. Table 3-2 shows the Intel® 6702PXH 64-bit PCI Hub power management registers and their address byte offset values.

Note: Registers that are not shown should be treated as Reserved.

Table 3-2. Power Management Register Summary

Address Offset	Symbol	Register Name	Default	Access
300–303h	PWR_BUDCAP	Power Budgeting Enhanced Capability Register	00010004h	RO
304h	PWR_DATASEL	Power Budgeting Data Select Register	00h	RW
308–30Bh	PWR_DATAREG	Power Budgeting Data Register	00000000h	RO
30C–30Dh	PWR_BUDREG	Power Budgeting Register	0000h	RWO
314h–...	PWR_BUDREG0	Power Budgeting Register 0...	0000h	RO, RW
...–374h	PWR_BUDREG23	Power Budgeting Register 23	0000h	RO, RW

3.6.2.1 Offset 300h: PWR_ENH_BUDCAP – Power Budgeting Capability Header Register (D0:F0, F2)

Offset: 300 – 303h **Attribute:** RO
Default Value: 00010004h **Size:** 32 bits

Refer to Section 7.9.3 of the *PCI Express Base Specification*, Revision 1.0a for details.

Bits	Type	Reset	Description
31:20	RO	0	**Next Capability Offset (NCAPOFF):** This field contains the offset to the next PCI Express* capability structure or a 000h if no other items exist in the linked list of capabilities. The 0000h value indicates that this is the last capability.
19:16	RO	1h	**Capability Version (CAPVER):** PCI-SIG defined version number that indicates the version of the capability structure present. Indicates 1.
15:0	RO	4h	**PCI Express Extended Capability ID (PEECAPID):** PCI-SIG defined extended capability ID. A value of 0004h indicates power budgeting capability.

3.6.2.2 Offset 304h: PWR_DATSEL – Power Budgeting Data Select Register (D0:F0, F2)

Offset: 304h **Attribute:** RW
Default Value: 00h **Size:** 8 bits

This register indexes the Power Budgeting Data reported through the Data register (DATREG, offset 308h) and selects the DWORD of Power Budgeting Data that should appear in the Data register.

Bits	Type	Reset	Description
7:0	RW	0h	**Data Select (DSEL):** This read-write register indexes the Power Budgeting Data reported through the Data register (DATREG, offset 308h) and selects the DWORD of Power Budgeting Data that should appear in the Data Register. Index values for this register start at 0 to select the first DWORD of Power Budgeting Data; subsequent DWORD's of Power Budgeting Data are selected by increasing index values. A value of 0 selects the DWORD data starting at address 0x314 to appear in the data register at offset 0x308, a value of 1 selects the DWORD data starting at address 0x318 to appear in the in the data registers at offset 0x308, and so on. Values greater than 23 for this register will report all zeros in the data register.

3.6.2.3 Offset 308h: PWR_DATREG – Power Budgeting Data Register (D0:F0, F2)

Offset: 308 – 30Bh **Attribute:** RO
Default Value: 00000000h **Size:** 32 bits

This register returns a DWORD Power Budgeting Data selected by the Data Select Register (DSEL, offset 304h). Each DWORD of the Power Budgeting Data describes the power usage of the Intel® 6702PXH 64-bit PCI Hub. The Intel® 6702PXH 64-bit PCI Hub reports its power consumption for Power Management states: D0, D3; Types: idle, sustained and max; Power rails: 12V, 3.3V, 1.8V and thermal.

Bits	Type	Reset	Description
31:21	RO	0	Reserved.

Bits	Type	Reset	Description
20:18	RO	0	**Power Rail (PWR_R):** Specifies the power rail of the operating condition being described. Defined encodings applicable to the Intel® 6702PXH 64-bit PCI Hub are: 0000b = 12V 001b = 3.3V 010b = 1.8V 111b = Thermal
17:15	RO	0	**Type (TYPE):** Specifies the type of the operating condition being described. Defines encodings are: 010b = Idle 011b = Sustained 111b = Maximum
14:13	RO	0	**PM State (PMST):** Specifies the Power Management state of the operating condition being described. Defines encodings are: 00b = D0 11b = D3
12:0	RO	0	Reserved.

3.6.2.4 Offset 30Ch: PWR_BUDREG – Power Budgeting Capability Register (D0:F0, F2)

Offset: 30Ch **Attribute:** RO, RWO
Default Value: 0h **Size:** 8 bits

This register indicates the Power Budgeting capabilities of the Intel® 6702PXH 64-bit PCI Hub.

Bits	Type	Reset	Description
7:1	RO	0	Reserved.
0	RWO	0	**System Allocated (SYSA):** When set to a 1, this bit indicates that the power budget for the Intel® 6702PXH 64-bit PCI Hub is included within the system power budget. Reported Power Budgeting Data for this device should be ignored by software for power budgeting decisions if this bit is set to a 1.

3.6.2.5 Offset 314h: PWR_BUDREG0 – Power Budgeting Register 0 (D0:F0, F2)

Offset: 314 – 317h **Attribute:** RO, RW
Default Value: 00000000h **Size:** 32 bits

This register reports various power consumption values in various power states.

Bits	Type	Reset	Description
31:21	RO	0	Reserved.
20:0	RW	0	**Power Budgeting Register 0 (PWRBUDREG0):** Software can program this field to report various power consumption values in various power states. Refer to the *PCI Express Base Specification, Revision 1.0a* for the format of this field for reporting the various power consumption values.

3.6.2.6 Offset 318h, 320h,...374hh: PWR_BUDREG1 — PWR_BUDREG23 Register (D0:F0, F2)

Offset: 318h – 31Bh, 320h – 32Bh, etc. **Attribute:** RO, RW
Default Value: 00000000h **Size:** 32 bits

Power Budgeting Registers 1 through 23 are the same as the Power Budgeting Register 0 above.

Offset	Register	Description
318h–31Bh	Power Budgeting Register 1	Same as Power Budgeting Register 0 (PWRBUDREG0), offset 314h.
31Ch–31Fh	Power Budgeting Register 2	
320h–323h	Power Budgeting Register 3	
324h–327h	Power Budgeting Register 4	
328h–32Bh	Power Budgeting Register 5	
32Ch–32Fh	Power Budgeting Register 6	
330h–333h	Power Budgeting Register 7	
334h–337h	Power Budgeting Register 8	
338h–33Bh	Power Budgeting Register 9	
33Ch–33Fh	Power Budgeting Register 10	
340h–343h	Power Budgeting Register 11	
344h–347h	Power Budgeting Register 12	
348h–34Bh	Power Budgeting Register 13	
34Ch–34Fh	Power Budgeting Register 14	
350h–353h	Power Budgeting Register 15	
354h–357h	Power Budgeting Register 16	
358h–35Bh	Power Budgeting Register 17	
35Ch–35Fh	Power Budgeting Register 18	
360h–363h	Power Budgeting Register 19	
364h–367h	Power Budgeting Register 20	
368h–36Bh	Power Budgeting Register 21	
36Ch–36Fh	Power Budgeting Register 22	Same as Power Budgeting Register 0 (PWRBUDREG0), offset 314h.
370h–373h	Power Budgeting Register 23	

3.7 Hot Plug Controller Registers

The Intel® 6702PXH 64-bit PCI Hub hot plug controller allows PCI card removal, replacement and addition without powering down the system.

3.7.1 Configuration Registers

Table 3-3. Hot Plug Controller Register Summary

Address Offset	Symbol	Register Name	Default	Access
00–03h	SHPC_BASEOFF	SHPC Base Offset Register	00000000h	RO
04–07h	SLOTS_AVAIL1	Slots Available I Register	00000000h	RWO
08–0Bh	SLOTS_AVAIL2	Slots Available II Register	00000000h	RWO
0C–0Fh	SLOT_CONFIG	Slot Configuration Register	00000000h	RWO
10–11h	SBUS_CONFIG	Secondary Bus Configuration Register	0000h	RO
12h	SHPC_MSI_CNTL	SHPC MSI Control Register	00h	RO
13h	SHPC_PROG_IF	SHPC Programming Interface Register	01h	RO
14–15h	CONT_COMMAND	Controller Command Register	0000h	RW
16–17h	CONT_COMMAND_ STS	Controller Command Status Register	0000h	RO
18–1Bh	INT_LOC	Interrupt Locator Register	00000000h	RO
1C–1Fh	SERR_LOC	SERR Locator Register	00000000h	RO
20–23h	SERR_INT	Controller SERR-INT Enable Register	0000000Fh	RW, RWC
24–3Bh	1_LSR	1st Logical Slot Register	8F00xxxxh	RW
	2_LSR	2nd Logical Slot Register		RW
	3_LSR	3rd Logical Slot Register		RW
	4_LSR	4th Logical Slot Register		RW
	5_LSR	5th Logical Slot Register		RW
	6_LSR	6th Logical Slot Register		RW

3.7.1.1 Offset 00h: SHPC_BASEOFF—SHPC Base Offset Register

Offset: 00–03h **Attribute:** RO
Default Value: 00000000h **Size:** 32 bits

This register is used by software and/or BIOS (in conjunction with the SHPC Base Address Register, SHPC_BAR) to determine the memory base address of the SHPC Working Register set. This register must be accessed initially via Configuration Space.

Bits	Type	Reset	Description
31:0	RO	0	**SHPC Base Offset (SHPCBO):** This field contains the byte offset that must be added to the 64-bit Base Address register SHPC_BAR in the Intel® 6702PXH 64-bit PCI Hub's configuration space to access the SHPC Working Register set using memory-mapped accesses. The Intel® 6702PXH 64-bit PCI Hub has the working register set starting at offset 0.

3.7.1.2 Offset 0Ch: SLOT_CONFIG—Slot Configuration Register

Offset: 0C–0Fh **Attribute:** RWO, RO
Default Value: 00000000h **Size:** 32 bits

This register describes the configuration of the slots controlled by the SHPC.

Bits	Type	Reset	Description
31	RWO	0	**Attention Button Implemented (ABI):** This bit specifies whether the hot plug slots controlled by this SHPC implement the optional Attention Button. If this bit is set, Attention Buttons are implemented on every PCI slot controlled by this SHPC.
30	RWO	0	**MRL Sensor Implemented (MRLSI):** This bit specifies whether MRL Sensors are implemented on the hot plug slots controlled by the SHPC. If this bit is set, the platform provides an MRL Sensor for each slot controlled by this SHPC.
29	RWO	0	**Physical Slot Number Up/Down (PSNUD):** This bit specifies the direction of enumeration of external slot labels, beginning with the value in the Physical Slot Number field (PSN) of this register (offset 0C-0Fh, bits 26:6). If this bit is set, each external slot label increments by 1 from the value in the Physical Slot Number field. If this bit is cleared, each external slot label decrements by 1 from the value in the Physical Slot Number field.
28:27	RO	0	Reserved.
26:16	RWO	0	**Physical Slot Number (PSN):** This field specifies the physical slot number of the device addressed by the First Device Number (FDN) at bits 12:8 of this register. This field must be hardware initialized to a value that assigns all slots (controlled by this SHPC) a slot number that is globally unique within the chassis.
15:13	RO	0	Reserved.
12:8	RWO	0	**First Device Number (FDN):** This field contains the device number assigned to the first hot plug slot on this bus segment.
7:5	RO	0	Reserved.
4:0	RWO	0	**Number of Slots Implemented (NSI):** This field contains the number of hot plug slots connected to the SHPC (that is, the number of slots controlled by the SHPC). This field must not return a value of 0. (If the controller does not control any slots in the system, the SHPC Capabilities List Item must not appear in the Capabilities List).

3.7.1.3 Offset 10h: SBUS_CONFIG

Offset: 10h **Attribute:** RO
Default Value: 00h **Size:** 16 bits

This register reflects the current speed and mode of PCI bus.

Bits	Type	Reset	Description
15:3:	RO	0	Reserved.
2:0	RO	0	**Current Bus Segment Speed/Mode:** Indicates the current speed and mode at which the PCI bus segment is operating. 000 : 33 MHz Conv 001 : 66 MHz Conv 010 : 66 MHz PCI-X Mode 011 : 100 MHz PCI-X Mode 100 : 133 MHz PCI-X Mode Others : Reserved

3.7.1.4 Offset 12h: SHPC_MSI_CNTL—SHPC MSI Control Register

Offset: 12h **Attribute:** RO
Default Value: 00h **Size:** 8 bits

This register indicates the specific message number that will be used by the SHPC to signal an interrupt when using Message Signaled Interrupts (MSI).

Bits	Type	Reset	Description
7:5	RO	0	Reserved.
4:0	RO	0	**SHPC Interrupt Message Number (SHPC_IMN):** Reflects the Multiple Message Enable field (MMEN, bits 6:4) of the MSI Capability Control register (MSI_MCNTL, offset 5Eh).

3.7.1.5 Offset 13h: SHPC_PROG_IF—SHPC Programming Interface Register

Offset: 13h **Attribute:** RO
Default Value: 01h **Size:** 8 bits

Identifies the format of the working register set.

Bits	Type	Reset	Description
7:0	RO	0	**SHPC Programming Interface:** Identifies the format of the SHPC Working Register set. A value of 01h identifies the SHPC Working Register set format defined in 1.0 specification.

3.7.1.6 Offset 14h: CONT_COMMAND—Controller Command Register

Offset: 14–15h **Attribute:** RW, RO
Default Value: 0000h **Size:** 16 bits

Bits	Type	Reset	Description
15:13	RO	0	Reserved.
12:8	RW	0	**Target Slot (TS):** This field selects the target slot for a Slot Operation command. For example, writing a 2 to this field would select the 2nd slot for the Slot Operation command. Software is permitted to write the Command Code and Target Slot fields simultaneously. However, software is not required to write these fields simultaneously. If the fields are not written simultaneously, the Slot Operation command targets the slot associated with the current value in this register. If the command is not a Slot Operation command, this field is ignored. When this field is read, it returns the value that was last written to it, even after the command has completed.
7:0	RW	0	**Command Code (CCODE):** Command to be executed by the SHPC. Writing to this field triggers the SHPC to begin executing the command. Refer to the *Standard Hot-Plug Controller and Subsystem Specification, Rev 1.0* for command encodings. When read, this field returns the command code that was last written to it, even after the command has completed.

3.7.1.7 Offset 16h: CONT_COMMAND_STS—Controller Command Status Register

Offset: 16–17h **Attribute:** RO
Default Value: 0000h **Size:** 16 bits

Bits	Type	Reset	Description
15:4	RO	0	Reserved.
3:1	RO	0	**Controller Command Error Code (CCEC):** This field shows the result of the last command completed by the SHPC. This field is updated when the Controller Busy bit (offset 16-17h, bit 0) transitions from 1 to 0 (indicating a command completion). If the command failed, the appropriate bit is set. If none of the bits in this field are set, the command completed successfully.
0	RO	0	**Controller Busy (CB):** This bit changes from 0 to 1 when a command code is written to the Controller Command register (CONT_COMMAND, offset 14h). It stays set until the SHPC has completed executing the command. The SHPC ignores writes to the Controller Command register (CONT_COMMAND, offset 14h) while this bit is set. This bit changes from 1 to 0 when the SHPC finishes executing a command. The SHPC must not set this bit for any other reason. For example, this bit must not be set to 1 when the SHPC automatically powers down the slot in response to detecting a MRL open event.

3.7.1.8 Offset 18h: INT_LOC—Interrupt Locator Register

Offset: 18 – 1Bh **Attribute:** RO
Default Value: 00000000h **Size:** 32 bits

Interrupt locator register for software to easily identify the source of an interrupt.

Bits	Type	Reset	Description
31:8	RO	0	Reserved.
7:1	RO	0	**Slot n Interrupt Pending Bits (SNIPB):** A set bit in this field indicates an interrupt pending condition on the associated slot. An interrupt pending condition occurs when the SHPC detects a Slot Event, and the event's Command Complete Interrupt Mask bit (CCIM, bit 2) in the Slot SERR-INT Mask field is cleared. Multiple bits are set if multiple slots have an interrupt pending. Clearing all bits in the Slot Event Latch field (SEL, bit) of the slot's Logical Slot register (LSR_SLOT, offset 24h) clears that slot's bit in this field.
0	RO	0	**Command Complete Interrupt Pending (CCIP):** The state of this bit is 1 when the Command Completion Detected bit (CCIM, bit 2) in the Slot SERR-INT Mask field (offset 20h) is set indicating a command completion and the Command Complete Interrupt Mask bit located in the Controller SERR-INT Enable register (SERR_INT, offset 20h) is cleared.

3.7.1.9 Offset 1Ch: SERR_LOC—SERR Locator Register

Offset: 1C – 1Fh **Attribute:** RO
Default Value: 00000000h **Size:** 32 bits

System Interrupt locator register for software to easily identify the source of interrupt.

Bits	Type	Reset	Description
31:8	RO	0	Reserved.
7:1	RO	0	**Slot n SERR Pending (SNSP):** A set bit in this field indicates an SERR pending condition on the associated slot. An SERR pending condition occurs when the SHPC detects a slot event capable of generating an SERR and that event's SERR Mask bit in the Slot SERR-INT Mask field is cleared. Multiple bits are set if multiple slots have an SERR pending. Clearing all bits in the slot's Slot Event Latch field that are capable of generating an SERR clears that slot's bit in this field.
0	RO	0	**Arbiter SERR Pending (ASP):** The state of this bit is 1 when the Arbiter Timeout Detected bit (ATD, bit 17) in the Controller SERR-INT Enable register (SERR_INT, offset 20h) is set and the Arbiter SERR Mask bit (ASM, bit 3) is cleared.

3.7.1.10 Offset 20h: SERR_INT—Controller SERR_INT Enable Register

Offset: 20–23h **Attribute:** RW, RWC, RO
Default Value: 0000000Fh **Size:** 32 bits

This register enables and disables SERR and System generation and reports global controller events.

Bits	Type	Reset	Description
31:18	RO	0	Reserved.
17	RWC	0	**Arbiter Timeout Detected (ATD):** This bit is set when the SHPC detects an arbiter timeout.
16	RWC	0	**Command Completion Detected (CCD):** This bit is set when the Controller Busy bit (CB, bit 0) in the Controller Command Status register (CONT_COMMAND_STS, offset 16h) transitions from 1 to 0 (indicating a command completion).
15:4	RO	0	Reserved.
3	RW	1	**Arbiter SERR Mask (ASM):** When this bit is set, arbiter timeout SERRs are masked. This bit is a mask and does not affect whether the Arbiter Timeout Detected bit (bit 17 of this register) is set. When this mask is cleared and the global SERR mask (bit 1 below) is clear, arbiter timeout error will cause ERR_NONFATAL message on the PCI Express* bus, provided the SERR enable bit is set in the PCICMD register or the nonfatal message enable bit is set in the PCI Express capability.
2	RW	1	**Command Complete Interrupt Mask (CCIM):** When this bit is set, command Completion Interrupts are masked. This bit is a mask and does not affect whether the Command Completion Detected bit (CCD, bit 16 of this register) is set.
1	RW	1	**Global SERR Mask (GSM):** When this bit is set, SERR generation from the SHPC is masked.
0	RW	1	**Global Interrupt Mask (GIM):** When this bit is set, System Interrupt generation by the SHPC is masked. This bit is a mask and does not affect any bits in the Interrupt Locator register. This bit has no effect on whether the Wakeup Signal is asserted.

3.7.2 Offset 24h – 40h: Logical Slot Registers (LSR) 1 to 6

Software uses the Logical Slot Register for the following:

- Current status of the slot
- Configure system interrupts and system errors generated by the slots
- Detect pending events on the slots

Each Logical Slot Register is formatted as follows and is described in further detail below.

31 24	23 16	15 0
Slot SERR-INT Mask	Slot Event Latch	Slot Status

3.7.2.1 SSTS – Slot Status Field, Bits [15:0]

This field contains status information about the slot.

Bits	Type	Reset	Description
15	RO	0	Reserved.
14	RO	0	Reserved.
13:12	RO	xx	**PCI-X Capability (PCI-X_CAP):** These bits report the current PCI-X capability of the add-in card installed in the slot. These bits are not valid if the slot is empty. If the slot is occupied, these bits are valid regardless of the state of the slot or speed/mode of the bus. 00b Non PCI-X 01b 66 MHz PCI-X Mode 10b Reserved 11b 133 MHz PCI-X Mode
11:10	RO	xx	**PRSNT1#/PRSNT2# (PRSNT1_PRSNT2):** These bits report the current de-bounced state of the PRSNT1# and PRSNT2# slot pins. These bits are valid regardless of the state of the slot or speed/mode of the bus. 00b Card Present; 7.5W 01b Card Present; 25W 10b Card Present; 15W 11b Slot Empty
9	RO	x	**66 MHz Capable (HP_M66EN):** This bit reports whether the add-in card is capable of running at 66 MHz conventional mode. This bit is latched as the slot is powered up or enabled, regardless of the current speed/mode of the bus. If this bit is 1, the card is capable of running at 66 MHz conventional mode. If this bit is 0, the card is only capable of 33 MHz conventional mode operation. This bit is valid only when the slot is occupied and powered or enabled.
8	RO	x	**MRL Sensor (HP_MRL):** This bit reports the current state of the MRL as reported by the de-bounced MRL Sensor input signal. If this bit is 1, the MRL Sensor is reporting that the MRL is open. If this bit is 0, the MRL Sensor is reporting that the MRL is closed.
7	RO	x	**Attention Button (ATTBUT):** This bit reports the current state of the de-bounced Attention Button input signal for this slot. If this bit is 1, the Attention Button is being pressed. If this bit is 0, the Attention Button is not being pressed.
6	RO	x	**Power Fault (PWRFLT):** This bit reports the current state of the power fault latch in the power controller circuitry for this slot. If this bit is 1, a power fault (either isolated or connected) has been detected by the power controller circuitry.
5:4	RO	x	**Attention Indicator State (ATTNIND):** This field reports the current state of the Attention Indicator associated with the slot. 00b Reserved 01b On 10b Blink 11b Off
3:2	RO	x	**Power Indicator State (PWRIND):** This field reports the current state of the Power Indicator associated with the slot. 00b Reserved 01b On 10b Blink 11b Off

Bits	Type	Reset	Description
1:0	RO	x	**Slot State (SLOT_STATUS):** This field reports the current state of the slot. 00b Reserved 01b Powered Only 10b Enabled 11b Disabled

3.7.2.2 SEVL – Slot Event Latch Field, Bits [23:16]

The Slot Event Latch field reports all latched events detected by the SHPC.

Bits	Type	Reset	Description
23:21	RO	0	Reserved.
20	RWC	0	**Connected Power Fault Detected (CPFD):** This bit is set when a connected power fault is detected by the power control circuitry for this slot.
19	RWC	0	**MRL Sensor Change Detected (MRLSCD):** This bit is set when the MRL Sensor bit in the Slot Status field changes state indicating a change in the position of the MRL.
18	RWC	0	**Attention Button Press Detected (ABPD):** This bit is set when the Attention Button bit in the Slot Status field transitions from 0 to 1 indicating the Attention Button has been pressed.
17	RWC	0	**Isolated Power Fault Detected (IPFD):** This bit is set when an isolated power fault is detected by the power control circuitry for this slot.
16	RWC	0	**Card Presence Change Detected (CPCD):** This bit is set when a change is detected on the PRSNT1#/PRSNT2# bits defined in the Slot Status field.

3.7.2.3 SSIM – Slot SERR-INT Mask Field, Bits [31:24]

The Slot SERR-INT Mask field controls masking and unmasking of system interrupts and system errors generated from events detected by the SHPC.

Bits	Type	Reset	Description
31	RO	0	Reserved.
30	RW	1	**Connected Power Fault SERR Mask (CPFSM):** If this bit is set, SERR assertions from Connected Power Fault Detected are masked. The state of this bit has no effect on the state of the Connected Power Fault Detected bit. When this bit is clear, then connected power faults can cause ERR_FATAL message on the PCI Express* bus provided the SERR enable bit in the PCICMD register is set or the ERR_FATAL enable bit is set in the PCI Express capability.
29	RW	1	**MRL Sensor SERR Mask (MSSM):** If this bit is set, SERR assertions from MRL Sensor Change Detected are masked. The state of this bit has no effect on the state of the MRL Sensor Change Detected bit. When this bit is clear, then MRL sensor error condition can cause ERR_FATAL message on the PCI Express bus provided the SERR enable bit in the PCICMD register is set or the ERR_FATAL enable bit is set in the PCI Express capability.
28	RW	1	**Connected Power Fault Interrupt Mask (CPFIM):** If this bit is set, system interrupts from Connected Power Fault Detected are masked. The state of this bit has no effect on the state of the Connected Power Fault Detected bit.

Bits	Type	Reset	Description
27	RW	1	**MRL Sensor Interrupt Mask (MSIM):** If this bit is set, system interrupts from MRL Sensor Change Detected are masked. The state of this bit has no effect on the state of the MRL Sensor Change Detected bit.
26	RW	1	**Attention Button Interrupt Mask (ABIM):** If this bit is set, system interrupts from Attention Button Press Detected are masked. The state of this bit has no effect on the state of the Attention Button Press Detected bit.
25	RW	1	**Isolated Power Fault Interrupt Mask (IPFIM):** If this bit is set, system interrupts from Isolated Power Fault Detected are masked. The state of this bit has no effect on the state of the Isolated Power Fault Detected bit.
24	RW	1	**Card Presence Interrupt Mask (CPIM):** If this bit is set, system interrupts from Card Presence Change Detected are masked. The state of this bit has no effect on the state of the Card Presence Change Detected bit.

3.8 I/OxAPIC Interrupt Controller Registers (Function 1)

The Intel® 6702PXH 64-bit PCI Hub contains one I/OxAPIC controller, which reside on the primary bus. The intended use of this controller for the Intel® 6702PXH 64-bit PCI Hub is to have the interrupts from PCI bus A connected to the interrupt controller on Function 1.

3.8.1 PCI Configuration Space Registers

3.8.1.1 Register Summary

Note: Registers that are not shown should be considered Reserved.

Address Offset	Symbol	Register Name	Default	Attribute
00–01h	VID	Vendor ID Register	8086h	RO
02–03h	DID	Device ID Register	0326h (F0)	RO
04–05h	CMD	Command Register	0000h	RO
06–07h	STS	Status Register	0010h	RWO, RO
08h	REVID	Revision ID Register	00h	RO
09–0Bh	CC	Class Code Register	080020h	RO
0Ch	CLS	Cache Line Size Register	00h	RO
0Dh	MLAT	Master Latency Register	00h	RO
0Eh	HEADTYP	Header Type Register	00h	RO
0Fh	BIST	Built-in Self Test Register	00h	RO
10–13h	MBAR	Memory Base Register	00000000h	RW, RO
2C–2Fh	SSID	Subsystem Identifier Register	00000000h	RWOS
34h	CAPP	Capabilities Pointer Register	44h	RWO
40–41h	ABAR	Alternate Base Address Register	0000h	RW, RO
44h	EXP_CAPID	PCI Express* Capability Identifier Register	10h	RO

Address Offset	Symbol	Register Name	Default	Attribute
45h	EXP_NXTP	Next Item Pointer Register	6Ch	RO
46–47h	EXP_CAP	PCI Express Capability Register	0001h	RO
48–4Bh	EXP_DEVCAP	PCI Express Device Capabilities Register	00000001h	RO
4C–4Dh	EXP_DEVCNTL	PCI Express Device Control Register	0020h	RW, RO
4E–4Fh	EXP_DEVSTS	PCI Express Device Status Register	0000h	RWC, RO
50–53h	EXP_LCAP	PCI Express Link Capabilities Register	0003E081h	RO
54–55h	EXP_LCNTL	PCI Express Link Control Register	0000h	RW, RO
56–57h	EXP_LSTS	PCI Express Link Status Register	00x0oh	RO
6Ch	PM_CAPID	Power Management Capability Identifier Register	00x0oh	RO
6Dh	PM_NXTPTR	Power Management Capability Identifier Register	00x0oh	RO
6E–6Fh	PM_CAP	Power Management Next Pointer Register	01h	RO
70–71h	PM_CNTLSTS	Power Management Control and Status Register	00h	RW, RO

80–C0h	Alias of memory space registers at 00h, 10h, 20h, and 40h

3.8.1.2 Offset 00h: VID—Vendor ID Register (D0: F1, F3)

Offset: **00–01h** **Attribute: RO**
Default Value: 8086h **Size: 16 bits**

This register contains the Vendor Identifiers.

Bits	Type	Reset	Description
15:0	RO	8086h	**Vendor ID (VID).** 16-bit field, which indicates that Intel is the vendor. VID=8086

3.8.1.3 Offset 02h: DID—Device ID Register (D0: F1)

Offset: 02–03h **Attribute:** RO
Default Value: 0326h (Function 1) **Size:** 16 bits

This register contains the Device Identifiers.

Bits	Type	Reset	Description
15:0	RO	Function 1: 0326h	**Device ID (DID).** Indicates device number assigned to this controller.

3.8.1.4 Offset 04h: CMD—Command Register (D0: F1, F3)

Offset: 04–05h **Attribute:** RW, RO
Default Value: 0000h **Size:** 16 bits

This register controls how the Intel® 6702PXH 64-bit PCI Hub behaves.

Bits	Type	Reset	Description
15:9	RO	0	Reserved.
8	RW	0	**SERR Enable (SEE):** Controls the enable for the SERR special cycle on the PCI Express* interface. This bit, when set to 1, enables reporting of fatal and non-fatal errors (using ERR_FATAL or ERR_NONFATAL messages on the PCI Express interface) for data parity errors to the I/OxAPIC configuration/memory space. 0 = Disable special cycle. 1 = Enable special cycle. Note that this bit does not affect the setting of the PCI Express error bits in the PCI Express capability registers.
7	RO	0	**Wait Cycle Control (WCC):** Reserved.
6	RW	0	**Parity Error Enable (PAREE):** Enables checking of parity. The I/OxAPIC function uses this bit to report data parity errors it receives on writes.
5	RO	0	**VGA Palette Snoop (VGA_PS):** Does not apply to PCI Express interface. Hardwired to 0.
4	RO	0	**Memory Write and Invalidate (MWI):** Does not apply to PCI Express interface. Hardwired to 0.
3	RO	0	**Special Cycle Enable (SCE):** Does not apply to PCI Express interface. Hardwired to 0.
2	RW	0	**Bus Master Enable (BME):** Controls the I/OxAPIC's ability to act as a master on the PCI Express bus when forwarding system bus interrupt. Note that this bit does not stop the Intel® 6702PXH 64-bit PCI Hub from issuing completions on the PCI Express bus. 0 = Disable. The Intel® 6702PXH 64-bit PCI Hub does not respond to any memory transactions on the PCI interface that target the PCI Express interface. 1 = Enable. Requests other than memory or I/O requests are not controlled by this bit.

Bits	Type	Reset	Description
1	RW	0	**Memory Space Enable (MSE):** Controls the I/OxAPIC's response as a target to memory accesses on the PCI Express interface that address the I/OxAPIC. 0 = These transactions are master aborted on the PCI Express interface. 1 = The Intel® 6702PXH 64-bit PCI Hub is allowed to accept cycles from PCI to be passed to the PCI Express interface.
0	RO	0	**I/O Space Enable (IOSE):** Reserved.

3.8.1.5 Offset 06h: STS—Status Register (D0: F1, F3)

Offset: 06–07h **Attribute:** RO, RWC
Default Value: 0010h **Size:** 16 bits

Establishes the mapping between PCI 2.3 and PCI Express for PCI 2.3 configuration space Status register.

Bits	Type	Reset	Description
15	RWC	0	**Detected Parity Error (DPE):** Indicates that a parity error was detected on cycles targeting the I/OxAPIC.
14	RWC	0	**Signaled System Error (SSE): This bit is set** whenever an ERR_FATAL or ERR_NONFATAL message is sent on a) the PCI Express* bus for data parity errors to APIC config/memory space or b) completor abort signaled by I/OxAPIC and the SERR enable bit (bit 8 in PCICMD) is set. This bit is also set on error messages generated on the PCI Express interface for errors not specific to a function provided the SERR enable bit (bit 8 in PCICMD) is set.
13	RO	0	**Received Master Abort (RMA):** Reserved.
12	RO	0	**Received Target Abort (RTA):** Reserved.
11	RO	0	**Signaled Target Abort (STA):** The I/OxAPIC sets this bit when it signals a completor abort for memory reads that are greater than a DWORD in length
10:9	RO	0	**DEVSEL# Timing (DT):** A value of 0 indicates that fast decode is performed by the I/OxAPIC.
8	RO	0	**Master Data Parity Error (MDPE):** Reserved.
7	RO	0	**Fast Back-to-Back Capable (FBC):** Reserved as not fast back-to-back capable.
6	RO	0	Reserved.
5	RO	0	**66 MHz Capable (C66):** A value of 1 indicates that the I/OxAPIC is 66 MHz capable.
4	RO	1	**Capabilities List Enable (CAPE):** This bit indicates that the Intel® 6702PXH 64-bit PCI Hub contains the capabilities pointer in the I/OxAPIC. Offset 34h indicates the offset for the first entry in the linked list of capabilities.
3:0	RO	0	Reserved.

3.8.1.6 Offset 08h: REVID—Revision ID Register (D0: F1, F3)

Offset: 08h **Attribute:** RO
Default Value: 00h **Size:** 8 bits

Identifies the I/OxAPIC stepping of the Intel® 6702PXH 64-bit PCI Hub.

Bits	Type	Reset	Description
7:0	RO	0	**Revision ID (RID):** Indicates the step of the I/OxAPIC of the Intel® 6702PXH 64-bit PCI Hub. 00h = A0 stepping. 04h = B0 stepping. 08h = C0 stepping.

3.8.1.7 Offset 09h: CC—Class Code Register (D0: F1, F3)

Offset: 09–0Bh **Attribute:** RO
Default Value: 080020h **Size:** 24 bits

This register contains the base class, sub-class and programming interface codes.

Bits	Type	Reset	Description
23:16	RO	08h	**Base Class Code (BCC):** The value of '08h' indicates that this is a generic system peripheral.
15:8	RO	0	**Sub Class Code (SCC):** The value of '00h' indicates that this generic peripheral is an interrupt controller.
7:0	RO	20h	**Programming Interface (PIF):** The value of '20h' indicates that this interrupt peripheral is an I/OxAPIC.

3.8.1.8 Offset 0Ch: CLS—Cache Line Size Register (D0: F1, F3)

Offset: 0Ch **Attribute:** RO
Default Value: 00h **Size:** 8 bits

This register is set by the system BIOS and the OS to equal the system cache line size. However, note that legacy PCI 2.3 software may not always be able to program this field directly, especially in the case of hot plug devices. This field is implemented by PCI Express devices as a read/write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

Bits	Type	Reset	Description
7:0	RO	0	**Cache Line Size (CLS):** Reserved.

3.8.1.9 Offset 0Dh: MLAT—Master Latency Timer Register (D0: F1, F3)

Offset: 0Dh **Attribute:** RO
Default Value: 00h **Size:** 8 bits

This Master Latency Timer register does not apply to PCI Express, and thus it is hardwired to zero by the Intel® 6702PXH 64-bit PCI Hub.

Bits	Type	Reset	Description
7:0	RO	0	**Latency Timer (LAT):** Reserved.

3.8.1.10 Offset 0Eh: HDRTYPE—Header Type Register (D0: F1, F3)

Offset: 0Eh **Attribute:** RO
Default Value: 00h **Size:** 8 bits

Bits	Type	Reset	Description
7:0	RO	0	**Header Type (HDRTYPE):** This indicates that it is a type "00" header (normal PCI device) and that it is part of a multi-function device.

3.8.1.11 Offset 0Fh: BIST—Built-in Self-Test Register (D0: F1, F3)

Offset: 0Fh **Attribute:** RO
Default Value: 00h **Size:** 8 bits

Bits	Type	Reset	Description
7:0	RO	0	**Built-In Self-Test (BIST):** Reserved.

3.8.1.12 Offset 10h: MBAR—Memory Base Register (D0: F1, F3)

Offset: 10–13h **Attribute:** RW, RO
Default Value: 00000000h **Size:** 32 bits

This register contains the I/OxAPIC Base Address for the I/OxAPIC memory space.

Bits	Type	Reset	Description
31:12	RW	0	**Address (ADDR):** These bits determine the base address of the I/OxAPIC.
11:4	RO	0	Reserved.
3	RO	0	**Prefetchable (PF):** A value of 0 indicates that the BAR is not prefetchable.
2:1	RO	0	**Location (LOC):** '00' indicates that the address can be located anywhere in the 32-bit address space.
0	RO	0	**Space Indicator (SI):** Indicates that the BAR is in memory space.

3.8.1.13 Offset 2Ch: SS—Subsystem Identifier Register (D0: F1, F3)

Offset: 2C–2Fh **Attribute:** RWOS
Default Value: 00000000h **Size:** 32 bits

This register is initialized to logic 0 by the assertion of PAPCIRST#. This register can be written only once after PAPCIRST# deassertion.

Bits	Type	Reset	Description
31:16	RWOS	0	**Subsystem ID (SSID):** Write once register for sub-system ID.
15:0	RWOS	0	**Subsystem Vendor ID (SSVID):** Write once register for holding the subsystem vendor ID.

3.8.1.14 Offset 34h: CAPP—Capabilities Pointer Register (D0: F1, F3)

Offset: 34h **Attribute:** RO
Default Value: 44h **Size:** 8 bits

Bits	Type	Reset	Description
7:0	RO	44h	**Capabilities Pointer (CAPP):** Indicates the presence of the PCI Express* capability list item.

3.8.1.15 Offset 40h: ABAR—Alternate Base Address Register (D0: F1, F3)

Offset: 40–41h **Attribute:** RW, RO
Default Value: 0000h **Size:** 16 bits

This register contains an alternate base address in the legacy I/OxAPIC range. This range can co-exist with the BAR register range. This range is needed for Operating Systems that support the legacy I/OxAPIC mapping, but do not yet support remapping the I/OxAPIC anywhere in the 4-Gbyte address space.

Bits	Type	Reset	Description
15	RW	0	**Enable (EN):** When set, the range FECX_YZ00 to FECX_YZFF is enabled as an alternate access method to the I/OxAPIC registers. Bits 'XYZ' are defined below.
14:12	RO	0	Reserved.
11:8	RW	0	**Base Address [19:16] (XBAD):** These bits determine the high order bits of the I/O APIC address map. When a memory address is recognized by the Intel® 6702PXH 64-bit PCI Hub, which matches FECX_YZ00 to FECX_YZFF, the Intel® 6702PXH 64-bit PCI Hub will respond to the cycle and access the internal I/O APIC.
7:4	RW	0	**Base Address [15:12] (YBAD):** These bits determine the low order bits of the I/O APIC address map. When a memory address is recognized by the Intel® 6702PXH 64-bit PCI Hub, which matches FECX_YZ00 to FECX_YZFF, the Intel® 6702PXH 64-bit PCI Hub will respond to the cycle and access the internal I/O APIC.
3:0	RW	0	**Base Address [11:8] (ZBAD):** These bits determine the low order bits of the I/O APIC address map. When a memory address is recognized by the Intel® 6702PXH 64-bit PCI Hub, which matches FECX_YZ00 to FECX_YZFF, the Intel® 6702PXH 64-bit PCI Hub will respond to the cycle and access the internal I/O APIC.

3.8.1.16 Offset 44h: EXP_CAPID—PCI Express Capability Identifier Register (D0: F1, F3)

Offset: 44h **Attribute:** RO
Default Value: 10h **Size:** 8 bits

Bits	Type	Reset	Description
7:0	RO	10h	**PCI Express* Capability ID (PECID):** Indicates PCI Express capability.

3.8.1.17 Offset 45h: EXP_NXTP—PCI Express Next Pointer Register (D0: F1, F3)

Offset: 45h **Attribute:** RO
Default Value: 6Ch **Size:** 8 bits

Bits	Type	Reset	Description
7:0	RO	6Ch	**Next Pointer (MNPTR):** Points to the next capabilities list pointer, which is the Power Management Capability Identifier Register.

3.8.1.18 Offset 46: EXP_CAP—PCI Express Capability Register (D0: F1, F3)

Offset: 46 - 47h **Attribute:** RO
Default Value: 0001h **Size:** 16 bits

This register carries the version number of the capability item and other base information contained in the PCI Express capability structure.

Bits	Type	Reset	Description
15:14	RO	0	Reserved.
13:9	RO	0	**Interrupt Message Number (IMN):** Not relevant for I/OxAPIC.
8	RO	0	**Slot Implemented (SLOTI):** Not relevant for I/OxAPIC.
7:4	RO	0	**Device/Port Type (DPT):** Indicated PCI Express* end-point device.
3:0	RO	01h	**Version Number (VN):** Indicates PCI Express capability structure version number.

3.8.1.19 Offset 48h: EXP_DCAP—PCI Express Device Capability Register (D0: F1, F3)

Offset: 48 – 4Bh **Attribute:** RO
Default Value: 00000001h **Size:** 32 bits

This register identifies PCI Express device specific capabilities.

Bits	Type	Reset	Description
31:28	RO	0	Reserved.
27:26	RO	0	**Captured Slot Power Limit Scale (CSPLS):** Specifies the scale used for the Slot Power Limit Value. Range of Values: 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x This value is set by the Set_Slot_Power_Limit message. In combination with the Slot Power Limit value, specifies the upper limit on power supplied by slot. Power limit (in Watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Value field.
25:18	RO	0	**Captured Slot Power Limit Value (CSPLV):** In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. This value is set by the Set_Slot_Power_Limit message.
17:12	RO	0	Reserved.
11:9	RO	0	**Endpoint L1s Acceptable Latency (EL1AL):** The Intel® 6702PXH 64-bit PCI Hub does not support L1 Link State Power Management (LSPM).
8:6	RO	0	**Endpoint L0s Acceptable Latency (EL0AL):** The Intel® 6702PXH 64-bit PCI Hub wants the least latency possible out of L0s
5	RO	0	**Extended Tag Field Supported (ETFS):** The Intel® 6702PXH 64-bit PCI Hub supports only a 5-bit tag.
4:3	RO	0	**Phantom Functions Supported (PFS):** The Intel® 6702PXH 64-bit PCI Hub does not support phantom functions.
2:0	RO	001b	**Max_ Payload_Size Supported (MPSS):** This field is set to a value of 001b, signifying that the Intel® 6702PXH 64-bit PCI Hub supports a maximum payload size of 256 byte packets.

3.8.1.20 Offset 4Ch: DEVCNTL—Device Control Register (D0: F1, F3)

Offset: 4C – 4Dh **Attribute:** RW; RO
Default Value: 0020h **Size:** 16 bits

This register controls PCI Express device specific (Intel® 6702PXH 64-bit PCI Hub) parameters.

Bits	Type	Reset	Description
15	RO	0	Reserved.
14:12	RO	0	**Max_Read_Request_Size (MRRS):** Does not apply to the I/OxAPIC.
11	R0	0	**Enable No Snoop (ENS):** This does not apply to the Intel® 6702PXH 64-bit PCI Hub since it does not set the NS bit on MSI Transactions it generates.
10	R0	0	**Auxiliary (AUX) Power PM Enable (AUXPPME):** The Intel® 6702PXH 64-bit PCI Hub ignores this bit since it does not support auxiliary power.
9	RO	0	**Phantom Function Enable (PFE):** The Intel® 6702PXH 64-bit PCI Hub ignores this bit since it does not support phantom functions.
8	RO	0	**Extended Tag Field Enable (ETFE):** The Intel® 6702PXH 64-bit PCI Hub ignores this bit since it supports only 5-bit tag.
7:5	RW	001b	**Max_ Payload_Size (MPS):** Does not affect the I/OxAPIC since it does not do writes greater than a DWORD.
4	RO	0	**Enable Relaxed Ordering (ERO):** Not applicable or used by the I/OxAPIC.
3	RW	0	**Unsupported Request Reporting Enable (URRE):** This bit enables reporting of Unsupported Requests when set to a 1. It is used by the I/OxAPIC to enable reporting of ERR_FATAL or ERR_NONFATAL messages on the PCI Express interface for reporting Unsupported Requests errors, such as data parity errors on writes to the I/OxAPIC (configuration or memory space). Refer to Section 6.2 of the *PCI Express Base Specification*, Revision 1.0a for further details.
2	RW	0	**Report Fatal Errors:** Used to gate the generation of ERR_FATAL message on Fatal link errors. Refer to the *PCI Express Base Specification*, Revision 1.0a for information on how this bit is used to report fatal errors in the context of multi-function devices like the Intel® 6702PXH 64-bit PCI Hub. This bit is not used by the APIC per se.
1	RW	0	**Non-Fatal Error Reporting Enable (NFERE):** This bit controls reporting of non-fatal errors. Used by I/OxAPIC to gate the generation of the ERR_NONFATAL message on data parity errors to it. 0 = Disable. 1 = Intel® 6702PXH 64-bit PCI Hub will report non-fatal errors. Refer to Section 6.2 of the *PCI Express Base Specification*, Revision 1.0a for further details.
0	RW	0	**Correctable Error Reporting Enable (CERE):** This bit controls reporting of correctable errors. When set to “1”, the Intel® 6702PXH 64-bit PCI Hub is enabled to generate ERR_CORR message on the PCI Express bus. Not used by I/OxAPIC in normal operation. 0 = Disable. 1 = Intel® 6702PXH 64-bit PCI Hub will report correctable errors.

3.8.1.21 Offset 4Eh: DSTS—Device Status Register (D0: F1, F3)

Offset: 4E-4Fh **Attribute:** RWC, RO
Default Value: 0000h **Size:** 16 bits

This register provides information on specific parameters of a PCI Express device, in this case the Intel® 6702PXH 64-bit PCI Hub.

Bits	Type	Reset	Description
15:6	RO	0	Reserved.
5	RO	0	**Transactions Pending (TP):** Not relevant for I/OxAPIC, since it does not generate non-posted requests.
4	RO	0	**Aux Power Detected (AUXPD):** Intel® 6702PXH 64-bit PCI Hub does not support aux power and hence this bit is reserved for the Intel® 6702PXH 64-bit PCI Hub.
3	RWC	0	**Unsupported Request Detected (URD):** This bit indicates that the Intel® 6702PXH 64-bit PCI Hub received an Unsupported request. The I/OxAPIC will set this bit whenever it receives a configuration or memory write with bad parity. It is also set on link unsupported request errors that are not specific to any function within the Intel® 6702PXH 64-bit PCI Hub.
2	RWC	0	**Fatal Error Detected (FED):** The I/OxAPIC does not set this bit on its own, but rather it is set on link fatal errors.
1	RWC	0	**Non-Fatal Error Detected (NFED):** The I/OxAPIC sets this bit whenever it detects a write to I/OxAPIC (configuration or memory space) with bad data parity. This bit is also set on link uncorrectable errors that are not specific to any functions within the Intel® 6702PXH 64-bit PCI Hub.
0	RWC	0	**Correctable Error Detected (CED):** The I/OxAPIC does not set this bit on its own, but rather it is set on link correctable errors.

3.8.1.22 Offset 50h: LCAP—Link Capabilities Register (D0:F1, F3)

Offset: 50-53h **Attribute:** RO
Default Value: 0003E081h **Size:** 32 bits

This register identifies PCI Express link specific capabilities of the Intel® 6702PXH 64-bit PCI Hub.

Bits	Type	Reset	Description
31:24	RO	0	**Port Number (PNUM):** Not applicable to the Intel® 6702PXH 64-bit PCI Hub and reserved to zero.
23:18	RO	0	Reserved.
17:15	RO	111b	**L1 Exit Latency (L1XL):** L1 transition is not supported by the Intel® 6702PXH 64-bit PCI Hub.

Bits	Type	Reset	Description
14:12	RO	6h	**L0 Exit Latency (L0XL): L0s Exit Latency:** The value in these bits is influenced by the PCI reference clock configuration in the Intel® 6702PXH 64-bit PCI Hub, since the reference clock is configured as a common clock. Because it is a common clock configuration, the Common Clock Configuration bit (CCC, bit 6) in the Link Control register (LCTL, offset 54h) is set to a 1. The mapping is shown below: Bit 6 PCI Express Link Control Link Capabilities Bits 14:12 0 110b = 2-4 µs. 1 010b - 128 ms to less than 256 ms Note that software could write the bit 6 in link control register to either a 1 or 0, and these bits should change accordingly.
11:10	RO	0	**Active State Link PM Support (ASLPMS):** Indicates the level of active state power management supported on the given PCI Express link. The PCI-SIG defined encodings are as follows: 00 L0s entry disabled. 01 Intel® 6702PXH 64-bit PCI Hub enters L0s per the specified requirements for L0s entry. 10 L0s entry disabled. 11 L0s entry disabled. The Intel® 6702PXH 64-bit PCI Hub supports only L0s, so this field is set to 01h. Not used by I/OxAPIC in normal operation.
9:4	RO	8h	**Maximum Link Width (MLW):** Intel® 6702PXH 64-bit PCI Hub supports a maximum PCI Express link width of x8, so this field is set to the PCI-SIG defined value for x8, which is 001000 b, or 8h.
3:0	RO	0001b	**Maximum Link Speed (MLS):** Intel® 6702PXH 64-bit PCI Hub supports a PCI Express link speed of 2.5 Gbps only, so this field is set to the PCI-SIG defined value for 2.5 Gbps, which is 0001b, or 1h.

3.8.1.23 Offset 54h: LCTL—Link Control Register (D0:F1, F3)

Offset: 54-55h **Attribute:** RW; RO
Default Value: 0000h **Size:** 16 bits

This register controls PCI Express link specific parameters.

Bits	Type	Reset	Description
15:7	RO	0	Reserved.

Bits	Type	Reset	Description
6	RW	0	**Common Clock Configuration (CCC):** This bit when set indicates that Intel® 6702PXH 64-bit PCI Hub and the component it is connected to via the PCI Express link (located at the opposite end of this link) are operating with a distributed common reference clock. A value of 0 indicates that this component and the component at the opposite end of this Link are operating with an asynchronous reference clock. 0 = Intel® 6702PXH 64-bit PCI Hub and the other PCI Express component have an asynchronous reference clock 1 = Intel® 6702PXH 64-bit PCI Hub and the other PCI Express component share a common clock Note that this bit is used to reflect the proper L0s exit latency value in the EXP_LSTS register.
5:4	RO	0	Reserved.
3	RO	0	**Read Request Return Parameter Control (RRRPC):** Not used by the I/OxAPIC.
2	RO	0	Reserved.
1:0	RW	0	**Active State Link PM Control (ASLPMC):** Controls the level of active state Power Management supported on the given PCI Express link. The PCI-SIG defined encodings are as follows: 00b Disabled 01b L0s entry supported 10b Reserved 11b L0s and L1s entry supported These bits enable Intel® 6702PXH 64-bit PCI Hub to enter L0s. Not used by I/OxAPIC in normal operation.

3.8.1.24 Offset 56h LSTS—Link Status Register (D0:F1, F3)

Offset: **56-57h** **Attribute:** **RO**
Default Value: **0001h (X4 Link)** **Size:** **16 bits**
0041h (X4 Link)
0081h (X8 Link)

This register provides information about PCI Express link specific parameters.

Bits	Type	Reset	Description
15:10	RO	0	Reserved.
9:4	RO	0h, 4h, or 8h	**Negotiated Link Width (NLW):** Indicates the negotiated width of PCI Express* Link. Defined encodings are: 000000b X1 width 000100b X4 width 001000b X8 width
3:0	RO	1h	**Link Speed (LS):** Intel® 6702PXH 64-bit PCI Hub supports a PCI Express link speed of 2.5 Gbps only, so this field is set to the PCI-SIG defined value for 2.5 Gbps, which is 0001b, or 1h.

3.8.1.25 Offset 6Ch: PM_CAPID – Power Management Capability Identifier Register (D0:F1, F3)

Offset: 6Ch **Attribute:** RO
Default Value: 00h **Size:** 8 bits

This register provides information about PCI Express link specific parameters.

Bits	Type	Reset	Description
7:0	RO	01h	**Capability ID (CAP_ID):** Capability ID indicates PCI compatible Power Management.

3.8.1.26 Offset 6Dh: PM_NXTPTR – Power Management Next Pointer

Offset: 6Dh **Attribute:** RO
Default Value: 00h **Size:** 8 bits

This register provides information about PCI Express link specific parameters.

Bits	Type	Reset	Description
7:0	RO	0	**Next Pointer (NXTPTR):** Next Pointer if non-zero.

3.8.1.27 Offset 6Eh: PM_CAP – Power Management Capabilities Register (D0: F1, F3)

Offset: 6Eh **Attribute:** RO
Default Value: 0002h **Size:** 16 bits

Bits	Type	Reset	Description
15:3	RO	0	Reserved.
2:0	RO	10b	**Version (VERS):** I/OxAPIC Power Management implementation is compliant with the *PCI PM Specification*, Revision 1.1.

3.8.1.28 Offset 70h: PM_CNTLSTS – Power Management Control and Status Register (D0: F1, F3)

Offset: 70h **Attribute:** RW, RO
Default Value: 0000h **Size:** 16 bits

This register provides information about PCI Express link specific parameters.

Bits	Type	Reset	Description
15:2	RO	0	Reserved.
1:0	RW	0	**PowerState (PWR_ST):** This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The I/OxAPIC supported field values are given below. 00b – **D0** 01b – Reserved 10b – Reserved 11b – **D3**$_{hot}$ If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs. When in **D3**hot state, the I/OxAPIC responds to configuration transactions only and a transition from **D3**hot to **D0** does not reset the I/OxAPIC's registers. Also, in **D3**hot state, the I/OxAPIC cannot generate any MSI. Virtual wire interrupts generated by the I/OxAPIC on behalf of PCI agents/SHPC are not masked by the **D3**hot state.

3.8.2 I/OxAPIC Direct Memory Space Registers

3.8.2.1 Register Summary

Offset Address	Symbol	Full Name	Default	Attribute
00h	IDX	Index Register	00h	RW
10–13h	WND	Window Register	00000000h	RW
20h	PAR	IRQ Pin Assertion Register	000000xxh	RW, RO
40h	EOI	EOI Register	xxh	WO

3.8.2.2 Offset 00h: IDX—Index Register

Offset: 00h **Attribute:** RW
Default Value: 00h **Size:** 8 bits

The Index Register will select which indirect register appears in the window register to be manipulated by software. Software will program this register to select the desired I/OxAPIC internal register.

Bits	Type	Reset	Description
7:0	RW	0	**Index (IDX):** Indirect register to access.

3.8.2.3 Offset 10h: WND—Window Register

Offset: 10–13h **Attribute:** RW
Default Value: 00000000h **Size:** 32 bits

This is a 32-bit register specifying the data to be read or written to the register pointed to by the Register Select register. This register can be accessed in byte quantities.

Bits	Type	Reset	Description
31:0	RW	0	**Window (WND):** Data to be written to the indirect register on writes, and location of register data from the indirect register on reads.

3.8.2.4 Offset 20h: PAR—IRQ Pin Assertion Register

Offset: 20h **Attribute:** RW, RO
Default Value: 000000xxh **Size:** 32 bits

The IRQ Pin Assertion Register is present to provide a mechanism to scale the number of interrupt inputs into the I/Ox APIC without increasing the number of dedicated input pins. When a device that supports this interrupt assertion protocol requires interrupt service, that device will issue a write to this register. Bits [4:0] written to this register contain the IRQ number for this interrupt. The only valid values are 0–23.

Bits	Type	Reset	Description
31:5	RO	0	Reserved.
4:0	RW	xx	**Assertion (PAR):** Virtual pin to be asserted (active high). Writes to this register are treated with edge triggered semantics regardless of what is programmed in the RDL DWord, though the interrupt message is generated directly from the contents of the RDL and RDH DWords.

3.8.2.5 Offset 40h: EOI—End of Interrupt (EOI) Register

Offset: 40h **Attribute:** WO
Default Value: xxh **Size:** 8 bits

The EOI register is present to provide a mechanism to maintain the level triggered semantics for level-triggered interrupts issued on the parallel bus.

When a write is issued to this register, the I/OxAPIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit for that I/O Redirection Entry is cleared.

Note that if multiple I/O Redirection entries, for any reason, assign the same vector for more than one interrupt input, each of those entries will have the Remote_IRR bit reset to ‘0’.

Bits	Type	Reset	Description
7:0	WO	xxh	**End of Interrupt (EOI):** Vector to be cleared by the EOI.

3.8.3 Indirect Memory Space Registers

3.8.3.1 Register Summary

To access the indirect memory space, an 8-bit value must be written to the index register, which is a “pointer” (indirect) to a 32-bit memory location. The 32-bit value in the Window Register can then be read.

Table 3-4. Indirect Memory Space Registers Summary

Address Offset	Symbol	Full Name	Default	Attribute
00h	ID	APIC ID Register	00000000h	RW, RO
01h	VS	Version Register	00178020h	RO
03h	BCFG	Boot Configuration Register	00000001h	RW, RO
10h	RDL[0]	Redirection Table Low DWord 0 Register	00010000h	RW, RO
11h	RDH[0]	Redirection Table High DWord 0 Register	00000000h	RW, RO
3E	RDL[23]	Redirection Table Low DWord 23 Register	00010000h	RW, RO
3F	RDH[23]	Redirection Table High DWord 23 Register	00000000h	RW, RO
40–FF	Reserved	Reserved.	00000000h	RO

3.8.3.2 Offset 00h: ID—APIC ID Register

Offset: 00h **Attribute:** RW, RO
Default Value: 00000000h **Size:** 32 bits

The APIC ID serves as a physical name of the APIC. The APIC bus arbitration ID for the APIC is derived from its I/OxAPIC ID. This register is reset to zero on power up reset.

Bits	Type	Reset	Description
31:28	RO	0	Reserved.
27:24	RW	0	**I/OxAPIC ID (APICID):** Software must program this value before using the I/OxAPIC.
23:0	RO	0	Reserved.

3.8.3.3 Offset 01h: VS—Version Register

Offset: 01h **Attribute:** RO
Default Value: 00178020h **Size:** 32 bits

Contains information related to this I/OxAPIC for driver/ OS/software.

Bits	Type	Reset	Description
31:24	RO	0	Reserved.
23:16	RO	17h	**Maximum Redirection Entries (MAX):** This is the entry number of the highest entry in the redirection table. It is equal to the number of interrupt inputs minus one. This field is hardwired to 17h to indicate 24 interrupts.

Bits	Type	Reset	Description
15	RO	1	**IRQ Assertion Register Supported (PRQ):** This bit is set to 1 to indicate that this version of the I/OxAPIC implements the IRQ Assertion register and allows PCI devices to write to it to cause interrupts.
14:8	RO	0	Reserved.
7:0	RO	20h	**Version (VS):** This identifies the implementation version. This field is hardwired to "20h" to indicate this is an I/OxAPIC.

3.8.3.4 Offset 02h: ARBID—Arbitration ID Register

Offset: 02h **Attribute:** RO
Default Value: 0000h **Size:** 32 bits

This register contains the APIC serial bus arbitration priority for the APIC, and is loaded whenever the APIC ID register is loaded. The Intel® 6702PXH 64-bit PCI Hub does not support APIC bus serial delivery and hence this register is never used.

Bits	Type	Reset	Description
31:28	RO	0	Reserved.
27:24	RO	0	**Arbitration ID (ARBID):** Reflects the I/OxAPIC Arbitration ID.
23:0	RO	0	Reserved.

3.8.3.5 Offset 03h: BCFG—Boot Configuration Register

Offset: 03h **Attribute:** RW, RO
Default Value: 00000000h **Size:** 32 bits

The Boot Configuration contains information that is only supposed to be accessed by BIOS and is not for OS use. It contains bits that must be programmed before the OS takes control of interrupts.

Bits	Type	Reset	Description
31:1	RO	0	Reserved.
0	RW	1	**Delivery Type (DT):** Software sets this bit to 1 to indicate that the delivery mechanism is as a system bus message and not the I/OxAPIC serial bus.

3.8.3.6 Offset 10h, 12h,…, 3Eh: RDL—Redirection Table Low DWord Register

Offset: 10h,12h,..,3Eh **Attribute:** RW, RO
Default Value: 00010000h **Size:** 32 bits

The information in this register is sent on the system bus to address a local APIC. There is one of these registers for every interrupt. The 1st interrupt (pin 0) has this entry at offset 10h. The 2nd interrupt at 12h, 3rd at 14h, etc., until the final interrupt (interrupt 23) at 3Eh.

Bits	Type	Reset	Description
31:18	RO	0	Reserved.
17	RW	0	**Disable Flushing Bit (DFLUSH):** This bit is maintained for any potential software compatibility, but the Intel® 6702PXH 64-bit PCI Hub will perform no flushing action, regardless of the setting of this bit.

Bits	Type	Reset	Description
16	RW	1	**Mask (MSK):** 0 = An edge or level on this interrupt pin results in the delivery of the interrupt to the destination. 1 = Interrupts are not delivered nor held pending. Setting this bit after the interrupt is accepted by a local APIC has no effect on that interrupt.
15	RW	0	**Trigger Mode (TM):** This field indicates the type of signal on the interrupt pin that triggers an interrupt. 0 = Edge sensitive. 1 = Level sensitive.
14	RO	0	**Remote IRR (RIRR):** This bit is used for level-triggered interrupts; its meaning is undefined for edge triggered interrupts. 0 = EOI message is received from a local APIC. 1 = For level triggered interrupts, this bit is set when Local APICs accept the level interrupt sent by the I/OxAPIC. It is reset when an EOI message is received from a local APIC.
13	RW	0	**Interrupt Input Pin Polarity (IP):** This bit specifies the polarity of each interrupt signal connected to the interrupt pins. 0 = Active high. 1 = Active low.
12	RO	0	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. It is read only. Writes to this bit have no effect. 0 = Idle; no activity for this interrupt. 1 = Pending - interrupt has been injected, but delivery is held up due the inability of the receiving APIC unit to accept the interrupt at this time.
11	RW	0	**Destination Mode (DSTM):** This field determines the interpretation of the Destination field. 0 = Physical; Destination APIC ID is identified by RDH bits [59:56]. 1 = Logical; Destination is identified by matching bits [63:56] with the Logical Destination in the Destination Format Register and Logical Destination Register in each local APIC.
10:8	RW	0	**Delivery Mode (DELM):** This field specifies how the APICs listed in the destination field should act upon reception of the interrupt. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are described in more detail in each serial message. The encodings are: 000 = Fixed: Trigger Mode can be edge or level. 001 = Lowest Priority: Trigger Mode can be edge or level. 010 = SMI/PMI: Not supported. 011 = Reserved. 100 = NMI: Not supported. 101 = INIT: Not supported. 110 = Reserved. 111 = ExtINT: Not supported.
7:0	RW	0	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

3.8.3.7 Offset 11h, 13h,…, 3Fh: RDH—Redirection Table High Register

Offset: 11h,13h,..,3Fh **Attribute:** RW, RO
Default Value: 00000000h **Size:** 32 bits

The information in this register is sent on the system bus to address a local APIC. There is one of these registers for every interrupt. The 1st interrupt (pin 0) has this entry at offset 11h. The 2nd interrupt at 13h, 3rd at 15h, etc., until the final interrupt (interrupt 23) at 3Fh.

Bits	Type	Reset	Description
31:24	RW	0	**Destination ID (DID):** This information is transferred in bits [19:12] of the address.
23:16	RW	0	**Extended Destination ID (EDID):** These bits are sent to a local APIC in system bus delivery mode. These are bits [11:4] of the address.
15:0	RO	0	Reserved.

§

4 Electrical Characteristics

4.1 DC Voltage and Current Specifications

4.1.1 VCC15 and VCC33 Voltage Requirements

The Intel® 6702PXH 64-bit PCI Hub requires that the VCC33 voltage rail be no less than 0.5V below VCC15 (absolute voltage value) at all times during Intel® 6702PXH 64-bit PCI Hub operation, including during system power up and power down. In other words, the following must always be true:

VCC33 ≥ (VCC15 - 0.5V)

This can be accomplished by placing a diode (with a voltage drop < 0.5V) between VCC15 and VCC33. Anode will be connected to VCC15 and cathode will be connected to VCC33.

If VCC15 (1.5V PCI-X I/O voltage) and VCC (1.5V core voltage) are tied together on the platform, then both voltages must meet the above rule.

If VCC33 voltage rail is powered before the VCC15 rail, then there may be a maximum of 525ms delay between the two voltage ramps. In the special case where a voltage regulator solution is used which shunts VCC15 to ground while VCC33 is powered, the maximum allowable time that VCC15 can be shunted to ground while VCC33 is fully ramped is 20ms. If VCC15 and VCC are tied together on the platform and VCC and/or VCC15 are shunted to ground while VCC33 is powered, the maximum time that VCC and/or VCC15 can be shunted to GND while VCC33 is fully ramped is 20ms.

4.1.2 VCCEXP and EXP_CLK_N/EXP_CLK_P

All Intel® 6702PXH 64-bit PCI Hub voltage rails must be stable and within their operating ranges before the PCI Express differential clocks EXP_CLK_N and EXP_CLK_P begin running. This is a requirement for all devices with PCI Express interfaces.

4.1.3 Intel® 6702PXH 64-bit PCI Hub DC Specifications

Table 4-1. Intel® 6702PXH 64-bit PCI Hub DC and AC Voltage Specifications

Symbol	Parameter	Minimum		Nominal	Maximum		Unit	Notes
		AC	DC		AC	DC		
VCC	Intel® 6702PXH 64-bit PCI Hub Core	1.425	1.455	1.5	1.575	1.545	V	1, 3
VCCAEXP	Analog PCI Express* Voltage	1.455		1.5	1.545		V	
VCCAPCI[2:0]	Analog PCI Voltages	1.455		1.5	1.545		V	
VCCBGEXP	Analog Bandgap Voltage	-10mV	2.425	2.5	+10mV	2.575	V	4,5
VCCEXP	PCI Express Interface Voltage	1.425	1.455	1.5	1.575	1.545	V	1, 2, 3, 5
VCC15	1.5V I/O Voltage	1.425	1.455	1.5	1.575	1.545	V	1, 3
VCC33	PCI/PCI-X Mode 1 Bus Interface Voltage	3.0		3.3	3.6		V	
VREFPCI	Analog Reference Voltage to PCI	0.728		0.75	0.773		V	6
Intel® 6702PXH 64-bit PCI Hub P_{TDP}	Intel® 6702PXH 64-bit PCI Hub Thermal Design Power				10.20		W	

NOTES:
1. Under no circumstances may the 1.5V supply voltage go past the AC min/max window. the 1.5V supply voltage window may go outside the DC min/max window for transient events.
2. Note that the VCCEXP balls on the Intel® 6702PXH 64-bit PCI Hub should be inductively isolated from the VCC balls to avoid potential noise injection from the core onto the VCCEXP rail, which is particularly sensitive to AC noise. Refer to the appropriate Intel® 6702PXH 64-bit PCI Hub sections of the associated Platform Design Guide for suggestions on how to achieve this isolation.
3. DC specification applies to conditions at frequencies below 5MHz. AC specification applies to transient conditions at frequencies above 5MHz.
4. The VCCBGEXP rail can tolerate no more than +/- 10mV AC noise about the DC voltage, which must be fixed within the DC limits shown.
5. The analog voltages are intended to be a filtered copy of the associated supply voltage. Refer to the Intel® 6702PXH 64-bit PCI Hub sections of the associated Platform Design Guide for reference implementation of the filter and the filter response curve.

Table 4-2 and Table 4-3 apply only to the Intel® 6702PXH 64-bit PCI Hub, except where noted to also apply to the Intel® 6702PXH 64-bit PCI Hub.

Table 4-2. ntel® 6702PXH 64-bit PCI Hub DC Current Specifications

Voltage Plane Current, Amps	133/x	133/133		100/100		66/x	66/66	
number of slots (segment A/B)	1/0[1]	1/1	1/2	2/2	2/0[1]	4/01	1/1	4/4
$I_{VCC(max)}$	1.68	2.16	2.16	2.03	1.61	1.55	1.9	1.9
IVCC15(max)	0.22	0.22	0.22	0.22	0.22	0.22	0.22	0.23
IVCEXP(max)	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
IVCC33	1.05	1.45	1.61	1.62	1.14	1.22	1.28	1.79

NOTE:
1. Also applies to Intel® 6702PXH 64-bit PCI Hub

Table 4-3. Intel® 6702PXH 64-bit PCI Hub Thermal Current, Amps (nominal)

Thermal Current, Amps (nominal)	133/x	133/133		100/100		66/x	66/66	
number of slots (segment A/B)	1/0	1/1	1/2	2/2	2/0	4/0	1/1	4/4
$I_{VCC(max)}$	1.24	1.64	1.64	1.52	1.18	1.11	1.4	1.4
IVCC15(max)	0.22	0.22	0.22	0.22	0.22	0.22	0.22	0.23
IVCEXP(max)	0.69	0.69	0.69	0.69	0.69	0.69	0.69	0.69
IVCC33	0.99	1.3	1.39	1.41	1.04	1.1	1.19	1.52

4.1.4 Input Characteristic Signal Association

Table 4-4. DC Characteristics Input Signal Association

Symbol	Signals
V_{IH1}/V_{IL1}	**Interrupt Signals:** PAIRQ_[15:0]#, PBIRQ_[15:0]# **PCI Signals:** PAAD[63:0], PBAD[63:0], PACBE_[7:0]#, PBCBE_[7:0]#, PAPAR, PBPAR, PADEVSEL#, PBDEVSEL#, PAFRAME#, PBFRAME#, PAIRDY#, PBIRDY#, PATRDY#, PBTRDY#, PASTOP#, PBSTOP#, PAPERR#, PBPERR#, PASERR#, PBSERR#, PAREQ_[5:0]#, PBREQ_[5:0]#, PAM66EN, PBM66EN, PA133EN, PB133EN, PAPCIXCAP, PBPCIXCAP, PAPAR64, PBPAR64, PAREQ64#, PBREQ64#, PAACK64#, PBACK64# **Hot plug Signals:** HPA_SID, HPB_SID, HPA_SLOT[3:0], HPB_SLOT[3:0] **Intel® 6702PXH 64-bit PCI Hub Clock Signals (3.3V Only):** PACLKI, PBCLKI **Miscellaneous Signals:** PWROK, RSTIN#
V_{IH2}/V_{IL2}	**PCI Express* Signals**: EXP_CLK, EXP_CLK#, EXP_TXP[7:0], EXP_TXN[7:0], EXP_COMP[1:0]
V_{IH3}/V_{IL3}	**SMB Signals:** SDTA, SCLK

4.1.5 DC Input Characteristics

Table 4-5. DC Input Characteristics

Symbol	Parameter	PCI		PCI-X		Unit
		Min	Max	Min	Max	
V_{IL1}	Input Low Voltage	-0.5	0.3VCC33	-0.5	0.35VCC33	V
V_{IH1}	Input High Voltage	0.5VCC33	VCC33 +0.5	0.5VCC33	VCC33 +0.5	V
Symbol	**Parameter**	**Max**		**Max**		
V_{IL2}	Input Low Voltage	N/A		N/A		V
V_{IH2}	Input High Voltage	N/A		N/A		V
V_{IL3}	Input Low Voltage	0.8		0.8		V
V_{IH3}	Input High Voltage	VCC33 + 0.5		VCC33 + 0.5		V

4.1.6 DC Characteristic Output Signal Association

Table 4-6. DC Characteristic Output Signal Association

Symbol	Signals
V_{OH1}/V_{OL1}	**PCI Signals**: PAAD[63:0], PBAD[63:0], PACBE_[7:0]#, PBCBE_[7:0]#, PAPAR, PBPAR, PADEVSEL#, PBDEVSEL#, PAFRAME#, PBFRAME#, PAIRDY#, PBIRDY#, PATRDY#, PBTRDY#, PASTOP#, PBSTOP#, PAPERR#, PBPERR#, PAM66EN, PBM66EN, PAGNT_[6:0]#, PBGNT_[5:0]#, PAPLOCK#, PBPLOCK#, PAPAR64, PBPAR64, PAREQ64#, PBREQ64#, PAACK64#, PBACK64# **PCI Clock Signals (3.3V Only):** PAPCLKO[6:0], PBPCLKO[6:0], PAPCIRST#, PBPCIRST# **Hot-Plug Signals**: HPA_SIC, HPB_SIC, HPA_SIL#, HPB_SIL#, HPA_SOR#, HPB_SOR#, HPA_SORR#, HPB_SORR#, HPA_SOC, HPB_SOC, HPA_SOL, HPB_SOL, HPA_SOLR, HPB_SOLR, HPA_SOD, HPB_SOD **Miscellaneous Signals**:
V_{OH2}/V_{OL2}	**PCI Express* Signals:** EXP_RXP[7:0], EXP_RXN[7:0]
V_{OH3}/V_{OL3}	**SMBus Signals:** SDTA, SCLK

4.1.7 DC Output Characteristics

Table 4-7. DC Output Characteristic (Sheet 1 of 2)

Symbol	Parameter	3.3V Signal		Unit	Notes
		Min	Max		
V_{OL1}	Output Low Voltage		0.1VCC33	V	(5V) Iout = 6 mA (3.3V) Iout = 1500 µA
V_{OH1}	Output High Voltage	0.9VCC33		V	(5V) Iout = -2 mA (3.3V) Iout = -500 µA
V_{OL2}	Output Low Voltage	N/A		V	

Table 4-7. DC Output Characteristic (Sheet 2 of 2)

Symbol	Parameter	3.3V Signal		Unit	Notes
		Min	Max		
V_{OH2}	Output High Voltage	N/A		V	
V_{OL3}	Output Low Voltage	0.4		V	I_{OL4}=14 mA
V_{OH3}	Output High Voltage	N/A		V	Open Drain

4.1.7.1 PCI Express Interface DC Specifications

4.1.7.1.1 Differential Transmitter (TX) DC Output Specifications

Table 4-8 defines the DC specifications of parameters for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 4-8. Differential Transmitter (TX) DC Output Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{TX-DIFFp-p}$	Differential Peak to Peak Output Voltage	0.800		1.2	V	$V_{TX-DIFFp-p}$ = 2*|V_{TX-D+}-V_{TX-D-}| See Note 1.
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB	This is the ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition See Note 1.
$V_{TX-CM-ACp}$	AC Peak Common Mode Output Voltage			20	mV	$V_{TX-CM-ACp}$ = |V_{TX-D+} + v_{TX-D-}| / 2 – $v_{TX-CM-DC}$ $v_{TX-CM-DC}$ = $DC_{(avg)}$ of |V_{TX-D+} + V_{TX-D-}| / 2 See Note 1.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0		100	mV	|$V_{TX-CM-DC}$– $V_{TX-CM-Idle-DC[During Electrical Idle]}$| =100mv $V_{TX-CM-DC}$ = $DC_{(avg)}$ of |V_{TX-D+} + V_{TX-D-}| / 2 [Electrical Idle] See Note 1.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-.	0		25	mV	|$V_{TX-CM-DC-D+}$– $V_{TX-CM-DC-D-}$| = 25mV $V_{TX-CM-DC-D+}$ = $DC_{(avg)}$ of |V_{TX-D+}| $V_{TX-CM-DC-D-}$ = $DC_{(avg)}$ of |V_{TX-D-}| See Note 1.
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0		20	mV	$V_{TX-IDLE-DIFFp}$ =|$V_{TX-Idle-D+}$ - $V_{Tx-Idle-D-}$| = 20mV See Note 1.
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during Receiver Detection			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present.
$RL_{TX-DIFF}$	Differential Return Loss	12			dB	Measured over 50 MHz to 1.25 GHz See Note 2.

Table 4-8. Differential Transmitter (TX) DC Output Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Units	Comments
RL_{TX-CM}	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz See Note 2.
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	W	TX DC Differential Mode Low impedance
$Z_{TX-COM-DC}$	Transmitter Common Mode High Impedance State (DC)	40k			W	Required TX D+ as well as D- DC impedance during all states.
C_{TX}	AC Coupling Capacitor	75		200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

NOTES:
1. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-2 and measured over any 250 consecutive TX UIs. (Also refer to the Transmitter Compliance Eye Diagram as shown in Figure 4-1.)
2. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50Ω to ground for both the D+ and D- line (i.e., as measured by a Vector Network Analyzer with 50Ω probes – see Figure 4-2). Note that the series capacitors C_{TX} is optional for the return loss measurement.

4.1.7.1.2 Differential Receiver (RX) DC Input Specifications

Table 4-9 defines the DC specifications of parameters for all differential receivers (RXs). The parameters are specified at the component pins.

Table 4-9. Differential Receiver (RX) DC Input Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{RX-DIFFp-p}$	Differential Input Peak to Peak Voltage	0.175		1.200	V	$V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ See Note 1.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage			150	mV	$V_{RX-CM-AC}=\|V_{RX-D+} + V_{RX-D-}\|/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\|V_{RX-D+} + V_{RX-D-}\|/2$ during L0 See Note 1.
$RL_{RX-DIFF}$	Differential Return Loss	15			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively. See Note 2.
RL_{RX-CM}	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 2
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	W	RX DC Differential Mode impedance. See Note 3.

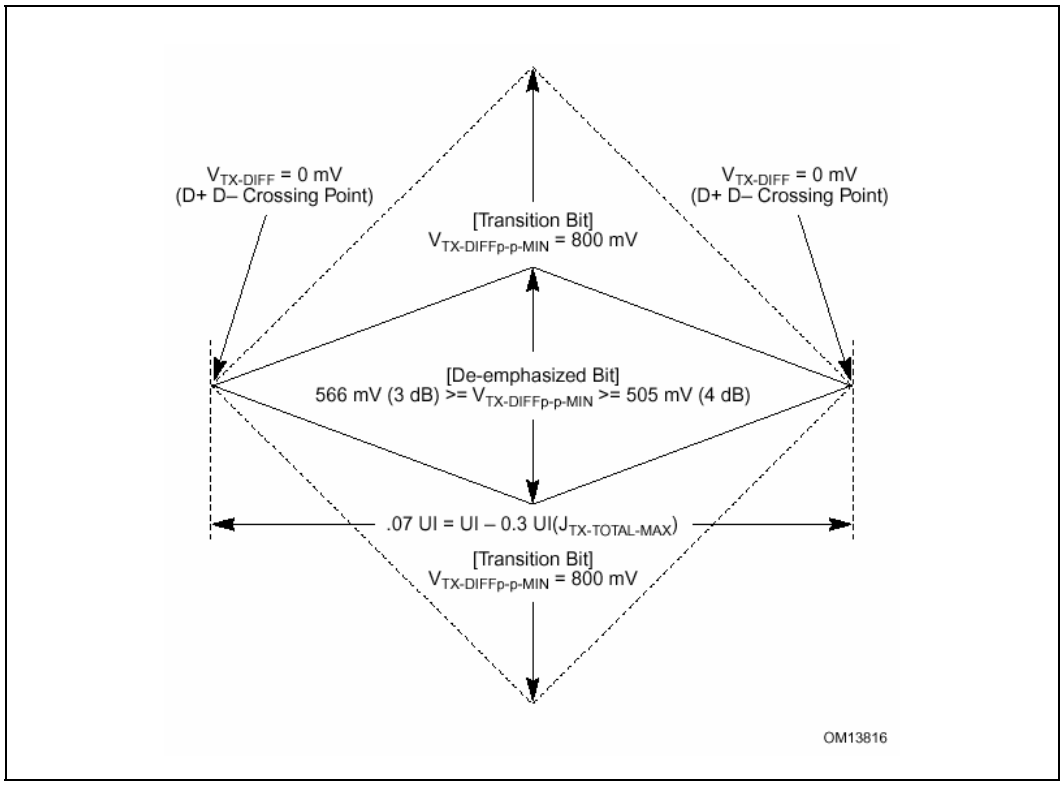
Table 4-9. Differential Receiver (RX) DC Input Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$Z_{RX- DC}$	DC Input Impedance	40	50	60	W	Required RX D+ as well as D-DC impedance (50 Ω+/-20% tolerance). See Notes 1 and 3.
$Z_{RX- HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k			W	Required RX D+ as well as D-DC impedance when the receiver terminations do not have power. See Note 4.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65		175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ Measured at the package pins of the Receiver.

NOTES:
1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 4-2 should be used as the RX device when taking measurements (also refer to the Receiver Compliance Eye Diagram as shown in Figure 4-3). If the clocks to the RX and TX are not derived from the same clock chip the TX UI must be used as a reference for the eye diagram.
2. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D- line (i.e., as measured by a Vector Network Analyzer with 50 Ω probes - see Figure 4-2). Note: that the series capacitors C_{TX} is optional for the return loss measurement.
3. Impedance during all LTSSM states. When transiting from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured Lanes of a Port.

The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

Figure 4-1. Minimum Transmitter Timing and Voltage Output Compliance Specification



There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit.

The eye diagram must be valid for any 250 consecutive UIs. An appropriate average TX UI must be used as the interval for measuring the eye diagram.

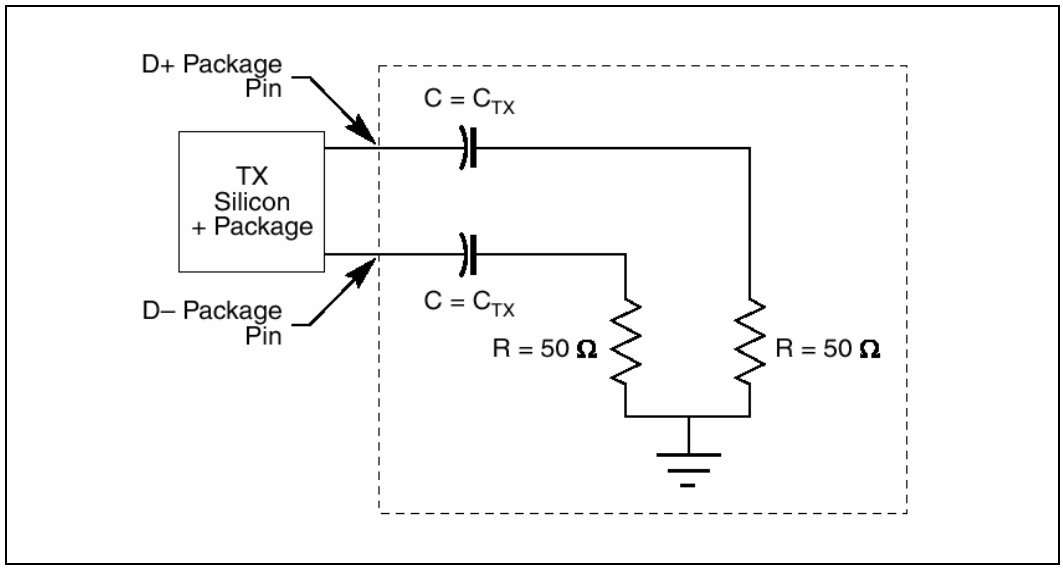
4.1.7.1.3 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified by the device vendor within 0.2 inches of the package pins, into a test/measurement load shown in Figure 4-2.

Note: The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in

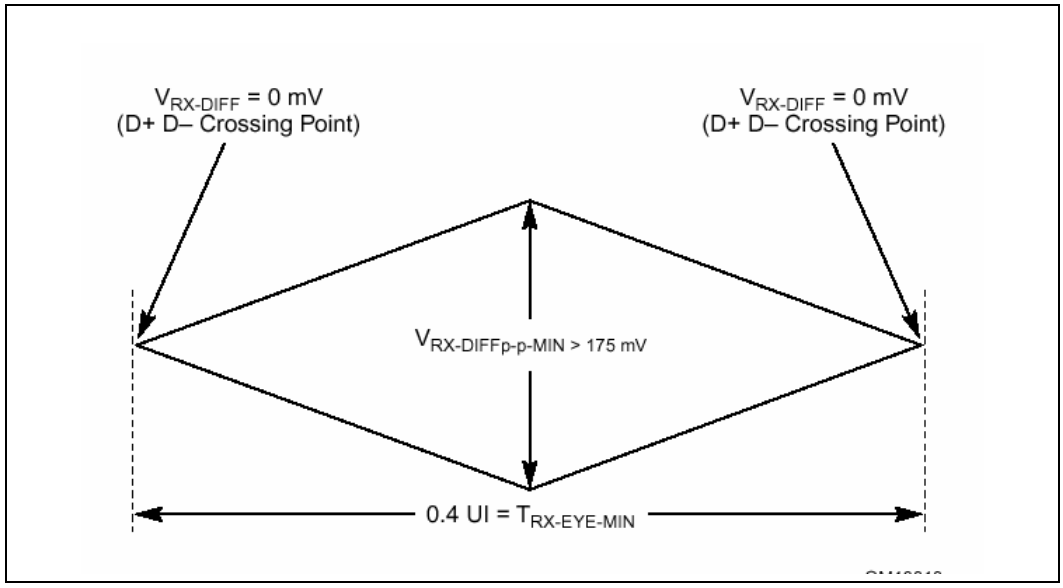
length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D-package pins.

Figure 4-2. Compliance Test/Measurement Load



The test load is shown at the transmitter package reference plane, but the same Test/Measurement load is applicable to the receiver package reference plane. CTX is an optional portion of the measurement test load. The measurement should be taken on the opposite side of the capacitor from the package, and the value of the CTX must be in the range of 75 nF to 200 nF.

Figure 4-3. Minimum Receiver Eye Timing and Voltage Compliance Specification



The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs. An appropriate average TX UI must be used as the interval for measuring the eye diagram.

4.1.7.2 PCI and PCI-X Interface DC Specifications (3.3V Signaling Environment)

Table 4-10 summarizes the DC specifications for 3.3V signaling.

Table 4-10. DC Specifications for PCI and Mode 1 PCI-X 3.3V Signaling

Symbol	Parameter	PCI		PCI-X		Units	Condition	Notes
		Min	Max	Min	Max			
VCC33	Supply Voltage	3.0	3.6	3.0	3.6	V		
V_{ih}	Input High Voltage	0.5VCC33	VCC33 +0.5	0.5VCC33	VCC33 +0.5	V		
V_{il}	Input Low Voltage	-0.5	0.3VCC33	-0.5	0.35VCC33	V		
V_{ipu}	Input Pull-up Voltage	0.7VCC33		0.7VCC33		V		1
I_{il}	Input Leakage Current		±10		±10	µA	$0 < V_{in} <$ VCC33	2
V_{oh}	Output High Voltage	0.9VCC33		0.9VCC33		V	I_{out} = -500 µA	
V_{ol}	Output Low Voltage		0.1VCC33		0.1VCC33	V	I_{out} = 1500 µA	
C_{in}	Input Pin Capacitance		10		10	pF		3
C_{clk}	PAPCLKI Pin Capacitance	5	8	5	8	pF		
C_{IDSEL}	IDSEL Pin Capacitance		8		8	pF		4
L_{pin}	Pin Inductance		20		20	nH		5
I_{Off}	PAPME# input leakage	-	1	-	1	µA	$V_o \leq 3.6$ V VCC33 off or floating	6

NOTES:
1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization must assure that the input buffer is conducting minimum current at this input voltage.
2. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
3. Absolute maximum pin capacitance for a PCI/PCI-X input except PAPCLKI and IDSEL.
4. For conventional PCI only, lower capacitance on this input-only pin allows for non-resistive coupling to PAAD[xx]. PCI-X configuration transactions drive the AD bus four clocks before PAFRAME# asserts (see Section 2.7.2.1 of the *PCI-X Protocol Addendum to the PCI Local Bus Specification*, Revision 2.0a).
5. For conventional PCI, this is a recommendation, not an absolute requirement. For PCI-X, this is a requirement.
6. This input leakage is the maximum allowable leakage into the PAPME# open drain driver when power is removed from VCC33 of the component. This assumes that no event has occurred to cause the device to attempt to assert PAPME#.

4.1.7.3 PCI Hot Plug DC Specifications

Table 4-11. PCI Hot Plug Slot Power Requirements

Supply Voltage	Maximum Operating Current[1]	Maximum Adapter Card Decoupling Capacitance	Minimum Supply Voltage Skew Rate	Maximum Supply Voltage Skew Rate
+5V	5 A	3000 µF	25 V/s	3300 V/s
+3.3V	7.6 A	3000 µF	16.5 V/s	3300 V/s
+12V	500 mA	300 µF	60 V/s	33000 V/s
-12V	100 mA	150 µF	60 V/s	66000 V/s

Combined maximum power drawn by all supply voltages in any one slot must not exceed 25W.

4.1.7.4 Input Clock DC Specifications

Table 4-12. DC Specification for Input Clock Signals

Symbol	Parameter	Min	Max	Units
CLK100	Input Low Voltage	-0.5	0.8	V
CLK100	Input High Voltage	2.0	VCC33 + 0.5	V
CLK133	Input Low Voltage	-0.5	0.8	V
CLK133	Input High Voltage	2.0	VCC33 + 0.5	V

4.1.7.5 Output Clock DC Specifications

Table 4-13. DC Specification for Output Clock Signals

Symbol	Parameter	Min	Max	Units	Condition
CLK33	Output Low Voltage		0.4	V	Iol = 1 mA
CLK33	Output High Voltage	2.4		V	Ioh= -1 mA
CLK66	Output Low Voltage		0.4	V	Iol = 1 mA
CLK66	Output High Voltage	2.4		V	Ioh= -1 mA
CLK100	Output Low Voltage		0.4	V	Iol = 1 mA
CLK100	Output High Voltage	2.4		V	Ioh= -1 mA
CLK133	Output Low Voltage		0.4	V	Iol = 1 mA
CLK133	Output High Voltage	2.4		V	Ioh= -1 mA

4.2 AC Specifications

4.2.1 PCI and PCI-X AC Characteristics

Table 4-14. Conventional PCI 3.3V AC Characteristics

Sym	Parameter	Condition	Min	Max	Unit	Note
$I_{oh(AC)}$	Switching Current High	V_{out} = 0.7VCC33		-32VCC33	mA	
		V_{out} = 0.3VCC33	-12VCC33		mA	1
$I_{ol(AC)}$	Switching Current Low	V_{out} = 0.18VCC33		38VCC33	mA	
		V_{out} = 0.6VCC33	16VCC33		mA	1
I_{ch}	High Clamp Current	VCC33 + 4 > V_{in} = VCC33 + 1	25 + (V_{in} – VCC33 – 1) / 0.015		mA	
I_{cl}	Low Clamp Current	-3 < V_{in} = -1	-25 + (V_{in} + 1) / 0.015		mA	
$slew_r$	Output Rise Slew Rate	0.3VCC33 to 0.6VCC33	1	4	V/ns	2
$slew_f$	Output Fall Slew Rate	0.6VCC33 to 0.3VCC33	1	4	V/ns	2

NOTES:
1. In conventional PCI switching, current characteristics for PAREQ# and PAGNT# are permitted to be one half of that specified here; i.e., half size drivers may be used on these signals. This specification does not apply to CLK and RSTIN# which are system outputs. “Switching Current High” specifications are not relevant to PASERR#, INTA#, INTB#, INTC# and INTD#, which are open drain outputs.
2. This parameter is to be interpreted as the cumulative edge rate across the specified range rather than the instantaneous rate at any point within the transition range. For more details on slew rate measurement conditions please refer to the *PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification*, Revision 2.0a.

Table 4-15. PCI-X 3.3V AC Characteristics

Sym	Parameter	Condition	Min	Max	Unit	Note
$I_{oh(AC)}$	Switching Current High	0 < VCC33 – V_{out} = 3.6V		-74(VCC33 - V_{out})	mA	
		0 < VCC33 – V_{out} = 1.2V	-32 (VCC33 – V_{out})		mA	1
		1.2V < VCC33 – V_{out} = 1.9V	-11 (VCC33 – V_{out}) – 25.2		mA	1
		1.9V < VCC33 – V_{out} = 3.6V	-1.8 (VCC33 – V_{out}) – 42.7		mA	1
$I_{ol(AC)}$	Switching Current Low	0 = V_{out} = 3.6V		$100V_{out}$	mA	
		0 < V_{out} = 1.3V	$48V_{out}$			1
		1.3V < V_{out} = 3.6V	$5.7V_{out}$ + 55			1
I_{cl}	Low Clamp Current	-3V < V_{in} ≤ -0.8875V	-40 + (V_{in} + 1) / 0.005		mA	
		-0.8875V < V_{in} ≤ -0.625V	-25 + (V_{in} + 1) / 0.015		mA	
I_{ch}	High Clamp Current	0.8875V < V_{in} – VCC33 ≤ -4V	40 + (V_{in} – VCC33 - 1) / 0.005		mA	
		0.625V < V_{in} – VCC33 ≤ 0.8875V	25 + (V_{in} – VCC33 - 1) / 0.015		mA	
$slew_r$	Output Rise Slew Rate	0.3VCC33 to 0.6VCC33	1	4	V/ns	2
$slew_f$	Output Fall Slew Rate	0.6VCC33 to 0.3VCC33	1	4	V/ns	2

NOTES:
1. In conventional PCI switching, current characteristics for PAREQ# and PAGNT# are permitted to be one half of that specified here; i.e., half size drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. “Switching Current High” specifications are not relevant to PASERR#, INTA#, INTB#, INTC# and INTD#, which are open drain outputs.
2. This parameter is to be interpreted as the cumulative edge rate across the specified range rather than the instantaneous rate at any point within the transition range. For more details on slew rate measurement conditions please refer to the *PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification,* Revision 2.0a.

4.3 Timing Specifications

4.3.1 PCI Express Interface Timing

4.3.1.1 Differential Transmitter (TX) Output Specifications

Table 4-16 defines the specifications of parameters for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 4-16. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps +/-300 ppm. UI does not account for SSC dictated variations. See Note 1.
T_{TX-EYE}	Minimum TX Eye Width	0.70			UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = .3 UI See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation for the median			0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0V) in relation to an appropriate average TX UI. See Notes 2 and 3.
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- TX Output Rise/ Fall Time	0.125			UI	See Notes 2 and 4.
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50			UI	Minimum time a transmitter must be in Electrical Idle.
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical Idle after sending an Electrical Idle ordered-set			20	UI	After sending an Electrical Idle ordered-set, the transmitter must meet all Electrical Idle specifications within this time.
$T_{TX-IDLE-RCV-DETECT-MAX}$	Maximum time spent in Electrical Idle before initiating a receiver detect sequence.			100	ms	Maximum time spent in Electrical Idle before initiating a receiver detect sequence.
$L_{TX-SKEW}$	Lane-to-Lane Output Skew			500 + 2UI	ps	Static skew between any two Transmitter Lanes within a single Link.

NOTES:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-2 and measured over any 250 consecutive TX UIs. (Also refer to the Transmitter Compliance Eye Diagram as shown in Figure 4-1.)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. Measured between 20-80% at Transmitter package pins into a test load as shown in Figure 4-2 for both V_{TX-D+} and V_{TX-D-}.

4.3.1.2 Differential Receiver (RX) Input Specifications

Table 4-17 defines the specifications of parameters for all differential Receivers (RXs). The parameters are specified at the component pins.

Table 4-17. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	The UI is 400 ps +/-300 ppm. UI does not account for SSC dictated variations. See Note 1.
T_{RX-EYE}	Minimum Receiver Eye Width	0.4			UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER}$ =1 -T_{RX-EYE} =0.6 UI See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to an appropriate average TX UI. See Notes 2 and 3.
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time			10	ms	An unexpected electrical idle ($V_{RX-DIFFp-p}$ <$V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ to signal an unexpected idle condition.
$L_{RX-SKEW}$	Total Skew			20	ns	Across all Lanes on a port. This includes variation in the length of a skip ordered-set (e.g., COM and 1 to 5 SKP symbols) at the RX as well as any delay differences arising from the interconnect itself.

NOTES:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 4-2 should be used as the RX device when taking measurements (also refer to the Receiver Compliance Eye Diagram as shown in Figure 4-3). If the clocks to the RX and TX are not derived from the same clock chip the TX UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total 0.60 UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same clock chip, the appropriate average TX UI must be used as the reference for the eye diagram.

4.3.2 PCI and PCI-X Interface Timing

Table 4-18. Conventional PCI Interface Timing

Functional Operating Range (VCC33 = 3.3V ± 5%, Tcase=0°C to 105°C)								
Symbol	Parameter	66 MHz		33 MHz		Units	Notes
		Min	Max	Min	Max		
T_{val}	CLK to Signal Valid Delay- bused signals	2	6	2	11	ns	1, 2, 3
$T_{val}(ptp)$	CLK to Signal Valid Delay-point-to-point signals	2	6	2	12	ns	1, 2, 3
T_{on}	Float to Active Delay	2		2		ns	1, 7
T_{off}	Active to Float Delay		14		28	ns	1, 7
T_{su}	Input Setup Time to CLK-Bused signals	3		7		ns	3, 4, 8
$T_{su}(ptp)$	Input Setup Time to CLK; point-to-point	5		10,12		ns	3, 4
T_h	Input Hold Time from CLK	0		0		ns	4
T_{rst}	Reset Active Time	1		1		ms	5
$T_{rst-clk}$	Reset Active Time after CLK stable	100		100		µs	5
$T_{rst-off}$	Reset Active to output float delay		40		40	ns	5, 6
T_{rrsu}	PAREQ64# to RSTIN# setup time	10		10		clocks	
T_{rrh}	RSTIN# to PAREQ64# hold Time	0	50	0	50	ns	9
T_{rhfa}	RSTIN# high to first configuration access	2^{25}		2^{25}		clocks	
T_{rhff}	RSTIN# high to first PAFRAME# Assertion	5		5		clocks	
T_{pvrh}	Power Valid to RSTIN# High	100		100		ms	

NOTES:
1. See Figure 4-4. It is important that all driven signal transitions drive to their V_{oh} or V_{ol} level within one T_{cyc}.
2. Minimum times are measured at the package pin (not the test point) with the load circuit shown in the *PCI-X Electrical and Mechanical Addendum*, Revision 2.0a. Maximum times are measured with the test point and load circuit shown in the *PCI-X Electrical and Mechanical Addendum*, Revision 2.0a.
3. PAREQ_[5:0]# and PAGNT_[5:0]# are point-to-point signals and have different input setup times than do bused signals. PAGNT_[5:0]# and PAREQ_[5:0]# have a setup of 5 ns at 66 MHz. All other signals are bused.
4. See Figure and the measurement conditions in the *PCI-X Electrical and Mechanical Addendum*, Revision 2.0a.
5. If PAM66EN is asserted, CLK is stable when it meets the requirements in the *PCI Local Bus Specification,* Revision 2.3. RSTIN# is asserted and deasserted asynchronously with respect to CLK.
6. When PAM66EN is asserted, the minimum specification for T_{val}(min), T_{val}(ptp)(min), and T_{on} may be reduced to 1 ns if a mechanism is provided to guarantee a minimum value of 2 ns when PAM66EN is deasserted.
7. For purposes of active/float timing measurements, the Hi-Z or “off” state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time. Refer to the *PCI Local Bus Specification*, Revision 2.3 for more details.
9. Maximum value is also limited by delay to the first transaction (T_{rhff}).

Figure 4-4. PCI Output Timing

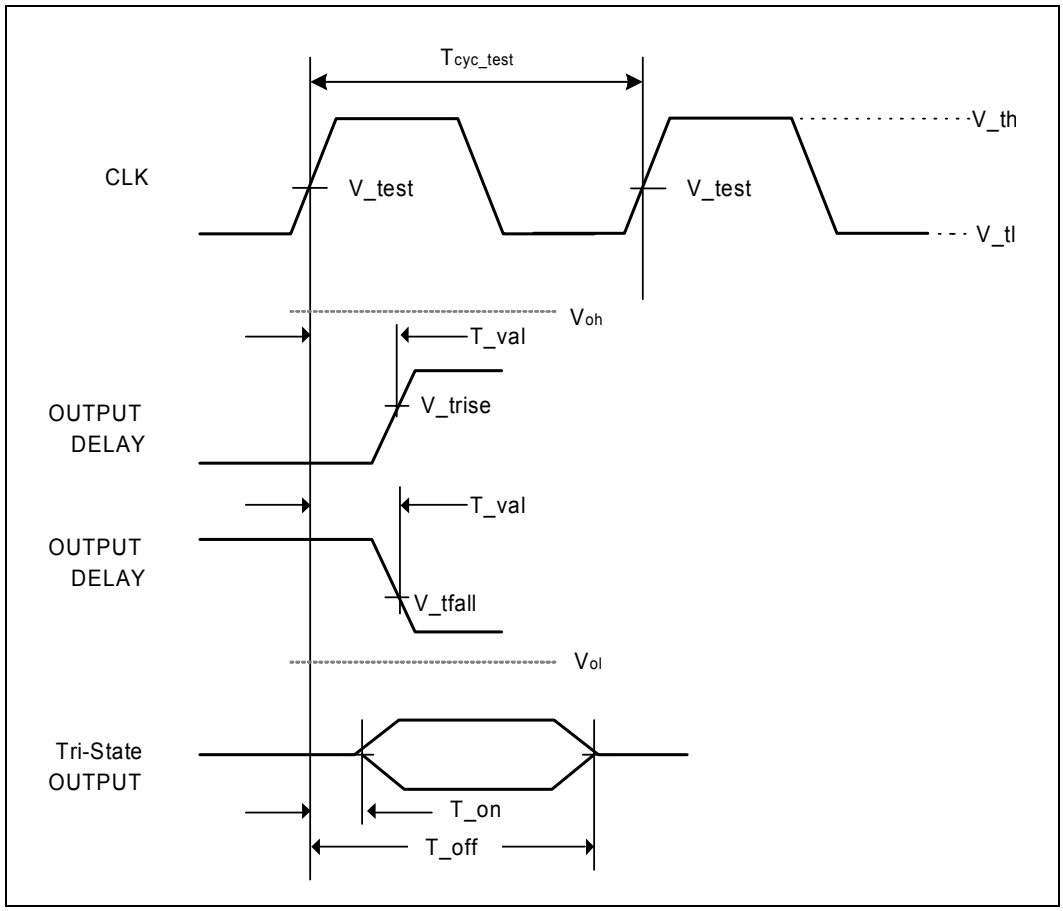
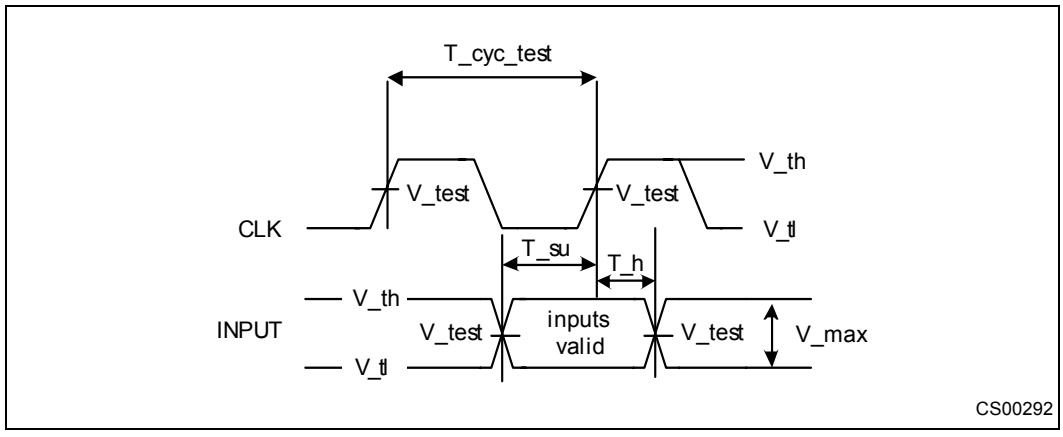


Figure 4-5. PCI Input Timing



NOTES:
1. See the timing measurement conditions in Figure 4-4.
2. Minimum times are measured at the package pin (not the test point) with the load circuit shown in the *PCI-X Electrical and Mechanical Addendum*, Revision 2.0a. Maximum times are measured with the test point and load circuit shown in *PCI-X Electrical and Mechanical Addendum*, Revision 2.0a.

3. See the timing measurement conditions in Figure 4-5 and the *PCI-X Electrical and Mechanical Addendum*, Revision 2.0a.
4. PAPCIRST# is asserted and deasserted asynchronously with respect to CLK.
5. For purposes of Active/Float timing measurements, the Hi-Z or "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification
6. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
7. Maximum value is also limited by delay to the first transaction (T_{rhfa}). The PCI-X initialization pattern control signals after the rising edge of RSTIN# must be deasserted no later than two clocks before the first PAFRAME# and must be floated no later than one clock before PAFRAME# is asserted.
8. Device must meet this specification independent of how many outputs switch simultaneously.

Table 4-19. PCI-X Mode 1 General Timing Parameters

Symbol	Parameter	PCI-X 133 MHz		PCI-X 66 MHz		Units	Notes
		Min	Max	Min	Max		
T_{val}	CLK to Signal Valid Delay (bused signals)	0.7	3.1	0.7	3.1	ns	1, 2, 3, 10, 11
$T_{val}(ptp)$	CLK to Signal Valid Delay (point-to-point signals)	0.7	3.1	0.7	3.1	ns	1, 2, 3, 10, 11
T_{on}	Float to Active Delay	0		0		ns	1, 7, 10, 11
T_{off}	Active to Float Delay		7		7	ns	1, 7, 11
T_{su}	Input Setup Time to CLK (bused signals)	1.2		1.7		ns	3, 4, 8
$T_{su}(ptp)$	Input Setup Time to CLK (point-to-point signals)	1.2		1.7		ns	3, 4
T_{h}	Input Hold Time from CLK	0.5		0.5		ns	4
T_{rst}	Reset Active Time after Power Stable	1		1		ms	5
$T_{rst-clk}$	Reset Active to CLK Stable	100		100		µs	5
$T_{rst-off}$	Reset Active to Output Float Delay		40		40	ns	5, 6
T_{rrsu}	PAREQ64# to RSTIN# Setup Time	10		10		ns	
T_{rrh}	RSTIN# to PAREQ64# Hold Time	0	50	0	50	ns	
T_{rhfa}	RSTIN# High to First Configuration Access	2^{27}		2^{27}		clocks	
T_{rhff}	RSTIN# High to First PAFRAME# Assertion	5		5		clocks	
T_{pvrh}	Power Valid to RSTIN# High	100		100		ms	
T_{prsu}	PCI-X Initialization Pattern to RSTIN# Setup Time	10		10		clocks	
T_{prh}	RSTIN# to PCI-X Initialization Patter Hold Time	0	50	0	50	ns	9
T_{rlcx}	Delay from RSTIN# Low to CLK Frequency Change	0		0		ns	

NOTES:
1. Refer to Figure 4-4. For timing and measurement condition details, refer to the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 2.0a.
2. Minimum times are measured at the package pin (not the test point).
3. Setup time for point-to-point signals applies to PAREQ_5:0]# and PAGNT_5:0]# only. All other signals are bused.
4. See the timing measurement conditions in Figure 4-5.
5. RST# is asserted and deasserted asynchronously with respect to CLK.
6. All output drivers must be floated when RSTIN# is active.
7. For purposes of Active/Float timing measurements, the Hi-Z or "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification
8. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
9. Maximum value is also limited by delay to the first transaction (T_{rhfa}). The PCI-X initialization pattern control signals after the rising edge of RSTIN# must be deasserted no later than two clocks before the first PAFRAME# and must be floated no later than one clock before PAFRAME# is asserted.
10. A PCI-X Mode 1 device is permitted to have the minimum values shown for T_{val}, T_{val}(ptp) and T_{on} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in the *PCI Local Bus Specification*, Revision 2.3 for the appropriate clock frequency.
11. Device must meet this specification independent of how many outputs switch simultaneously.

Figure 4-6. PCI-X Mode 1 Output Timing

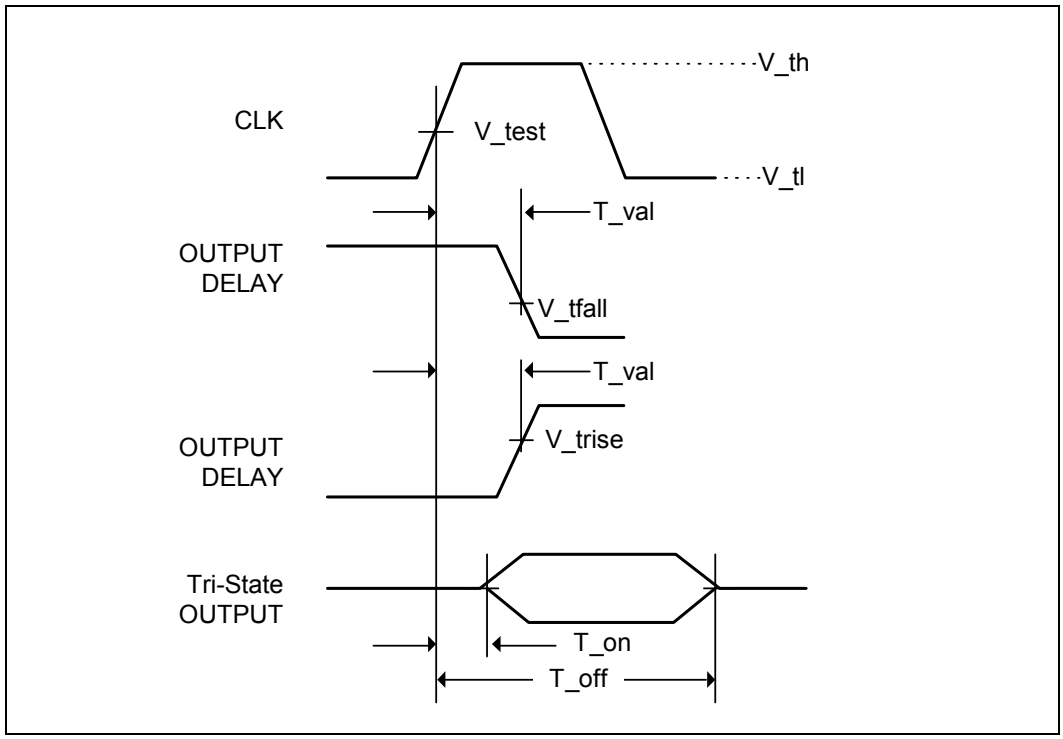
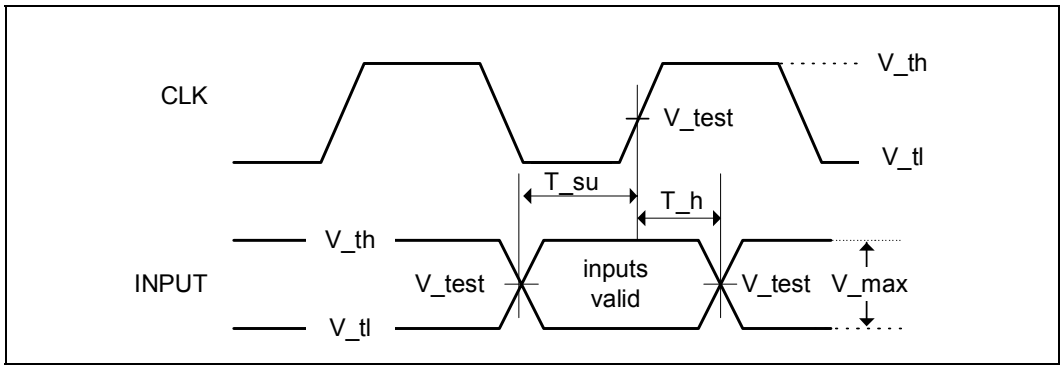


Figure 4-7. PCI-X Mode 1 Input Timing



4.3.3 PCI and PCI-X Clock Specification

Clock measurement conditions are the same for PCI-X devices as for conventional PCI devices in a 3.3V signaling environment except for voltage levels specified in Table 4-20. The same spread-spectrum clocking techniques are allowed in PCI-X as for 66 MHz conventional PCI. If a device includes a PLL, that PLL must track the input variations of spread-spectrum clocking specified in Figure 4-20.

Figure 4-8. PCI-X 3.3V Clock Waveform

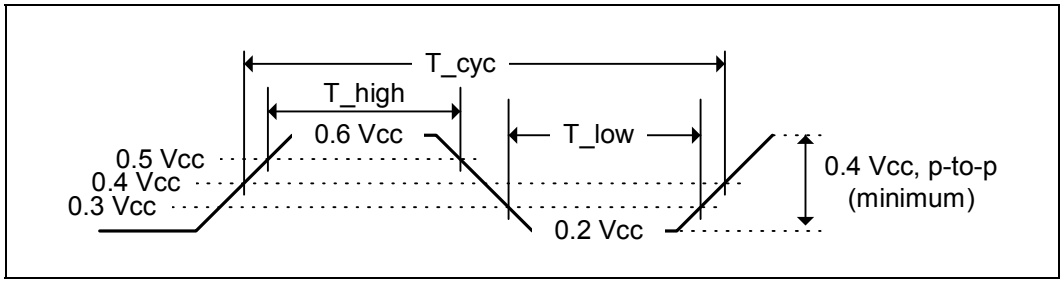


Table 4-20. PCI and PCI-X Clock Timings

Symbol	Parameter	PCI-X 133		PCI-X 66		PCI 66		PCI 33		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
T_{cyc}	CLK cycle time (Average)	7.5	20	15	20	15	30	30	∞	ns	1,3,4
	CLK Cycle Time (Absolute Minimum)	7.375									1,3
T_{high}	CLK high time	3		6		6		11		ns	
T_{low}	CLK low time	3		6		6		11		ns	
T_{jit}	CLK Period Jitter	125	-125	200	-200	200	-200	300	-300	ps	5
Slew Rate											
—	CLK slew rate	1.5	4	1.5	4	1.5	4	1	4	V/ns	2
Spread Spectrum Requirements											
fmod	Modulation frequency	30	33	30	33	30	33			kHz	
fspread	Frequency spread	-1	0	-1	0	-1	0			%	

NOTES:
1. For clock frequencies above 33 MHz, the clock frequency may not change beyond the spread-spectrum and jitter limits except while RSTIN# is asserted.
2. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in the *PCI-X Electrical and Mechanical Addendum*, Revision 2.0a.
3. The minimum clock period must not be violated for any single clock cycle (i.e., accounting for all system jitter).
4. Average T_{cyc} is measured over any 1 µs period of time and must include all sources of clock variation.
5. Period jitter is the deviation between any single period of the clock, T_{cyc}, and the average period of the clock, $T_{cyc(average)}$.

4.3.3.1 Spread Spectrum Clocking

Spread spectrum clocking can be used on the Intel® 6702PXH 64-bit PCI Hub to reduce energy. Spread Spectrum clocking is a common technique used by system designers to meet FCC emissions, where the frequency is deliberately shifted around to spread the energy off of the peak. The following is to be observed when using Spread Spectrum clocking:

1. All device timings (including jitter, skew, min/max clock period, output rise/fall time) MUST meet the existing non-spread spectrum specifications
2. All non-spread Host and PCI functionality must be maintained in the spread spectrum mode (includes all power management functions).
3. The minimum clock period cannot be violated. The preferred method is to adjust the spread technique to not allow for modulation above the nominal frequency. This technique is often called “down-spreading”. The modulation profile in a modulation period can be expressed as:

Equation 4-1. Modulation Profile in a Modulation Period

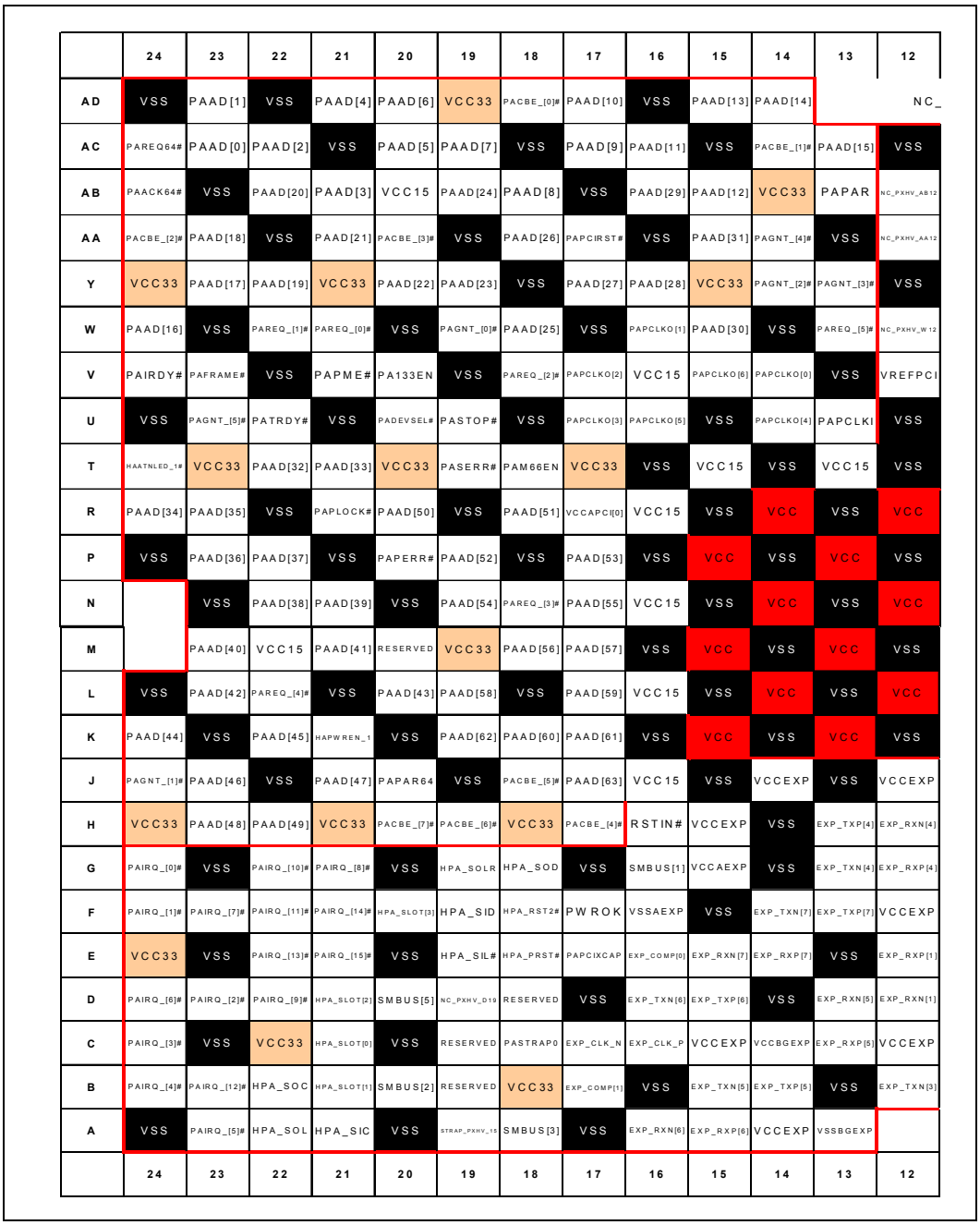
$$f = \begin{cases} (1-\delta)f_{nom} + 2f_m \cdot \delta \cdot f_{nom} \cdot t & when \;\; 0 < t < \dfrac{1}{2f_m} \\ (1+\delta)f_{nom} - 2f_m \cdot \delta \cdot f_{nom} \cdot t & when \;\; \dfrac{1}{2f_m} < t < \dfrac{1}{f_m} \end{cases}$$

where:
f_{nom} is the nominal frequency in the non-SSC mode
f_m is the modulation frequency
f_m is the modulation amount
t is time

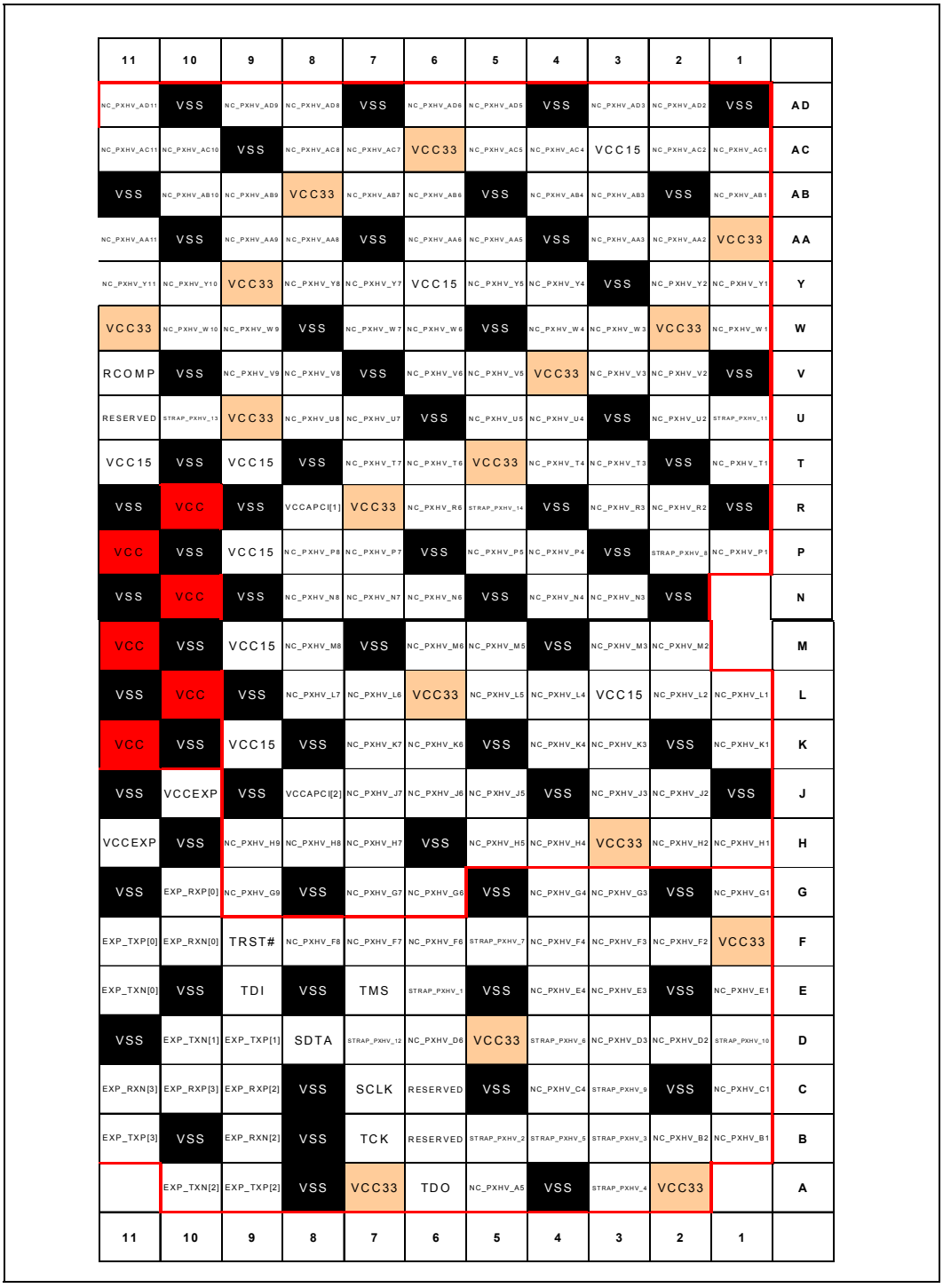
§

5 Component Ballout

5.1 Intel® 6702PXH 64-bit PCI Hub



	24	23	22	21	20	19	18	17	16	15	14	13	12
AD	VSS	PAAD[1]	VSS	PAAD[4]	PAAD[6]	VCC33	PACBE_[0]#	PAAD[10]	VSS	PAAD[13]	PAAD[14]		NC_
AC	PAREQ64#	PAAD[0]	PAAD[2]	VSS	PAAD[5]	PAAD[7]	VSS	PAAD[9]	PAAD[11]	VSS	PACBE_[1]#	PAAD[15]	VSS
AB	PAACK64#	VSS	PAAD[20]	PAAD[3]	VCC15	PAAD[24]	PAAD[8]	VSS	PAAD[29]	PAAD[12]	VCC33	PAPAR	NC_PXHV_AB12
AA	PACBE_[2]#	PAAD[18]	VSS	PAAD[21]	PACBE_[3]#	VSS	PAAD[26]	PAPCIRST#	VSS	PAAD[31]	PAGNT_[4]#	VSS	NC_PXHV_AA12
Y	VCC33	PAAD[17]	PAAD[19]	VCC33	PAAD[22]	PAAD[23]	VSS	PAAD[27]	PAAD[28]	VCC33	PAGNT_[2]#	PAGNT_[3]#	VSS
W	PAAD[16]	VSS	PAREQ_[1]#	PAREQ_[0]#	VSS	PAGNT_[0]#	PAAD[25]	VSS	PAPCLKO[1]	PAAD[30]	VSS	PAREQ_[5]#	NC_PXHV_W12
V	PAIRDY#	PAFRAME#	VSS	PAPME#	PA133EN	VSS	PAREQ_[2]#	PAPCLKO[2]	VCC15	PAPCLKO[6]	PAPCLKO[0]	VSS	VREFPCI
U	VSS	PAGNT_[5]#	PATRDY#	VSS	PADEVSEL#	PASTOP#	VSS	PAPCLKO[3]	PAPCLKO[5]	VSS	PAPCLKO[4]	PAPCLKI	VSS
T	HAATNLED_1#	VCC33	PAAD[32]	PAAD[33]	VCC33	PASERR#	PAM66EN	VCC33	VSS	VCC15	VSS	VCC15	VSS
R	PAAD[34]	PAAD[35]	VSS	PAPLOCK#	PAAD[50]	VSS	PAAD[51]	VCCAPCI[0]	VCC15	VSS	VCC	VSS	VCC
P	VSS	PAAD[36]	PAAD[37]	VSS	PAPERR#	PAAD[52]	VSS	PAAD[53]	VSS	VCC	VSS	VCC	VSS
N		VSS	PAAD[38]	PAAD[39]	VSS	PAAD[54]	PAREQ_[3]#	PAAD[55]	VCC15	VSS	VCC	VSS	VCC
M		PAAD[40]	VCC15	PAAD[41]	RESERVED	VCC33	PAAD[56]	PAAD[57]	VSS	VCC	VSS	VCC	VSS
L	VSS	PAAD[42]	PAREQ_[4]#	VSS	PAAD[43]	PAAD[58]	VSS	PAAD[59]	VCC15	VSS	VCC	VSS	VCC
K	PAAD[44]	VSS	PAAD[45]	HAPWREN_1	VSS	PAAD[62]	PAAD[60]	PAAD[61]	VSS	VCC	VSS	VCC	VSS
J	PAGNT_[1]#	PAAD[46]	VSS	PAAD[47]	PAPAR64	VSS	PACBE_[5]#	PAAD[63]	VCC15	VSS	VCCEXP	VSS	VCCEXP
H	VCC33	PAAD[48]	PAAD[49]	VCC33	PACBE_[7]#	PACBE_[6]#	VCC33	PACBE_[4]#	RSTIN#	VCCEXP	VSS	EXP_TXP[4]	EXP_RXN[4]
G	PAIRQ_[0]#	VSS	PAIRQ_[10]#	PAIRQ_[8]#	VSS	HPA_SOLR	HPA_SOD	VSS	SMBUS[1]	VCCAEXP	VSS	EXP_TXN[4]	EXP_RXP[4]
F	PAIRQ_[1]#	PAIRQ_[7]#	PAIRQ_[11]#	PAIRQ_[14]#	HPA_SLOT[3]	HPA_SID	HPA_RST2#	PWROK	VSSAEXP	VSS	EXP_TXN[7]	EXP_TXP[7]	VCCEXP
E	VCC33	VSS	PAIRQ_[13]#	PAIRQ_[15]#	VSS	HPA_SIL#	HPA_PRST#	PAPCIXCAP	EXP_COMP[0]	EXP_RXN[7]	EXP_RXP[7]	VSS	EXP_RXP[1]
D	PAIRQ_[6]#	PAIRQ_[2]#	PAIRQ_[9]#	HPA_SLOT[2]	SMBUS[5]	NC_PXHV_D19	RESERVED	VSS	EXP_TXN[6]	EXP_TXP[6]	VSS	EXP_RXN[5]	EXP_RXN[1]
C	PAIRQ_[3]#	VSS	VCC33	HPA_SLOT[0]	VSS	RESERVED	PASTRAP0	EXP_CLK_N	EXP_CLK_P	VCCEXP	VCCBGEXP	EXP_RXP[5]	VCCEXP
B	PAIRQ_[4]#	PAIRQ_[12]#	HPA_SOC	HPA_SLOT[1]	SMBUS[2]	RESERVED	VCC33	EXP_COMP[1]	VSS	EXP_TXN[5]	EXP_TXP[5]	VSS	EXP_TXN[3]
A	VSS	PAIRQ_[5]#	HPA_SOL	HPA_SIC	VSS	STRAP_PXHV_13	SMBUS[3]	VSS	EXP_RXN[6]	EXP_RXP[6]	VCCEXP	VSSBGEXP	
	24	23	22	21	20	19	18	17	16	15	14	13	12



11	10	9	8	7	6	5	4	3	2	1	
NC_PXHV_AD11	VSS	NC_PXHV_AD9	NC_PXHV_AD8	VSS	NC_PXHV_AD6	NC_PXHV_AD5	VSS	NC_PXHV_AD3	NC_PXHV_AD2	VSS	AD
NC_PXHV_AC11	NC_PXHV_AC10	VSS	NC_PXHV_AC8	NC_PXHV_AC7	VCC33	NC_PXHV_AC5	NC_PXHV_AC4	VCC15	NC_PXHV_AC2	NC_PXHV_AC1	AC
VSS	NC_PXHV_AB10	NC_PXHV_AB9	VCC33	NC_PXHV_AB7	NC_PXHV_AB6	VSS	NC_PXHV_AB4	NC_PXHV_AB3	VSS	NC_PXHV_AB1	AB
NC_PXHV_AA11	VSS	NC_PXHV_AA9	NC_PXHV_AA8	VSS	NC_PXHV_AA6	NC_PXHV_AA5	VSS	NC_PXHV_AA3	NC_PXHV_AA2	VCC33	AA
NC_PXHV_Y11	NC_PXHV_Y10	VCC33	NC_PXHV_Y8	NC_PXHV_Y7	VCC15	NC_PXHV_Y5	NC_PXHV_Y4	VSS	NC_PXHV_Y2	NC_PXHV_Y1	Y
VCC33	NC_PXHV_W10	NC_PXHV_W9	VSS	NC_PXHV_W7	NC_PXHV_W6	VSS	NC_PXHV_W4	NC_PXHV_W3	VCC33	NC_PXHV_W1	W
RCOMP	VSS	NC_PXHV_V9	NC_PXHV_V8	VSS	NC_PXHV_V6	NC_PXHV_V5	VCC33	NC_PXHV_V3	NC_PXHV_V2	VSS	V
RESERVED	STRAP_PXHV_13	VCC33	NC_PXHV_U8	NC_PXHV_U7	VSS	NC_PXHV_U5	NC_PXHV_U4	VSS	NC_PXHV_U2	STRAP_PXHV_11	U
VCC15	VSS	VCC15	VSS	NC_PXHV_T7	NC_PXHV_T6	VCC33	NC_PXHV_T4	NC_PXHV_T3	VSS	NC_PXHV_T1	T
VSS	VCC	VSS	VCCAPCI[1]	VCC33	NC_PXHV_R6	STRAP_PXHV_14	VSS	NC_PXHV_R3	NC_PXHV_R2	VSS	R
VCC	VSS	VCC15	NC_PXHV_P8	NC_PXHV_P7	VSS	NC_PXHV_P5	NC_PXHV_P4	VSS	STRAP_PXHV_8	NC_PXHV_P1	P
VSS	VCC	VSS	NC_PXHV_N8	NC_PXHV_N7	NC_PXHV_N6	VSS	NC_PXHV_N4	NC_PXHV_N3	VSS		N
VCC	VSS	VCC15	NC_PXHV_M8	VSS	NC_PXHV_M6	NC_PXHV_M5	VSS	NC_PXHV_M3	NC_PXHV_M2		M
VSS	VCC	VSS	NC_PXHV_L7	NC_PXHV_L6	VCC33	NC_PXHV_L5	NC_PXHV_L4	VCC15	NC_PXHV_L2	NC_PXHV_L1	L
VCC	VSS	VCC15	VSS	NC_PXHV_K7	NC_PXHV_K6	VSS	NC_PXHV_K4	NC_PXHV_K3	VSS	NC_PXHV_K1	K
VSS	VCCEXP	VSS	VCCAPCI[2]	NC_PXHV_J7	NC_PXHV_J6	NC_PXHV_J5	VSS	NC_PXHV_J3	NC_PXHV_J2	VSS	J
VCCEXP	VSS	NC_PXHV_H9	NC_PXHV_H8	NC_PXHV_H7	VSS	NC_PXHV_H5	NC_PXHV_H4	VCC33	NC_PXHV_H2	NC_PXHV_H1	H
VSS	EXP_RXP[0]	NC_PXHV_G9	VSS	NC_PXHV_G7	NC_PXHV_G6	VSS	NC_PXHV_G4	NC_PXHV_G3	VSS	NC_PXHV_G1	G
EXP_TXP[0]	EXP_RXN[0]	TRST#	NC_PXHV_F8	NC_PXHV_F7	NC_PXHV_F6	STRAP_PXHV_7	NC_PXHV_F4	NC_PXHV_F3	NC_PXHV_F2	VCC33	F
EXP_TXN[0]	VSS	TDI	VSS	TMS	STRAP_PXHV_1	VSS	NC_PXHV_E4	NC_PXHV_E3	VSS	NC_PXHV_E1	E
VSS	EXP_TXN[1]	EXP_TXP[1]	SDTA	STRAP_PXHV_12	NC_PXHV_D6	VCC33	STRAP_PXHV_6	NC_PXHV_D3	NC_PXHV_D2	STRAP_PXHV_10	D
EXP_RXN[3]	EXP_RXP[3]	EXP_RXP[2]	VSS	SCLK	RESERVED	VSS	NC_PXHV_C4	STRAP_PXHV_9	VSS	NC_PXHV_C1	C
EXP_TXP[3]	VSS	EXP_RXN[2]	VSS	TCK	RESERVED	STRAP_PXHV_2	STRAP_PXHV_5	STRAP_PXHV_3	NC_PXHV_B2	NC_PXHV_B1	B
	EXP_TXN[2]	EXP_TXP[2]	VSS	VCC33	TDO	NC_PXHV_A5	VSS	STRAP_PXHV_4	VCC33		A
11	10	9	8	7	6	5	4	3	2	1	

§

6 Signal Lists

6.1 Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name)

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 1 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
EXP_CLK_N		C17
EXP_CLK_P		C16
EXP_COMP[0]		E16
EXP_COMP[1]		B17
EXP_RXN[0]		F10
EXP_RXN[1]		D12
EXP_RXN[2]		B9
EXP_RXN[3]		C11
EXP_RXN[4]		H12
EXP_RXN[5]		D13
EXP_RXN[6]		A16
EXP_RXN[7]		E15
EXP_RXP[0]		G10
EXP_RXP[1]		E12
EXP_RXP[2]		C9
EXP_RXP[3]		C10
EXP_RXP[4]		G12
EXP_RXP[5]		C13
EXP_RXP[6]		A15
EXP_RXP[7]		E14
EXP_TXN[0]		E11
EXP_TXN[1]		D10
EXP_TXN[2]		A10
EXP_TXN[3]		B12
EXP_TXN[4]		G13
EXP_TXN[5]		B15
EXP_TXN[6]		D16
EXP_TXN[7]		F14
EXP_TXP[0]		F11

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 2 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
EXP_TXP[1]		D9
EXP_TXP[2]		A9
EXP_TXP[3]		B11
EXP_TXP[4]		H13
EXP_TXP[5]		B14
EXP_TXP[6]		D15
EXP_TXP[7]		F13
HAATNLED_1_N		T24
HAPWREN_1		K21
HPA_PRST_N	HPA_RST1_N	E18
HPA_RST2_N		F18
HPA_SIC	HAPWRLED2_N	A21
HPA_SID	HAPCIXCAP1_2	F19
HPA_SIL_N	HACLKEN_1_N	E19
HPA_SLOT[0]	HAMRL_2_N	C21
HPA_SLOT[1]	HAPRSNT1_1_N	B21
HPA_SLOT[2]		D21
HPA_SLOT[3]	HAPWRLED1_N	F20
HPA_SOC	HAPCIXCAP2_2	B22
HPA_SOD	HACLKEN_2_N	G18
HPA_SOL	HABUTTON2_N	A22
HPA_SOLR	HAATNLED2_N	G19
NC_PXHV_A5		A5
NC_PXHV_AA2		AA2
NC_PXHV_AA3		AA3
NC_PXHV_AA5		AA5
NC_PXHV_AA6		AA6
NC_PXHV_AA8		AA8
NC_PXHV_AA9		AA9
NC_PXHV_AA11		AA11
NC_PXHV_AA12		AA12
NC_PXHV_AB1		AB1
NC_PXHV_AB3		AB3
NC_PXHV_AB4		AB4
NC_PXHV_AB6		AB6
NC_PXHV_AB7		AB7
NC_PXHV_AB9		AB9

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 3 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
NC_PXHV_AB10		AB10
NC_PXHV_AB12		AB12
NC_PXHV_AC1		AC1
NC_PXHV_AC2		AC2
NC_PXHV_AC4		AC4
NC_PXHV_AC5		AC5
NC_PXHV_AC7		AC7
NC_PXHV_AC8		AC8
NC_PXHV_AC10		AC10
NC_PXHV_AC11		AC11
NC_PXHV_AD2		AD2
NC_PXHV_AD3		AD3
NC_PXHV_AD5		AD5
NC_PXHV_AD6		AD6
NC_PXHV_AD8		AD8
NC_PXHV_AD9		AD9
NC_PXHV_AD11		AD11
NC_PXHV_B1		B1
NC_PXHV_B2		B2
NC_PXHV_C1		C1
NC_PXHV_C4		C4
NC_PXHV_D2		D2
NC_PXHV_D3		D3
NC_PXHV_D6		D6
NC_PXHV_D19		D19
NC_PXHV_E1		E1
NC_PXHV_E3		E3
NC_PXHV_E4		E4
NC_PXHV_F2		F2
NC_PXHV_F3		F3
NC_PXHV_F4		F4
NC_PXHV_F6		F6
NC_PXHV_F7		F7
NC_PXHV_F8		F8
NC_PXHV_G1		G1
NC_PXHV_G3		G3
NC_PXHV_G4		G4

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 4 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
NC_PXHV_G6		G6
NC_PXHV_G7		G7
NC_PXHV_G9		G9
NC_PXHV_H1		H1
NC_PXHV_H2		H2
NC_PXHV_H4		H4
NC_PXHV_H5		H5
NC_PXHV_H7		H7
NC_PXHV_H8		H8
NC_PXHV_H9		H9
NC_PXHV_J2		J2
NC_PXHV_J3		J3
NC_PXHV_J5		J5
NC_PXHV_J6		J6
NC_PXHV_J7		J7
NC_PXHV_K1		K1
NC_PXHV_K3		K3
NC_PXHV_K4		K4
NC_PXHV_K6		K6
NC_PXHV_K7		K7
NC_PXHV_L1		L1
NC_PXHV_L2		L2
NC_PXHV_L4		L4
NC_PXHV_L5		L5
NC_PXHV_L7		L7
NC_PXHV_L8		L8
NC_PXHV_M2		M2
NC_PXHV_M3		M3
NC_PXHV_M5		M5
NC_PXHV_M6		M6
NC_PXHV_M8		M8
NC_PXHV_N3		N3
NC_PXHV_N4		N4
NC_PXHV_N6		N6
NC_PXHV_N7		N7
NC_PXHV_N8		N8
NC_PXHV_P1		P1

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 5 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
NC_PXHV_P4		P4
NC_PXHV_P5		P5
NC_PXHV_P7		P7
NC_PXHV_P8		P8
NC_PXHV_R2		R2
NC_PXHV_R3		R3
NC_PXHV_R6		R6
NC_PXHV_T1		T1
NC_PXHV_T3		T3
NC_PXHV_T4		T4
NC_PXHV_T6		T6
NC_PXHV_T7		T7
NC_PXHV_U2		U2
NC_PXHV_U4		U4
NC_PXHV_U5		U5
NC_PXHV_U7		U7
NC_PXHV_U8		U8
NC_PXHV_V2		V2
NC_PXHV_V3		V3
NC_PXHV_V5		V5
NC_PXHV_V6		V6
NC_PXHV_V8		V8
NC_PXHV_V9		V9
NC_PXHV_W1		W1
NC_PXHV_W3		W3
NC_PXHV_W4		W4
NC_PXHV_W6		W6
NC_PXHV_W7		W7
NC_PXHV_W9		W9
NC_PXHV_W10		W10
NC_PXHV_W12		W12
NC_PXHV_Y1		Y1
NC_PXHV_Y2		Y2
NC_PXHV_Y4		Y4
NC_PXHV_Y5		Y5
NC_PXHV_Y7		Y7
NC_PXHV_Y8		Y8

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 6 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
NC_PXHV_Y10		Y10
NC_PXHV_Y11		Y11
PA133EN		V20
PAACK64_N		AB24
PAAD[0]		AC23
PAAD[1]		AD23
PAAD[10]		AD17
PAAD[11]		AC16
PAAD[12]		AB15
PAAD[13]		AD15
PAAD[14]		AD14
PAAD[15]		AC13
PAAD[16]		W24
PAAD[17]		Y23
PAAD[18]		AA23
PAAD[19]		Y22
PAAD[2]		AC22
PAAD[20]		AB22
PAAD[21]		AA21
PAAD[22]		Y20
PAAD[23]		Y19
PAAD[24]		AB19
PAAD[25]		W18
PAAD[26]		AA18
PAAD[27]		Y17
PAAD[28]		Y16
PAAD[29]		AB16
PAAD[3]		AB21
PAAD[30]		W15
PAAD[31]		AA15
PAAD[32]		T22
PAAD[33]		T21
PAAD[34]		R24
PAAD[35]		R23
PAAD[36]		P23
PAAD[37]		P22
PAAD[38]		N22

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 7 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
PAAD[39]		N21
PAAD[4]		AD21
PAAD[40]		M23
PAAD[41]		M21
PAAD[42]		L23
PAAD[43]		L20
PAAD[44]		K24
PAAD[45]		K22
PAAD[46]		J23
PAAD[47]		J21
PAAD[48]		H23
PAAD[49]		H22
PAAD[5]		AC20
PAAD[50]		R20
PAAD[51]		R18
PAAD[52]		P19
PAAD[53]		P17
PAAD[54]		N19
PAAD[55]		N17
PAAD[56]		M18
PAAD[57]		M17
PAAD[58]		L19
PAAD[59]		L17
PAAD[6]		AD20
PAAD[60]		K18
PAAD[61]		K17
PAAD[62]		K19
PAAD[63]		J17
PAAD[7]		AC19
PAAD[8]		AB18
PAAD[9]		AC17
PACBE_N[0]		AD18
PACBE_N[1]		AC14
PACBE_N[2]		AA24
PACBE_N[3]		AA20
PACBE_N[4]		H17
PACBE_N[5]		J18

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 8 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
PACBE_N[6]		H19
PACBE_N['7]		H20
PADEVSEL_N		U20
PAFRAME_N		V23
PAGNT_N[0]		W19
PAGNT_N[1]		J24
PAGNT_N[2]		Y14
PAGNT_N[3]	HAPWREN_2	Y13
PAGNT_N[4]	HABUSEN_2_N	AA14
PAGNT_N[5]	HABUSEN_1_N	U23
PAIRDY_N		V24
PAIRQ_N[0]		G24
PAIRQ_N[1]		F24
PAIRQ_N[10]	HAPCIXCAP1_1	G22
PAIRQ_N[11]	HAM66EN_1	F22
PAIRQ_N[12]	HAM66EN_2	B23
PAIRQ_N[13]	HAPWRFLT_2_N	E22
PAIRQ_N[14]	HAPWRFLT_1_N	F21
PAIRQ_N[15]	HAMRL1_N	E21
PAIRQ_N[2]		D23
PAIRQ_N[3]		C24
PAIRQ_N[4]		B24
PAIRQ_N[5]		A23
PAIRQ_N[6]		D24
PAIRQ_N[7]		F23
PAIRQ_N[8]	HABUTTON_1_N	G21
PAIRQ_N[9]	HAPCIXCAP2_1	D22
PAM66EN		T18
PAPAR		AB13
PAPAR64		J20
PAPCIRST_N		AA17
PAPCIXCAP		E17
PAPCLKI		U13
PAPCLKO[0]		V14
PAPCLKO[1]		W16
PAPCLKO[2]		V17
PAPCLKO[3]		U17

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 9 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
PAPCLKO[4]		U14
PAPCLKO[5]		U16
PAPCLKO[6]		V15
PAPERR_N		P20
PAPLOCK_N		R21
PAPME_N		V21
PAREQ_N[0]		W21
PAREQ_N[1]		W22
PAREQ_N[2]		V18
PAREQ_N[3]	HAPRSNT2_1_N	N18
PAREQ_N[4]	HAPRSNT2_2_N	L22
PAREQ_N[5]	HAPRSNT1_2_N	W13
PAREQ64_N		AC24
PASERR_N		T19
PASTOP_N		U19
PASTRAP0		C18
PATRDY_N		U22
PWROK		F17
RCOMP		V11
RESERVED		B6
RESERVED		B19
RESERVED		C19
RESERVED		C6
RESERVED		D18
RESERVED		M20
RESERVED		U11
RSTIN_N		H16
SCLK		C7
SDTA		D8
SMBUS[1]		G16
SMBUS[2]		B20
SMBUS[3]		A18
SMBUS[5]		D20
STRAP_PXHV_1		E6
STRAP_PXHV_2		B5
STRAP_PXHV_3		B3
STRAP_PXHV_4		A3

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 10 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
STRAP_PXHV_5		B4
STRAP_PXHV_6		D4
STRAP_PXHV_7		F5
STRAP_PXHV_8		P2
STRAP_PXHV_9		C3
STRAP_PXHV_10		D1
STRAP_PXHV_11		U1
STRAP_PXHV_12		D7
STRAP_PXHV_13		U10
STRAP_PXHV_14		R5
STRAP_PXHV_15		A19
TCK		B7
TDI		E9
TDO		A6
TMS		E7
TRST_N		F9
VCC		K11
VCC		K13
VCC		K15
VCC		L10
VCC		L12
VCC		L14
VCC		M11
VCC		M13
VCC		M15
VCC		N10
VCC		N12
VCC		N14
VCC		P11
VCC		P13
VCC		P15
VCC		R10
VCC		R12
VCC		R14
VCC15		AB20
VCC15		AC3
VCC15		J16

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 11 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
VCC15		K9
VCC15		L16
VCC15		L3
VCC15		M22
VCC15		M9
VCC15		N16
VCC15		P9
VCC15		R16
VCC15		T11
VCC15		T13
VCC15		T15
VCC15		T9
VCC15		V16
VCC15		Y6
VCC33		B18
VCC33		A2
VCC33		A7
VCC33		AA1
VCC33		AB14
VCC33		AB8
VCC33		AC6
VCC33		AD19
VCC33		C22
VCC33		D5
VCC33		E24
VCC33		F1
VCC33		H18
VCC33		H21
VCC33		H24
VCC33		H3
VCC33		L6
VCC33		M19
VCC33		R7
VCC33		T17
VCC33		T20
VCC33		T23
VCC33		T5

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 12 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
VCC33		U9
VCC33		V4
VCC33		W11
VCC33		W2
VCC33		Y15
VCC33		Y21
VCC33		Y24
VCC33		Y9
VCCAEXP		G15
VCCAPCI[0]		R17
VCCAPCI[1]		R8
VCCAPCI[2]		J8
VCCBGEXP		C14
VCCEXP		A14
VCCEXP		C12
VCCEXP		C15
VCCEXP		F12
VCCEXP		H11
VCCEXP		H15
VCCEXP		J10
VCCEXP		J12
VCCEXP		J14
VREFPCI		V12
VSS		B8
VSS		B10
VSS		B13
VSS		B16
VSS		A17
VSS		A20
VSS		A24
VSS		A4
VSS		A8
VSS		AA10
VSS		AA13
VSS		AA16
VSS		AA19
VSS		AA22

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 13 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
VSS		AA4
VSS		AA7
VSS		AB11
VSS		AB17
VSS		AB2
VSS		AB23
VSS		AB5
VSS		AC12
VSS		AC15
VSS		AC18
VSS		AC21
VSS		AC9
VSS		AD1
VSS		AD10
VSS		AD16
VSS		AD22
VSS		AD24
VSS		AD4
VSS		AD7
VSS		C2
VSS		C20
VSS		C23
VSS		C5
VSS		C8
VSS		D11
VSS		D14
VSS		D17
VSS		E10
VSS		E13
VSS		E2
VSS		E20
VSS		E23
VSS		E5
VSS		E8
VSS		F15
VSS		G11
VSS		G14

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 14 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
VSS		G17
VSS		G2
VSS		G20
VSS		G23
VSS		G5
VSS		G8
VSS		H10
VSS		H14
VSS		H6
VSS		J1
VSS		J11
VSS		J13
VSS		J15
VSS		J19
VSS		J22
VSS		J4
VSS		J9
VSS		K10
VSS		K12
VSS		K14
VSS		K16
VSS		K2
VSS		K20
VSS		K23
VSS		K5
VSS		K8
VSS		L11
VSS		L13
VSS		L15
VSS		L18
VSS		L21
VSS		L24
VSS		L9
VSS		M10
VSS		M12
VSS		M14
VSS		M16

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 15 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
VSS		M4
VSS		M7
VSS		N11
VSS		N13
VSS		N15
VSS		N2
VSS		N20
VSS		N23
VSS		N5
VSS		N9
VSS		P10
VSS		P12
VSS		P14
VSS		P16
VSS		P18
VSS		P21
VSS		P24
VSS		P3
VSS		P6
VSS		R1
VSS		R11
VSS		R13
VSS		R15
VSS		R19
VSS		R22
VSS		R4
VSS		R9
VSS		T10
VSS		T12
VSS		T14
VSS		T16
VSS		T2
VSS		T8
VSS		U12
VSS		U15
VSS		U18
VSS		U21

Table 6-1. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Signal Name) (Sheet 16 of 16)

Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux	Pin#
VSS		U24
VSS		U3
VSS		U6
VSS		V1
VSS		V10
VSS		V13
VSS		V19
VSS		V22
VSS		V7
VSS		W14
VSS		W17
VSS		W20
VSS		W23
VSS		W5
VSS		W8
VSS		Y12
VSS		Y18
VSS		Y3
VSSAEXP		F16
VSSBGEXP		A13

6.2 Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number)

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 1 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
A2	VCC33	
A3	STRAP_PXHV_4	HBMRL_2_N
A4	VSS	
A5	NC_PXHV_A5	HBATNLED2_N
A6	TDO	
A7	VCC33	
A8	VSS	
A9	EXP_TXP[2]	
A10	EXP_TXN[2]	
A13	VSSBGEXP	
A14	VCCEXP	
A15	EXP_RXP[6]	
A16	EXP_RXN[6]	
A17	VSS	
A18	SMBUS[3]	
A19	STRAP_PXHV_15	
A20	VSS	
A21	HPA_SIC	HAPWRLED2_N
A22	HPA_SOL	HABUTTON2_N
A23	PAIRQ_N[5]	
A24	VSS	
B1	NC_PXHV_B1	HBPCIXCAP1_1
B2	NC_PXHV_B2	
B3	STRAP_PXHV_3	HBPCIXCAP2_2
B4	STRAP_PXHV_5	HBPRSNT1_1_N
B5	STRAP_PXHV_2	HBPCIXCAP1_2
B6	RESERVED	
B7	TCK	
B8	VSS	
B9	EXP_RXN[2]	
B10	VSS	
B11	EXP_TXP[3]	
B12	EXP_TXN[3]	

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 2 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
B13	VSS	
B14	EXP_TXP[5]	
B15	EXP_TXN[5]	
B16	VSS	
B17	EXP_COMP[1]	
B18	VCC33	
B19	RESERVED	
B20	SMBUS[2]	
B21	HPA_SLOT[1]	HAPRSNT1_1_N
B22	HPA_SOC	HAPCIXCAP2_2
B23	PAIRQ_N[12]	HAM66EN_2
B24	PAIRQ_N[4]	
C1	NC_PXHV_C1	
C2	VSS	
C3	STRAP_PXHV_9	HBM66EN_1
C4	NC_PXHV_C4	HBBUTTON2_N
C5	VSS	
C6	RESERVED	
C7	SCLK	
C8	VSS	
C9	EXP_RXP[2]	
C10	EXP_RXP[3]	
C11	EXP_RXN[3]	
C12	VCCEXP	
C13	EXP_RXP[5]	
C14	VCCBGEXP	
C15	VCCEXP	
C16	EXP_CLK_P	
C17	EXP_CLK_N	
C18	PASTRAP0	
C19	RESERVED	
C20	VSS	
C21	HPA_SLOT[0]	HAMRL_2_N
C22	VCC33	
C23	VSS	
C24	PAIRQ_N[3]	
D1	STRAP_PXHV_10	HBM66EN_2

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 3 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
D2	NC_PXHV_D2	
D3	NC_PXHV_D3	HBPCIXCAP2_1
D4	STRAP_PXHV_6	
D5	VCC33	
D6	NC_PXHV_D6	HBCLKEN_2_N
D7	STRAP_PXHV_12	
D8	SDTA	
D9	EXP_TXP[1]	
D10	EXP_TXN[1]	
D11	VSS	
D12	EXP_RXN[1]	
D13	EXP_RXN[5]	
D14	VSS	
D15	EXP_TXP[6]	
D16	EXP_TXN[6]	
D17	VSS	
D18	RESERVED	
D19	NC_PXHV_D19	
D20	SMBUS[5]	
D21	HPA_SLOT[2]	
D22	PAIRQ_N[9]	HAPCIXCAP2_1
D23	PAIRQ_N[2]	
D24	PAIRQ_N[6]	
E1	NC_PXHV_E1	
E2	VSS	
E3	NC_PXHV_E3	HBPWRFLT_1_N
E4	NC_PXHV_E4	
E5	VSS	
E6	STRAP_PXHV_1	HBPWRLED2_N
E7	TMS	
E8	VSS	
E9	TDI	
E10	VSS	
E11	EXP_TXN[0]	
E12	EXP_RXP[1]	
E13	VSS	
E14	EXP_RXP[7]	

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 4 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
E15	EXP_RXN[7]	
E16	EXP_COMP[0]	
E17	PAPCIXCAP	
E18	HPA_PRST_N	HPA_RST1_N
E19	HPA_SIL_N	HACLKEN_1_N
E20	VSS	
E21	PAIRQ_N[15]	HAMRL1_N
E22	PAIRQ_N[13]	HAPWRFLT_2_N
E23	VSS	
E24	VCC33	
F1	VCC33	
F2	NC_PXHV_F2	
F3	NC_PXHV_F3	
F4	NC_PXHV_F4	HBMRL1_N
F5	STRAP_PXHV_7	HBPWRLED1_N
F6	NC_PXHV_F6	HBCLKEN_1_N
F7	NC_PXHV_F7	
F8	NC_PXHV_F8	HPB_RST1_N
F9	TRST_N	
F10	EXP_RXN[0]	
F11	EXP_TXP[0]	
F12	VCCEXP	
F13	EXP_TXP[7]	
F14	EXP_TXN[7]	
F15	VSS	
F16	VSSAEXP	
F17	PWROK	
F18	HPA_RST2_N	
F19	HPA_SID	HAPCIXCAP1_2
F20	HPA_SLOT[3]	HAPWRLED1_N
F21	PAIRQ_N[14]	HAPWRFLT_1_N
F22	PAIRQ_N[11]	HAM66EN_1
F23	PAIRQ_N[7]	
F24	PAIRQ_N[1]	
G1	NC_PXHV_G1	
G2	VSS	
G3	NC_PXHV_G3	HBBUTTON_1_N

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 5 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
G4	NC_PXHV_G4	HBPWRFLT_2_N
G5	VSS	
G6	NC_PXHV_G6	
G7	NC_PXHV_G7	
G8	VSS	
G9	NC_PXHV_G9	
G10	EXP_RXP[0]	
G11	VSS	
G12	EXP_RXP[4]	
G13	EXP_TXN[4]	
G14	VSS	
G15	VCCAEXP	
G16	SMBUS[1]	
G17	VSS	
G18	HPA_SOD	HACLKEN_2_N
G19	HPA_SOLR	HAAATNLED2_N
G20	VSS	
G21	PAIRQ_N[8]	HABUTTON_1_N
G22	PAIRQ_N[10]	HAPCIXCAP1_1
G23	VSS	
G24	PAIRQ_N[0]	
H1	NC_PXHV_H1	
H2	NC_PXHV_H2	
H3	VCC33	
H4	NC_PXHV_H4	
H5	NC_PXHV_H5	
H6	VSS	
H7	NC_PXHV_H7	
H8	NC_PXHV_H8	
H9	NC_PXHV_H9	
H10	VSS	
H11	VCCEXP	
H12	EXP_RXN[4]	
H13	EXP_TXP[4]	
H14	VSS	
H15	VCCEXP	
H16	RSTIN_N	

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 6 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
H17	PACBE_N[4]	
H18	VCC33	
H19	PACBE_N[6]	
H20	PACBE_N['7]	
H21	VCC33	
H22	PAAD[49]	
H23	PAAD[48]	
H24	VCC33	
J1	VSS	
J2	NC_PXHV_H2	
J3	NC_PXHV_J3	
J4	VSS	
J5	NC_PXHV_J5	
J6	NC_PXHV_J6	
J7	NC_PXHV_J7	
J8	VCCAPCI[2]	
J9	VSS	
J10	VCCEXP	
J11	VSS	
J12	VCCEXP	
J13	VSS	
J14	VCCEXP	
J15	VSS	
J16	VCC15	
J17	PAAD[63]	
J18	PACBE_N[5]	
J19	VSS	
J20	PAPAR64	
J21	PAAD[47]	
J22	VSS	
J23	PAAD[46]	
J24	PAGNT_N[1]	
K3	NC_PXHV_K3	
K4	NC_PXHV_K4	
K5	VSS	
K6	NC_PXHV_K6	
K7	NC_PXHV_K7	

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 7 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
K8	VSS	
K9	VCC15	
K10	VSS	
K11	VCC	
K12	VSS	
K13	VCC	
K14	VSS	
K15	VCC	
K16	VSS	
K17	PAAD[61]	
K18	PAAD[60]	
K19	PAAD[62]	
K20	VSS	
K21	HAPWREN_1	
K22	PAAD[45]	
K23	VSS	
K24	PAAD[44]	
L1	NC_PXHV_L1	
L2	NC_PXHV_L2	
L3	VCC15	
L4	NC_PXHV_L4	
L5	NC_PXHV_L5	
L6	VCC33	
L7	NC_PXHV_L7	
L8	NC_PXHV_L8	HBBUSEN_1_N
L9	VSS	
L10	VCC	
L11	VSS	
L12	VCC	
L13	VSS	
L14	VCC	
L15	VSS	
L16	VCC15	
L17	PAAD[59]	
L18	VSS	
L19	PAAD[58]	
L20	PAAD[43]	

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 8 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
L21	VSS	
L22	PAREQ_N[4]	HAPRSNT2_2_N
L23	PAAD[42]	
L24	VSS	
M2	NC_PXHV_M2	
M3	NC_PXHV_M3	
M4	VSS	
M5	NC_PXHV_M5	
M6	NC_PXHV_M6	
M7	VSS	
M8	NC_PXHV_M8	
M9	VCC15	
M10	VSS	
M11	VCC	
M12	VSS	
M13	VCC	
M14	VSS	
M15	VCC	
M16	VSS	
M17	PAAD[57]	
M18	PAAD[56]	
M19	VCC33	
M20	RESERVED	
M21	PAAD[41]	
M22	VCC15	
M23	PAAD[40]	
N2	VSS	
N3	NC_PXHV_N3	
N4	NC_PXHV_N4	
N5	VSS	
N6	NC_PXHV_N6	
N7	NC_PXHV_N7	
N8	NC_PXHV_N8	
N9	VSS	
N10	VCC	
N11	VSS	
N12	VCC	

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 9 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
N13	VSS	
N14	VCC	
N15	VSS	
N16	VCC15	
N17	PAAD[55]	
N18	PAREQ_N[3]	HAPRSNT2_1_N
N19	PAAD[54]	
N20	VSS	
N21	PAAD[39]	
N22	PAAD[38]	
N23	VSS	
P1	NC_PXHV_P1	
P2	STRAP_PXHV_8	
P3	VSS	
P4	NC_PXHV_P4	
P5	NC_PXHV_P5	
P6	VSS	
P7	NC_PXHV_P7	
P8	NC_PXHV_P8	
P9	VCC15	
P10	VSS	
P11	VCC	
P12	VSS	
P13	VCC	
P14	VSS	
P15	VCC	
P16	VSS	
P17	PAAD[53]	
P18	VSS	
P19	PAAD[52]	
P20	PAPERR_N	
P21	VSS	
P22	PAAD[37]	
P23	PAAD[36]	
P24	VSS	
R1	VSS	
R2	NC_PXHV_R2	

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 10 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
R3	NC_PXHV_R3	
R4	VSS	
R5	STRAP_PXHV_14	
R6	HBPWREN_1	
R7	VCC33	
R8	VCCAPCI[1]	
R9	VSS	
R10	VCC	
R11	VSS	
R12	VCC	
R13	VSS	
R14	VCC	
R15	VSS	
R16	VCC15	
R17	VCCAPCI[0]	
R18	PAAD[51]	
R19	VSS	
R20	PAAD[50]	
R21	PAPLOCK_N	
R22	VSS	
R23	PAAD[35]	
R24	PAAD[34]	
T1	NC_PXHV_T1	HBPRSNT2_1_N
T2	VSS	
T3	NC_PXHV_T3	
T4	NC_PXHV_T4	
T5	VCC33	
T6	NC_PXHV_T6	
T7	NC_PXHV_T7	
T8	VSS	
T9	VCC15	
T10	VSS	
T11	VCC15	
T12	VSS	
T13	VCC15	
T14	VSS	
T15	VCC15	

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 11 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
T16	VSS	
T17	VCC33	
T18	PAM66EN	
T19	PASERR_N	
T20	VCC33	
T21	PAAD[33]	
T22	PAAD[32]	
T23	VCC33	
T24	HAATNLED_1_N	
U1	STRAP_PXHV_11	
U2	NC_PXHV_U2	
U3	VSS	
U4	NC_PXHV_U4	
U5	NC_PXHV_U5	
U6	VSS	
U7	NC_PXHV_U7	
U8	NC_PXHV_U8	
U9	VCC33	
U10	STRAP_PXHV_13	
U11	RESERVED	
U12	VSS	
U13	PAPCLKI	
U14	PAPCLKO[4]	
U15	VSS	
U16	PAPCLKO[5]	
U17	PAPCLKO[3]	
U18	VSS	
U19	PASTOP_N	
U20	PADEVSEL_N	
U21	VSS	
U22	PATRDY_N	
U23	PAGNT_N[5]	HABUSEN_1_N
U24	VSS	
V1	VSS	
V2	NC_PXHV_V2	
V3	NC_PXHV_V3	
V4	VCC33	

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 12 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
V5	NC_PXHV_V5	HBPRSNT2_2_N
V6	NC_PXHV_V6	
V7	VSS	
V8	NC_PXHV_V8	
V9	NC_PXHV_V9	
V10	VSS	
V11	RCOMP	
V12	VREFPCI	
V13	VSS	
V14	PAPCLKO[0]	
V15	PAPCLKO[6]	
V16	VCC15	
V17	PAPCLKO[2]	
V18	PAREQ_N[2]	
V19	VSS	
V20	PA133EN	
V21	PAPME_N	
V22	VSS	
V23	PAFRAME_N	
V24	PAIRDY_N	
W1	NC_PXHV_W1	
W2	VCC33	
W3	NC_PXHV_W3	
W4	NC_PXHV_W4	
W5	VSS	
W6	NC_PXHV_W6	
W7	NC_PXHV_W7	
W8	VSS	
W9	NC_PXHV_W9	
W10	NC_PXHV_W10	
W11	VCC33	
W12	NC_PXHV_W12	HBBUSEN_2_N
W13	PAREQ_N[5]	HAPRSNT1_2_N
W14	VSS	
W15	PAAD[30]	
W16	PAPCLKO[1]	
W17	VSS	

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 13 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
W18	PAAD[25]	
W19	PAGNT_N[0]	
W20	VSS	
W21	PAREQ_N[0]	
W22	PAREQ_N[1]	
W23	VSS	
W24	PAAD[16]	
Y1	NC_PXHV_Y1	
Y2	NC_PXHV_Y2	
Y3	VSS	
Y4	NC_PXHV_Y4	
Y5	NC_PXHV_Y5	
Y6	VCC15	
Y7	NC_PXHV_Y7	
Y8	NC_PXHV_Y8	
Y9	VCC33	
Y10	NC_PXHV_Y10	
Y11	NC_PXHV_Y11	
Y12	VSS	
Y13	PAGNT_N[3]	HAPWREN_2
Y14	PAGNT_N[2]	
Y15	VCC33	
Y16	PAAD[28]	
Y17	PAAD[27]	
Y18	VSS	
Y19	PAAD[23]	
Y20	PAAD[22]	
Y21	VCC33	
Y22	PAAD[19]	
Y23	PAAD[17]	
Y24	VCC33	
AA1	VCC33	
AA2	NC_PXHV_AA2	
AA3	NC_PXHV_AA3	
AA4	VSS	
AA5	NC_PXHV_AA5	
AA6	NC_PXHV_AA6	

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 14 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
AA7	VSS	
AA8	NC_PXHV_AA8	
AA9	NC_PXHV_AA9	
AA10	VSS	
AA11	NC_PXHV_AA11	HBPWREN_2
AA12	NC_PXHV_AA12	HBPRSNT1_2_N
AA13	VSS	
AA14	PAGNT_N[4]	HABUSEN_2_N
AA15	PAAD[31]	
AA16	VSS	
AA17	PAPCIRST_N	
AA18	PAAD[26]	
AA19	VSS	
AA20	PACBE_N[3]	
AA21	PAAD[21]	
AA22	VSS	
AA23	PAAD[18]	
AA24	PACBE_N[2]	
AB1	NC_PXHV_AB1	
AB2	VSS	
AB3	NC_PXHV_AB3	
AB4	NC_PXHV_AB4	
AB5	VSS	
AB6	NC_PXHV_AB6	
AB7	NC_PXHV_AB7	
AB8	VCC33	
AB9	NC_PXHV_AB9	
AB10	NC_PXHV_AB10	
AB11	VSS	
AB12	NC_PXHV_AB12	
AB13	PAPAR	
AB14	VCC33	
AB15	PAAD[12]	
AB16	PAAD[29]	
AB17	VSS	
AB18	PAAD[8]	
AB19	PAAD[24]	

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 15 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
AB20	VCC15	
AB21	PAAD[3]	
AB22	PAAD[20]	
AB23	VSS	
AB24	PAACK64_N	
AC1	NC_PXHV_AC1	
AC2	NC_PXHV_AC2	
AC3	VCC15	
AC4	NC_PXHV_AC4	
AC5	NC_PXHV_AC5	
AC6	VCC33	
AC7	NC_PXHV_AC7	
AC8	NC_PXHV_AC8	
AC9	VSS	
AC10	NC_PXHV_AC10	
AC11	NC_PXHV_AC11	
AC12	VSS	
AC13	PAAD[15]	
AC14	PACBE_N[1]	
AC15	VSS	
AC16	PAAD[11]	
AC17	PAAD[9]	
AC18	VSS	
AC19	PAAD[7]	
AC20	PAAD[5]	
AC21	VSS	
AC22	PAAD[2]	
AC23	PAAD[0]	
AC24	PAREQ64_N	
AD1	VSS	
AD2	NC_PXHV_AD2	
AD3	NC_PXHV_AD3	
AD4	VSS	
AD5	NC_PXHV_AD5	
AD6	NC_PXHV_AD6	
AD7	VSS	
AD8	NC_PXHV_AD8	

Table 6-2. Intel® 6702PXH 64-bit PCI Hub Signal List (Sorted by Pin Number) (Sheet 16 of 16)

Pin#	Intel® 6702PXH 64-bit PCI Hub	Parallel HP Mux
AD9	NC_PXHV_AD9	
AD10	VSS	
AD11	NC_PXHV_AD11	
AD14	PAAD[14]	
AD15	PAAD[13]	
AD16	VSS	
AD17	PAAD[10]	
AD18	NC	
AD19	VCC33	
AD20	PAAD[6]	
AD21	PAAD[4]	
AD22	VSS	
AD23	PAAD[1]	
AD24	VSS	

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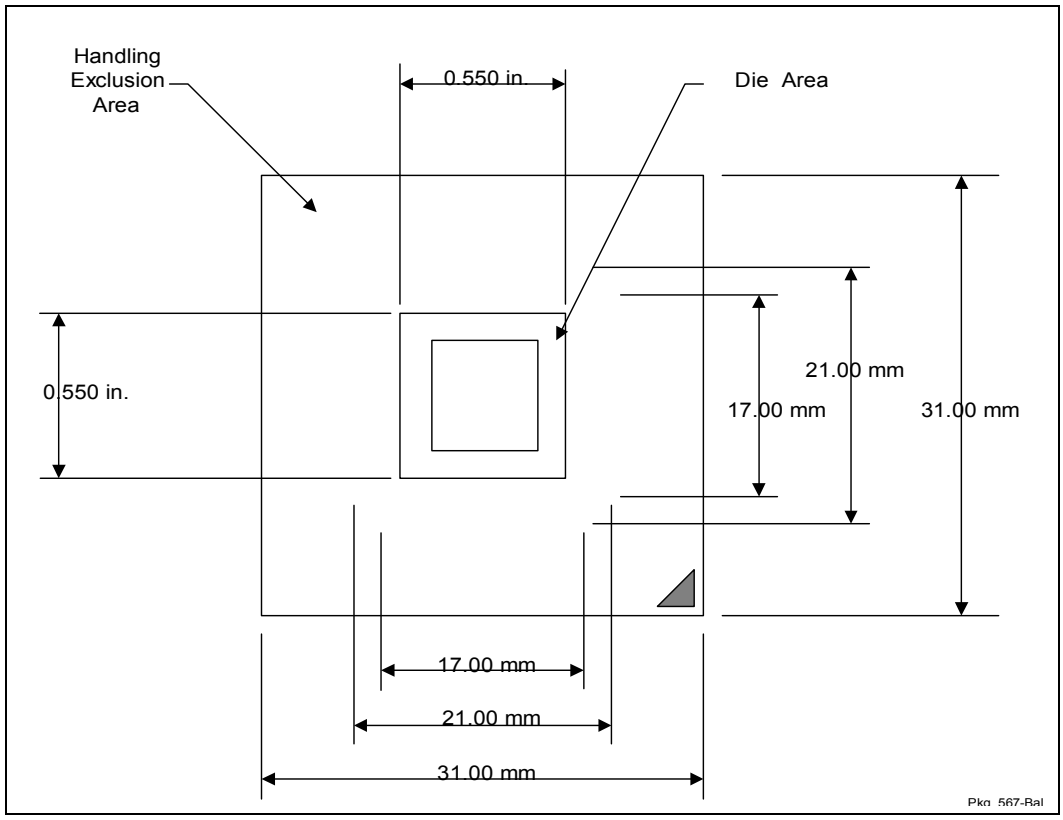
7 Mechanical Specifications

Figure 7-1. Top View – Intel® 6702PXH 64-bit PCI Hub 567-Ball FCBGA Package Dimensions



The Intel® 6702PXH 64-bit PCI Hub and Intel® 6702PXH 64-bit PCI Hub are pin compatible and share the same package dimensions. The Intel® 6702PXH 64-bit PCI Hub is a 567-ball FCBGA package, 31 mm X 31 mm in size, with a 1.27 mm ball pitch.

Figure 7-2. Bottom View – Intel® 6702PXH 64-bit PCI Hub 567-Ball FCBGA Package Dimensions

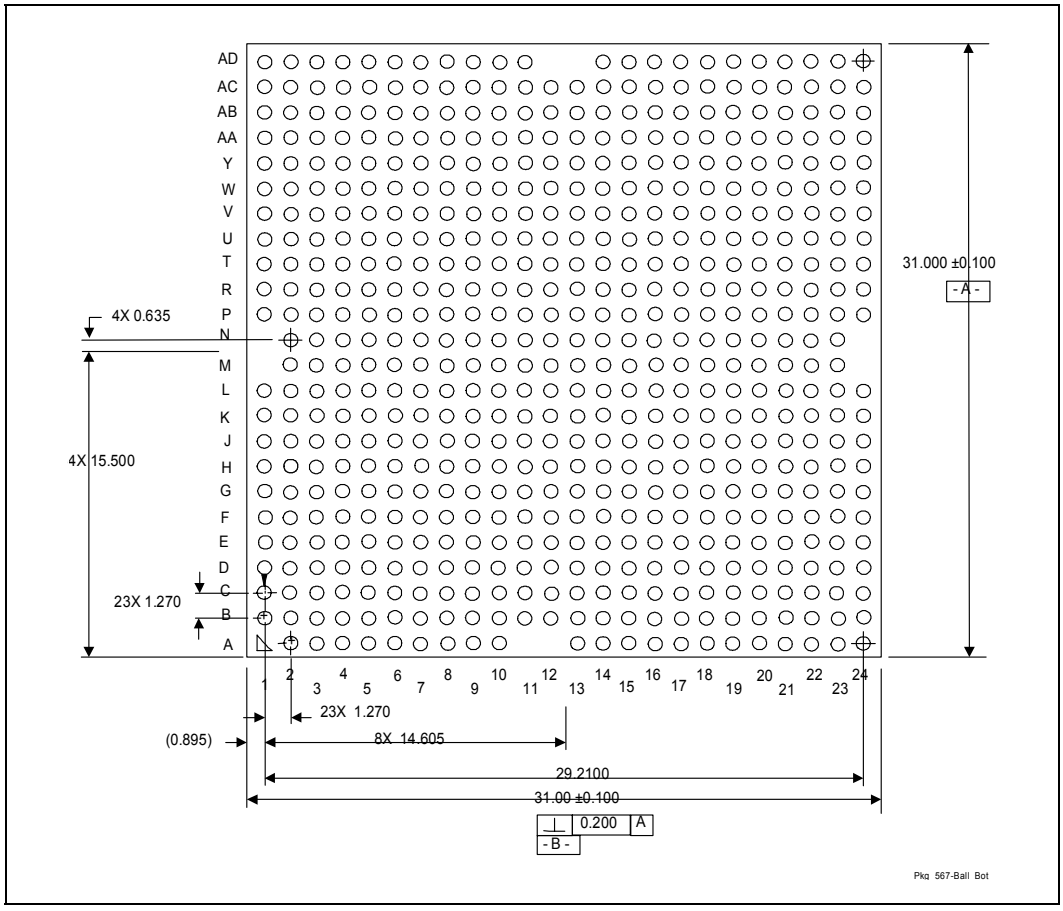
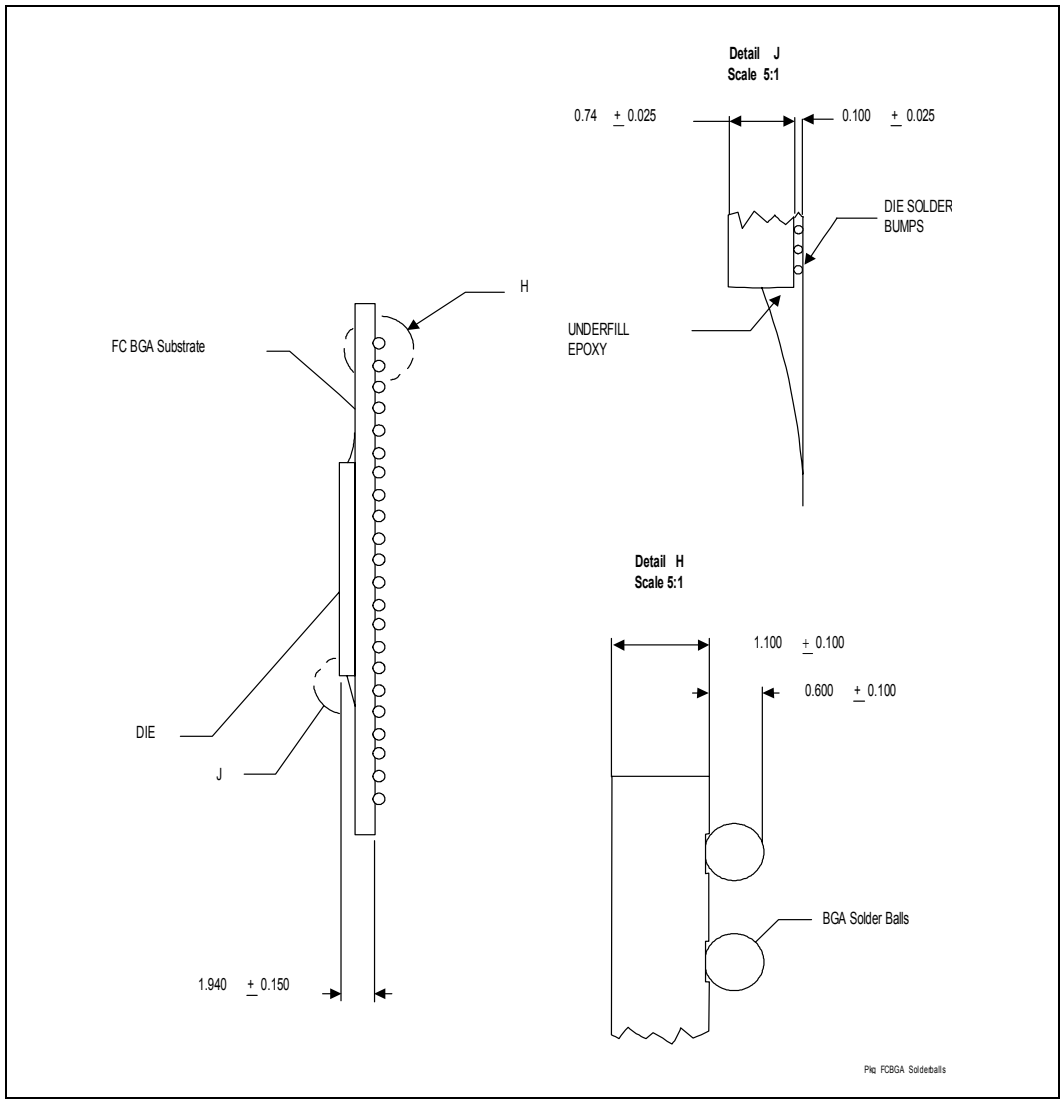


Figure 7-3. Side View – Intel® 6702PXH 64-bit PCI Hub 567-Ball FCBGA Package Dimensions



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