NEC

MOS INTEGRATED CIRCUIT

μPD30671

VR7701

64-/32-BIT MICROPROCESSOR

DESCRIPTION

The μPD30671 (VR7701) is a member of the VR™ Series of RISC (Reduced Instruction Set Computer) microprocessors. It is a high-performance 64-/32-bit microprocessor that employs the RISC architecture developed by MIPS™.

The VR7701 has a VR5500 core as the CPU. It is also equipped with many peripheral units such as a secondary cache, 64-bit DDR SDRAM memory controller, 64-bit PCI-X, 10/100 BASE Ethernet™ controller (MAC), LocalBus interface, interrupt controller, serial controller, and timer.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.

- **VR7701 User's Manual (U16334E)**

FEATURES

- Employs VR5500 core, a 64-bit RISC core, as CPU.
  - High-speed operation processing with 2-way superscalar super pipeline
  - 804 MIPS at 400 MHz operation
  - Conforms to MIPS I, II, III, and IV instruction sets. Also supports some of MIPS64 instructions.
  - High-speed translation lookaside buffer (TLB) (48 double entries)
  - On-chip floating-point unit (FPU)
  - On-chip primary cache memory
    Instruction/data: 32 KB each
    2-way set associative cache
  - On-chip hardware debug function (N-Wire)
- On-chip secondary cache memory
  - 256 KB 4-way set associative cache
  - Instruction/data mixed
  - ★ Supports freeze control.
- SDRAM interface
  - DDR SDRAM
  - Supports 64/128/256/512 Mb/1 Gb SDRAM.
  - Operating frequency: 133 MHz
- LocalBus interface
  - 32-bit address/data multiplexed bus
  - Address space: 25 bits (128 MB)
  - 4-channel I/O DMA interface
- PCI-X interface
  - Conforms to 64-bit PCI-X Rev. 1.0a (133 MHz MAX.).
  - PCI mode (PCI Rev. 2.2, 33 MHz MAX.) selectable
- Ethernet controller
  - 10/100 BASE MAC and MII (2 channels each)
  - Operating frequency: 2.5 MHz, 25 MHz
- On-chip peripheral units
  - Timer (9 channels)
  - Interrupt controller
  - 16550-compatible serial interface (2 channels)
  - Clocked serial interface
- Supply voltage
  Core block: 1.48 to 1.64 V
  I/O block: 3.14 to 3.47 V, 2.3 to 2.7 V

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Document No. U16395EJ2V0DS00 (2nd edition)
Date Published August 2003 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

APPLICATIONS

- Disk array equipment
- High-end set-top boxes
- Network equipment, etc.

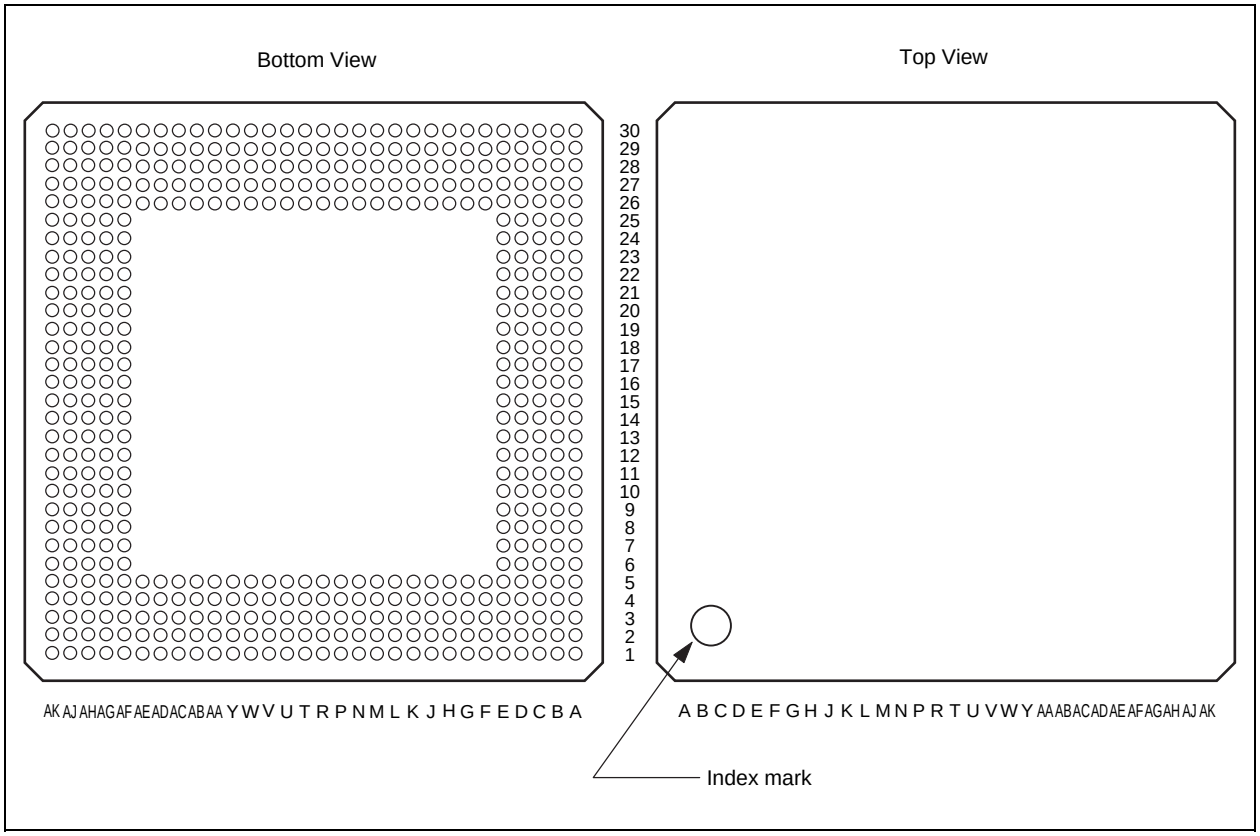
ORDERING INFORMATION

Part Number	Package	Maximum Operating Frequency
★ μPD30671F2-400-UA5-A[Note]	500-pin plastic BGA (C/D advanced type) (40 × 40)	400 MHz

★ **Note** Lead-free product

PIN CONFIGURATION

- 500-pin plastic BGA (C/D advanced type) (40 × 40)



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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	GND	B9	PAD26	C17	PIRDY#
A2	GND	B10	PAD21	C18	PSTOP#
A3	VD3	B11	GND	C19	PPAR64
A4	PAD43	B12	PAD14	C20	MMD0
A5	PAD40	B13	PAD9	C21	MMD1
A6	PAD35	B14	VD3	C22	MMD7
A7	PAD31	B15	PAD1	C23	MMD9
A8	PAD28	B16	PREQ2#	C24	MDQS1
A9	PAD23	B17	VD3	C25	MMD11
A10	PAD19	B18	PACK64#	C26	MDQS2
A11	PAD18	B19	PDEVSEL#	C27	MMD23
A12	PAD13	B20	GND	C28	VD2
A13	PAD8	B21	MMD5	C29	MVref0
A14	PAD5	B22	MMD6	C30	MMD25
A15	PAD0	B23	VDD	D1	PAD58
A16	PREQ1#	B24	SDLLE1V	D2	PAD56
A17	PREQ0#	B25	MMD14	D3	PAD53
A18	PFRAME#	B26	GND	D4	PAD48
A19	PTRDY#	B27	MDQM2	D5	VDD
A20	MCLKIN	B28	MMD19	D6	PAD44
A21	MCLKIN#	B29	GND	D7	PAD39
A22	MDQS0	B30	GND	D8	GND
A23	MMD3	C1	GND	D9	PAD30
A24	MMD13	C2	PAD52	D10	PAD25
A25	MDQM1	C3	PAD47	D11	VD3
A26	MMD16	C4	VD3	D12	PAD16
A27	MMD17	C5	PAD46	D13	PAD11
A28	VD2	C6	PAD41	D14	GND
A29	GND	C7	PAD36	D15	PAD3
A30	GND	C8	PAD34	D16	YPLLGND1
B1	PAD50	C9	PAD29	D17	GND
B2	PAD51	C10	PAD24	D18	MDLLVDD
B3	VDD	C11	PAD20	D19	PPAR
B4	PAD45	C12	PAD15	D20	VD2
B5	GND	C13	PAD10	D21	MDQM0
B6	PAD38	C14	PAD6	D22	MMD8
B7	PAD33	C15	PAD2	D23	GND
B8	VDD	C16	YPLLVDD1	D24	MMD15

Remark # indicates active low.

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
D25	MMD21	F3	PAD59	K1	PPERR#
D26	MMD22	F4	VD3	K2	VDD
D27	VDD	F5	PAD55	K3	PINTD#
D28	MMD24	F26	MMD29	K4	GND
D29	GND	F27	MMD26	K5	PREQ64#
D30	MDQS3	F28	MMD27	K26	IC-PDnR
E1	PCBE2#	F29	MMDP4	K27	IC-PDnR
E2	PAD61	F30	MMDP1	K28	IC-PDnR
E3	PAD57	G1	PCBE5#	K29	IC-PDnR
E4	PAD54	G2	GND	K30	MMA14
E5	PAD49	G3	PCBE0#	L1	PCIFREQ0
E6	GND	G4	PAD62	L2	PCIBUS64
E7	PAD42	G5	PAD60	L3	PRST#
E8	PAD37	G26	MMD30	L4	PINTB#
E9	PAD32	G27	MMDP0	L5	PINTC#
E10	PAD27	G28	MDQSP	L26	IC-PDnR
E11	PAD22	G29	MMDP2	L27	VD2
E12	PAD17	G30	MMDP7	L28	IC-PDnR
E13	PAD12	H1	PGNT2#	L29	SDLLN1V
E14	PAD7	H2	PGNT0#	L30	MMA13
E15	PAD4	H3	PCBE6#	M1	JTDI
E16	PREQ3#	H4	PCBE4#	M2	PCIMODE
E17	YPLLGND2	H5	PCBE1#	M3	PCIFREQ1
E18	YPLLVDD2	H26	MMDP5	M4	HOSTMODE
E19	PCLKIN	H27	GND	M5	PINTA#
E20	MMD4	H28	MDQM8	M26	MCKE3
E21	MMD2	H29	VDD	M27	MCKE2
E22	MMD12	H30	IC-PDnR	M28	MCKE1
E23	MMD10	J1	IDSEL	M29	MCKE0
E24	MMD20	J2	PSERR#	M30	MMA12
E25	MMD18	J3	PGNT3#	N1	JTMS
E26	VD2	J4	PGNT1#	N2	JTDO
E27	MMD28	J5	PCBE7#	N3	SPLLVDD
E28	MDQM3	J26	MMDP6	N4	JTCK
E29	GND	J27	MMDP3	N5	SPLLGND
E30	MMD31	J28	IC-PDnR	N26	MMA11
F1	PCBE3#	J29	IC-PDnR	N27	MMA9
F2	PAD63	J30	IC-PDnR	N28	MMA7

Remark # indicates active low.

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
N29	MMA8	U27	GND	AA5	LAD1
N30	MMA5	U28	MWE#	AA26	IC-PDnR
P1	NTrcData1	U29	VD2	AA27	IC-PDnR
P2	NTrcData0	U30	MCAS#	AA28	IC-PDnR
P3	NTrcClk	V1	DEVMEM0	AA29	IC-PDnR
P4	VD3	V2	DEVCPU2	AA30	IC-PDnR
P5	JTRST#	V3	TCLKIN	AB1	LAD0
P26	MMA6	V4	DEVCPU0	AB2	LAD2
P27	GND	V5	DEVCPU1	AB3	LAD3
P28	MMA4	V26	MCS5#	AB4	LAD5
P29	VD2	V27	MCS3#	AB5	LAD7
P30	MMA3	V28	MCS2#	AB26	IC-PDnR
R1	NMI	V29	MCS1#	AB27	IC-PDnR
R2	BKTGIO#	V30	MCS4#	AB28	IC-PDnR
R3	NTrcEnd	W1	IC-PDnR	AB29	IC-PDnR
R4	NTrcData2	W2	DEVLC1	AB30	IC-PDnR
R5	NTrcData3	W3	DEVMEM1	AC1	LAD4
R26	N.C.	W4	DEVLC0	AC2	LAD6
R27	N.C.	W5	IC-PUpR	AC3	LAD8
R28	IC-PDnR	W26	IC-PDnR	AC4	LAD10
R29	MMA2	W27	IC-PDnR	AC5	LAD12
R30	MMA1	W28	MCS7#	AC26	MMD36
T1	INTP4/GP54	W29	MCS6#	AC27	GND
T2	INTP3/GP53	W30	IC-PDnR	AC28	IC-PDnR
T3	INTP2/GP52	Y1	IC-PDnR	AC29	VDD
T4	INTP0/GP50	Y2	IC-PDnR	AC30	IC-PDnR
T5	INTP1/GP51	Y3	BIGENDIAN	AD1	LAD9
T26	MMBA1	Y4	OOOMode	AD2	LAD11
T27	MMA10	Y5	IC-PDnR	AD3	LAD13
T28	MMA0	Y26	IC-PDnR	AD4	LAD15
T29	MMBA0	Y27	VD2	AD5	LAD17
T30	MRAS#	Y28	IC-PDnR	AD26	MMD34
U1	INTP7/GP57	Y29	SDLLN2V	AD27	MMD33
U2	GND	Y30	IC-PDnR	AD28	MMD32
U3	INTP6/GP56	AA1	N.C.	AD29	IC-PDnR
U4	VD3	AA2	VDD	AD30	IC-PDnR
U5	INTP5/GP55	AA3	IC-PDnR	AE1	LAD14
U26	MCS0#	AA4	GND	AE2	GND

Remark # indicates active low.

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
AE3	LAD18	AG1	LAD20	AH9	MI1TXEN/GP1
AE4	VD3	AG2	LAD22	AH10	MI1TXER/GP6
AE5	LAD23	AG3	LAD24	AH11	MI1RXDV/GP10
AE26	VDD	AG4	VD3	AH12	MI1RXER/GP15
AE27	MMD39	AG5	LAD30	AH13	MI2TXD0/GP20
AE28	MDQM4	AG6	LCS2#	AH14	MI2TXER/GP24
AE29	GND	AG7	LWR#	AH15	MI2RXD0/GP29
AE30	MMD37	AG8	GND	AH16	MI2MDCLK/GP34
AF1	LAD16	AG9	N.C.	AH17	UARTCLK
AF2	LAD19	AG10	MI1TXD3/GP5	AH18	U1CTS/GP39
AF3	LAD21	AG11	VD3	AH19	U2TXD/GP44
AF4	LAD25	AG12	MI1RXD3/GP14	AH20	U2DSR/GP49
AF5	VDD	AG13	MI2TXEN/GP19	AH21	MMD59
AF6	LALE	AG14	GND	AH22	MDQM7
AF7	LCS6#	AG15	MI2RXDV/GP28	AH23	MMD51
AF8	LBT16#	AG16	MI2RXER/GP33	AH24	MMD55
★ AF9	IC-PUpR	AG17	GND	AH25	MMD49
AF10	MI1TXD2/GP4	AG18	U1DTR/CSI_DO/GP40	AH26	MMD43
AF11	MI1RXCLK/GP9	AG19	U2RTS/GP45	AH27	MDQS5
AF12	MI1RXD1/GP12	AG20	VD2	AH28	MMD40
AF13	MI1MD/GP17	AG21	MMD63	AH29	VDD
AF14	MI2TXD2/GP22	AG22	MMD57	AH30	VD2
AF15	MI2RXCLK/GP27	AG23	GND	AJ1	GND
AF16	MI2RXD3/GP32	AG24	MDQM6	AJ2	GND
AF17	U1RXD/GP36	AG25	MMD48	AJ3	LAD28
AF18	U1DCD/CSI_DI/GP41	AG26	MMD42	AJ4	LAD31
AF19	U2CTS/GP46	AG27	MMD44	AJ5	GND
AF20	VDDOK	AG28	GND	AJ6	LRD#
AF21	MMD62	AG29	MVref1	AJ7	LRDY#
AF22	MMD61	AG30	MMD38	AJ8	VD3
AF23	MMD54	AH1	LAD26	AJ9	MI1TXD0/GP2
AF24	MMD53	AH2	LAD27	AJ10	MI1COL/GP7
AF25	MMD46	AH3	VDD	AJ11	GND
AF26	MMD45	AH4	LAD29	AJ12	MI1MDCLK/GP16
AF27	VD2	AH5	LCS1#	AJ13	MI2TXD1/GP21
AF28	MMD35	AH6	LCS3#	AJ14	VDD
AF29	VD2	AH7	MI1TXCLK/GP0	AJ15	MI2CRS/GP26
AF30	MDQS4	AH8	LDRQ0	AJ16	MI2RXD2/GP31

Remark # indicates active low.

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
AJ17	VD3	AK2	GND	AK17	MI2MD/GP35
AJ18	U1RTS/GP38	AK3	VD3	AK18	U1TXD/GP37
AJ19	U2RXD/GP43	AK4	LCS4#	AK19	U1DSR/CSI_CLK/GP42
AJ20	GND	AK5	LCS5#	AK20	U2DTR/GP47
★ AJ21	RESET#	AK6	IC-PUpR	AK21	U2DCD/GP48
AJ22	MMD58	AK7	LBCLKOUT	AK22	COLDRESET#
AJ23	VD2	AK8	LDRQ1	AK23	MDQS7
AJ24	MMD56	AK9	MI1TXD1/GP3	AK24	MMD60
AJ25	MDQS6	AK10	MI1CRS/GP8	AK25	MMD50
AJ26	SDLLW1V	AK11	MI1RXD0/GP11	AK26	MMD52
AJ27	VD2	AK12	MI1RXD2/GP13	AK27	MMD47
AJ28	MMD41	AK13	MI2TXCLK/GP18	AK28	MDQM5
AJ29	GND	AK14	MI2TXD3/GP23	AK29	GND
AJ30	GND	AK15	MI2COL/GP25	AK30	GND
AK1	GND	AK16	MI2RXD1/GP30		

Remark # indicates active low.

Pin Identification (1/2)

BIGENDIAN:	Big endian	MDQS(7:0):	SDRAM data strobe
BKTGIO#:	Break/trigger input/output	MDQSP:	SDRAM data parity strobe
COLDRESET#:	Cold reset	MI1COL:	MII channel 1 collision
CSI_CLK:	CSI clock	MI1CRS:	MII channel 1 carrier sense
CSI_DI:	CSI serial data input	MI1MD:	MII channel 1 management data
CSI_DO:	CSI serial data output	MI1MDCLK:	MII channel 1 management clock
DEVCPU(2:0):	Divide mode for CPU	MI1RXCLK:	MII channel 1 receive clock
DEVLC(1:0):	Divide mode for LocalBus	MI1RXD(3:0):	MII channel 1 receive data
DEVMEM(1:0):	Divede mode for SDRAM	MI1RXDV:	MII channel 1 receive data valid
GND:	Ground	MI1RXER:	MII channel 1 receive error
GP(57:0):	General purpose I/O	MI1TXCLK:	MII channel 1 transmit clock
HOSTMODE:	PCI-X host mode	MI1TXD(3:0):	MII channel 1 transmit data
★ IC-PDnR:	Pull-down with resistor	MI1TXEN:	MII channel 1 transmit enable
★ IC-PUpR:	Pull-up with resistor	MI1TXER:	MII channel 1 transmit error
IDSEL:	PCI-X initialization device select	MI2COL:	MII channel 2 collision
INTP(7:0):	Interrupt	MI2CRS:	MII channel 2 carrier sense
JTCK:	JTAG clock	MI2MD:	MII channel 2 management data
JTDI:	JATG data input	MI2MDCLK:	MII channel 2 management clock
JTDO:	JTAG data output	MI2RXCLK:	MII channel 2 receive clock
JTMS:	JTAG mode select	MI2RXD(3:0):	MII channel 2 receive data
JTRST#:	JTAG reset	MI2RXDV:	MII channel 2 receive data valid
LAD(31:0):	LocalBus address/data bus	MI2RXER:	MII channel 2 receive error
LALE:	LocalBus address latch enable	MI2TXCLK:	MII channel 2 transmit clock
LBCLKOUT:	LocalBus clock output	MI2TXD(3:0):	MII channel 2 transmit data
LBT16#:	LocalBus boot size	MI2TXEN:	MII channel 2 transmit enable
LCS(6:1)#:	LocalBus chip select	MI2TXER:	MII channel 2 transmit error
LDRQ0:	LocalBus channel 0 DMA request	MMA(14:0):	SDARM address
LDRQ1:	LocalBus channel 1 DMA request	MMBA(1:0):	SDRAM bank address
LRD#:	LocalBus read	MMD(63:0):	SDRAM data bus
LRDY#:	LocalBus ready	MMDP(7:0):	SDRAM data bus parity
LWR#:	LocalBus write	MRAS#:	SDRAM row address strobe
MCAS#:	SDRAM column address strobe	MVref(1:0):	SDRAM Vref
MCKE(3:0):	SDRAM clock enable	MWE#:	SDRAM write enable
MCLKIN:	SDRAM clock input	N.C.:	No connection
MCLKIN#:	SDRAM clock input	NMI:	Non-maskable interrupt
MCS(7:0)#:	SDRAM chip select	NTrcClk:	N-Trace clock
MDLLVDD:	Quiet V_{DD} for DLL	NTrcData(3:0):	N-Trace data output
MDQM(8:0):	SDRAM data input mask	NTrcEnd:	N-Trace end

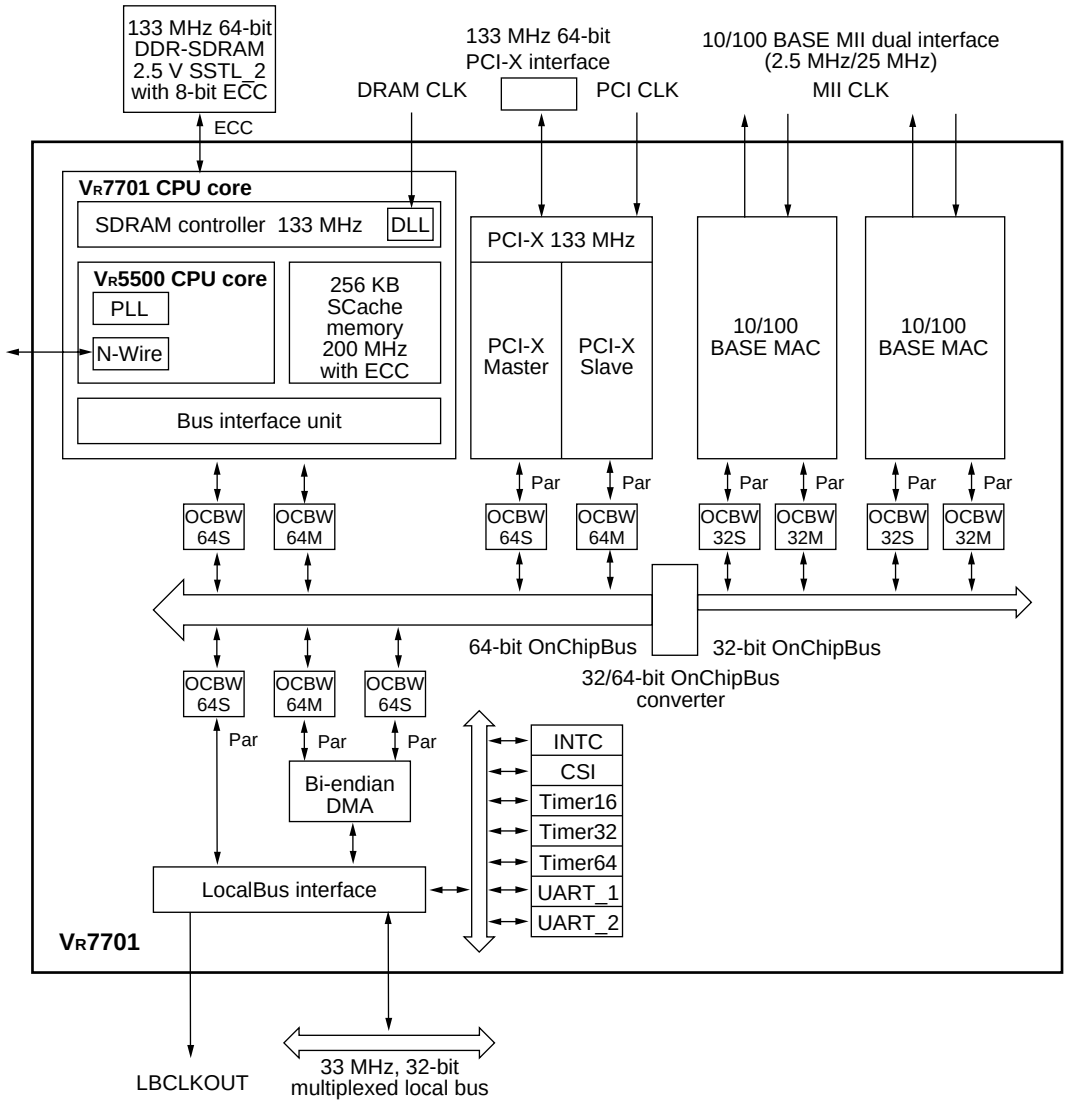
Remark # indicates active low.

Pin Identification (2/2)

★	OOOMode:	Out-of-order return mode	SDLLN1V:	Quiet V_{DD} for DLL
	PACK64#:	PCI-X acknowledge 64 bit transfer	SDLLN2V:	Quiet V_{DD} for DLL
	PAD(63:0):	PCI-X address/data bus	SDLLW1V:	Quiet V_{DD} for DLL
	PCBE(7:0)#:	PCI-X bus command/byte enable	SPLLGND:	Quiet GND for PLL
	PCIBUS64:	PCI-X 64 bit bus mode	SPLLVDD:	Quiet V_{DD} for PLL
	PCIFREQ(1:0):	PCI-X frequency	TCLKIN:	Timer clock input
	PCIMODE:	PCI-X mode	U1CTS:	UART1 clear to send
	PCLKIN:	PCI-X clock	U1DCD:	UART1 data carrier detect
	PDEVSEL#:	PCI-X device select	U1DSR:	UART1 data set ready
	PGNT0#:	PCI-X grant/bus request	U1DTR:	UART1 data terminal ready
	PGNT(3:1)#:	PCI-X grant	U1RTS:	UART1 data request to send
	PFRAME#:	PCI-X cycle frame	U1RXD:	UART1 receive data
	PINTA#:	PCI-X interrupt A	U1TXD:	UART1 transmit data
	PINTB#:	PCI-X interrupt B	U2CTS:	UART2 clear to send
	PINTC#:	PCI-X interrupt C	U2DCD:	UART2 data carrier detect
	PINTD#:	PCI-X interrupt D	U2DSR:	UART2 data set ready
	PIRDY#:	PCI-X initiator ready	U2DTR:	UART2 data terminal ready
	PPAR:	PCI-X parity	U2RTS:	UART2 data request to send
	PPAR64:	PCI-X parity 64	U2RXD:	UART2 receive data
	PPERR#:	PCI-X parity error	U2TXD:	UART2 transmit data
	PREQ0#:	PCI-X request/grant	UARTCLK:	UART clock
	PREQ(3:1)#:	PCI-X bus request	VD2:	Power supply for SDRAM
	PREQ64#:	PCI-X request 64 bit transfer	VD3:	Power supply for I/O
	PRST#:	PCI-X reset	VDD:	Power supply for CPU core
	PSERR#:	PCI-X system error	VDDOK:	VDD ok
	PSTOP#:	PCI-X stop	YPLLGND1:	Quiet GND for PLL
	PTRDY#:	PCI-X target ready	YPLLGND2:	Quiet GND for PLL
	RESET#:	Reset	YPLLVDD1:	Quiet V_{DD} for PLL
	SDLLE1V:	Quiet V_{DD} for DLL	YPLLVDD2:	Quiet V_{DD} for PLL

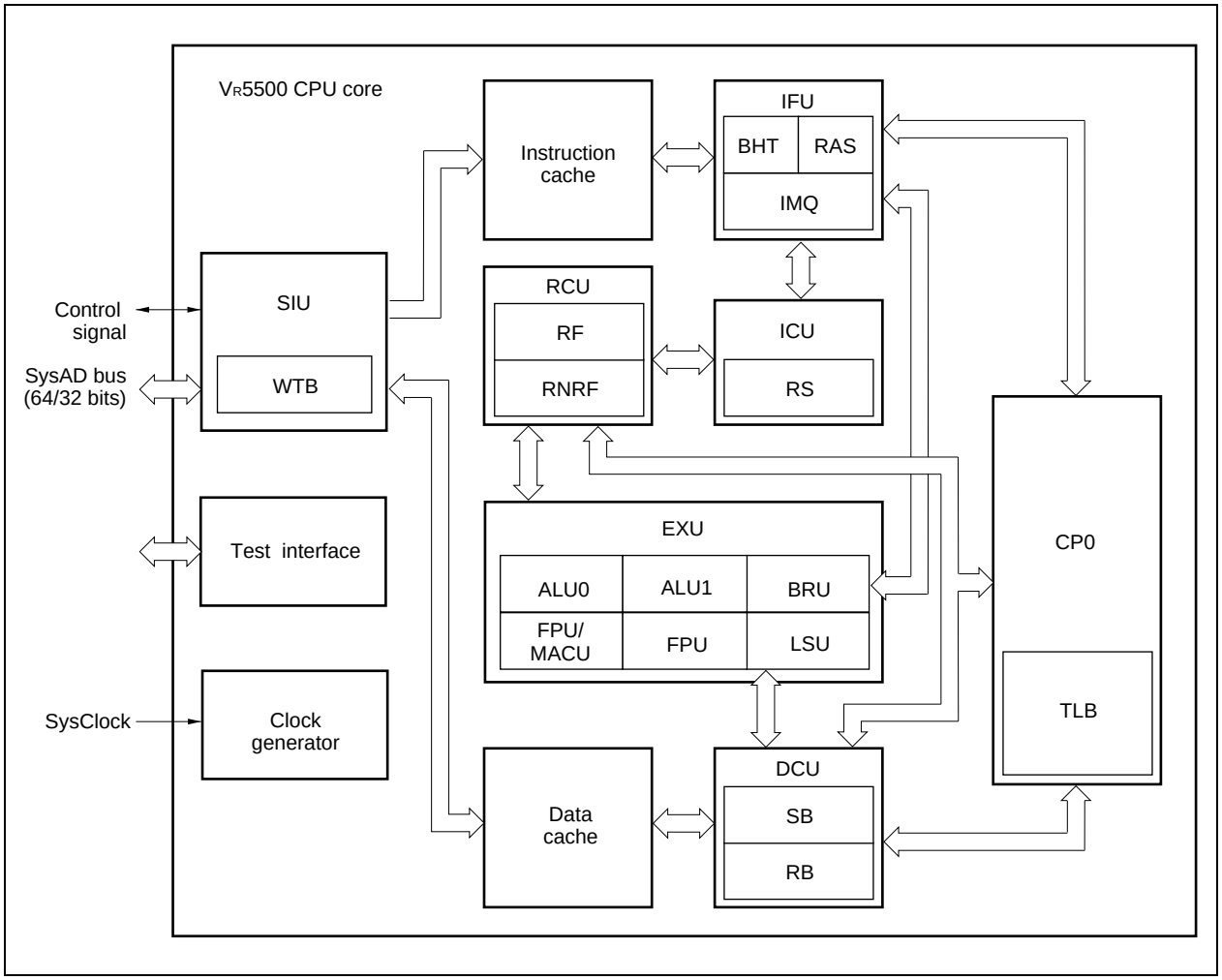
Remark # indicates active low.

INTERNAL BLOCK DIAGRAM AND EXAMPLE OF EXTERNAL CONNECTION



Remark Par: Parity check
ECC: ECC check
OCBW64S, OCBW32S: OnChipBus wrapper slave
OCBW64M, OCBW32M: OnChipBus wrapper master

CPU CORE INTERNAL BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

Remark # indicates active low.

1.1 List of Pin Functions

(1) Initialization interface signals

Signal Name	I/O	Function
RESET#	I	Reset. Logically initializes the internal status of the processor. The DRAM interface is not initialized, however.
COLDRESET#	I	Cold reset. Completely initializes the internal status of the processor, including the DRAM interface.
DEVMEM(1:0)	I	Division mode. Sets a combination of frequency ratios of MCLKIN vs. VCO (PLL oscillation clock) and SysClk vs. DClk (same frequency as MCLKIN). DEVMEM(1:0) SysClk vs. DClk VCO 00 Div1 MCLKIN × 3 01 Div2 MCLKIN × 4 10 Div1.5 MCLKIN × 3 11 Reserved Reserved Use these pins in the combinations shown in Table 1-1.
DEVLC(1:0)	I	Division mode. Sets the division ratio of VCO and ebclk (clock to LocalBus interface. About 33 MHz.) 00: Div9 01: Div12 10: Div15 11: Reserved Use these pins in the combinations shown in Table 1-1.
DEVCPU(2:0)	I	Division mode. Sets the division ratio of SysClk and PClk (pipeline clock). 000: Div2 001: Div2.5 010: Div3 011: Div3.5 100: Div4 101: Div4.5 110: Div5 111: Div5.5 Use these pins in the combinations shown in Table 1-1.
BIGENDIAN	I	Endian mode. Sets the byte order for addressing. 0: Little endian 1: Big endian PCI-X always operates in the little-endian mode.
★ OOOMode	I	Out-of-order return mode. Sets the SysAD bus protocol. 0: Out-of-order return mode 1: Normal mode **Remark** Out-of-order return mode is the mode in which BIU can return a response to a processor read request regardless of the order that the request is issued.

★ **Table 1-1. Combinations of DEVMEM(1:0), DEVLC(1:0), and DEVCPU(2:0)**

DEVMEM(1:0)	DEVLC(1:0)	DEVCPU(2:0)	MCLKIN	VCO	SysClk	ebclk	PClk	Remark
10	01	000	133 MHz	400 MHz	200 MHz	33 MHz	400 MHz	Recommended value
01	01	000	100 MHz	400 MHz	200 MHz	33 MHz	400 MHz	

(2) Interrupt interface signals

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Signal Name	I/O	Function
NMI	I	Non-maskable interrupt. Interrupt request that cannot be masked[Note]
INTP0/GP50	I/O	The function of this pin differs depending on the setting of the INTSEL0 bit of the GPIO_SEL register. • In INT mode (input) This pin functions as INTP0[Note], which inputs a general-purpose processor interrupt. • In GP mode This pin functions as GP50, a general-purpose I/O port.
INTP1/GP51	I/O	The function of this pin differs depending on the setting of the INTSEL1 bit of the GPIO_SEL register. • In INT mode (input) This pin functions as INTP1[Note], which inputs a general-purpose processor interrupt. • In GP mode This pin functions as GP51, a general-purpose I/O port.
INTP2/GP52	I/O	The function of this pin differs depending on the setting of the INTSEL2 bit of the GPIO_SEL register. • In INT mode (input) This pin functions as INTP2[Note], which inputs a general-purpose processor interrupt. • In GP mode This pin functions as GP52, a general-purpose I/O port.
INTP3/GP53	I/O	The function of this pin differs depending on the setting of the INTSEL3 bit of the GPIO_SEL register. • In INT mode (input) This pin functions as INTP3[Note], which inputs a general-purpose processor interrupt. • In GP mode This pin functions as GP53, a general-purpose I/O port.
INTP4/GP54	I/O	The function of this pin differs depending on the setting of the INTSEL4 bit of the GPIO_SEL register. • In INT mode (input) This pin functions as INTP4[Note], which inputs a general-purpose processor interrupt. • In GP mode This pin functions as GP54, a general-purpose I/O port.
INTP5/GP55	I/O	The function of this pin differs depending on the setting of the INTSEL5 bit of the GPIO_SEL register. • In INT mode (input) This pin functions as INTP5[Note], which inputs a general-purpose processor interrupt. • In GP mode This pin functions as GP55, a general-purpose I/O port.

Note Unlike the existing VR Series, these pins of the VR7701 are active-high.

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Signal Name	I/O	Function
INTP6/GP56	I/O	The function of this pin differs depending on the setting of the INTSEL6 bit of the GPIO_SEL register. • In INT mode (input) This pin functions as INTP6[Note], which inputs a general-purpose processor interrupt. • In GP mode This pin functions as GP56, a general-purpose I/O port.
INTP7/GP57	I/O	The function of this pin differs depending on the setting of the INTSEL7 bit of the GPIO_SEL register. • In INT mode (input) This pin functions as INTP7[Note], which inputs a general-purpose processor interrupt. • In GP mode This pin functions as GP57, a general-purpose I/O port.

Note Unlike the existing VR Series, these pins of the VR7701 are active-high.

(3) Power/clock interface signals

Signal Name	I/O	Function
TCLKIN	I	Timer clock. This clock is input to the timer.
VDDOK	I	VDD voltage OK. The external agent asserts this signal when power input and clock input have become stabilized.

(4) SDRAM interface signals

The SDRAM interface conforms to the JEDEC Specification.

Signal Name	I/O	Function
★ MCS(7:0)#	O	SDRAM chip select. Bank select signals of SDRAM. The bank is selected by the following combinations. Bank 1: MCS0#, MCS1# Bank 2: MCS2#, MCS3# Bank 3: MCS4#, MCS5# Bank 4: MCS6#, MCS7#
MMA(14:0)	O	SDRAM address. Address signals output to SDRAM.
MMBA(1:0)	O	SDRAM bank address. These signals specify one of the four banks to which commands are to be applied.
MDQM(8:0)	O	SDRAM data input mask. These signals mask input of write data to SDRAM. When these signals are asserted when SDRAM is written, data input to SDRAM is masked.
MRAS#	O	SDRAM row address strobe. The basic command is defined by a combination of the MRAS#, MCAS#, and MWE# signals.
MCAS#	O	SDRAM column address strobe. The basic command is defined by a combination of the MRAS#, MCAS#, and MWE# signals.
MWE#	O	SDRAM write enable. The basic command is defined by a combination of the MRAS#, MCAS#, and MWE# signals.
MMD(63:0)	I/O	SDRAM data bus. This is a bus for inputting/outputting data from/to SDRAM.
MMDP(7:0)	I/O	SDRAM data bus parity. These are ECC bits for MMD(63:0).
MDQS(7:0)	I/O	SDRAM data strobe. These signals are output from SDRAM along with read data, and input to SDRAM along with write data. These signals function as an operating reference clock when DDR SDRAM is read or written.
MDQSP	I/O	SDRAM data parity strobe. This is a strobe signal for the MMDP(7:0) signal.
MVref(1:0)	I	SDRAM Vref. Reference voltage for SDRAM input/output pins.
MCLKIN	I	SDRAM clock. Clock input for SDRAM interface.
MCLKIN#	I	SDRAM clock. Clock input for SDRAM interface that is the complement of MCLKIN.
MCKE(3:0)	O	SDRAM clock enable. These signals determine whether the MCLKIN signal is valid or not.

(5) PCI-X interface signals

The PCI-X interface conforms to PCISIG Specifications.

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Signal Name	I/O	Function
PCLKIN	I	PCI-X clock. Clock input to PCI-X. An appropriate clock must be input to this pin even if the PCI-X bus is not used.
★ PRST#	I/O	PCI-X reset. • When the HOSTMODE signal is 1 Reset output to PCI-X. The level specified in the PCI Reset register is output. • When the HOSTMODE signal is 0 Reset input from PCI-X.
PAD(63:0)	I/O	PCI-X address/data bus. The bus master outputs an address in the address phase and the transmitter device outputs data in the data phase.
PCBE(7:0)#	I/O	PCI-X bus command/byte enable. These signals are output by the bus master. In the address phase, these signals indicate a bus command. They indicate a valid byte lane in the data phase.
PPAR	I/O	PCI-X parity. Even parity for PAD(31:0) and PCBE(3:0)#.
PFRAME#	I/O	PCI-X cycle frame. This signal is output by the bus master, indicating that a bus cycle is under execution.
PIRDY#	I/O	PCI-X initiator ready. This signal is output by the bus master, indicating that data can be transferred.
PTRDY#	I/O	PCI-X target ready. This signal is output by the target, indicating that data can be transferred.
PSTOP#	I/O	PCI-X stop. This signal is output by the target, requesting stoppage of a bus cycle.
PDEVSEL#	I/O	PCI-X device select. This signal is output by the target, reporting a response to a bus cycle.
PPERR#	I/O	PCI-X parity error. This signal is output by the receiver device, indicating detection of a parity error in the data phase.
PSERR#	I/O	PCI-X system error. This signal is output by the PCI-X device, indicating detection of other bus errors (this signal is asynchronous to PCLKIN).
PREQ64#	I/O	PCI-X 64-bit request. This signal is output by the bus master, indicating that 64-bit data can be transferred.
PACK64#	I/O	PCI-X 64-bit acknowledge. This signal is output by the target, indicating that 64-bit data can be transferred.
PPAR64	I/O	PCI-X parity 64. This is an even parity bit for PAD(64:32) and PCBE(7:4)#.
PREQ(3:1)#	I	PCI-X bus request. These signals are output by the PCI-X device, requesting the arbiter for the bus mastership.

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Signal Name	I/O	Function
PREQ0#	I	PCI-X bus request/grant. • If PBA bit [Note] is 1 The PCI-X device outputs this signal, requesting the arbiter for the bus mastership. • If PBA bit [Note] is 0 The arbiter outputs this signal, granting the bus mastership to the PCI-X device.
PGNT(3:1)#	O	PCI-X grant. The arbiter outputs this signal, granting the bus mastership to the PCI-X device.
PGNT0#	O	PCI-X grant/bus request. • If PBA bit [Note] is 1 The arbiter outputs this signal, granting the bus mastership to the PCI-X device. • If PBA bit [Note] is 0 The PCI-X device outputs this signal, requesting the arbiter for the bus mastership.
PINTA#	I/O	PCI-X interrupt A. • When the HOSTMODE signal is 1 Interrupt request input. • When the HOSTMODE signal is 0 Interrupt request output (this signal is asynchronous to PCLKIN).
PINTB#	I	PCI-X interrupt B. The PCI-X device outputs this signal, requesting an interrupt (this signal is asynchronous to PCLKIN).
PINTC#	I	PCI-X interrupt C. The PCI-X device outputs this signal, requesting an interrupt (this signal is asynchronous to PCLKIN).
PINTD#	I	PCI-X interrupt D. The PCI-X device outputs this signal, requesting an interrupt (this signal is asynchronous to PCLKIN).
PCIMODE	I	PCI-X mode setting. 0: PCI-X mode 1: PCI mode
PCIFREQ(1:0)	I	Setting of PCI-X frequency. These signals are used to determine the range of PLL for the clock of the PCI-X interface, and the initialize pattern in the host bridge mode. 00: 33 MHz 01: 66 MHz 10: 100 MHz 11: 133 MHz
PCIBUS64	I	PCI-X 64-bit bus mode. 0: 32-bit bus mode 1: 64-bit bus mode
HOSTMODE	I	PCI-X host mode. This signal is used to determine the host bridge mode and target device mode. 0: PCI device 1: PCI host device
IDSEL	I	PCI-X initialization device select. The bus master outputs this signal during configuration.

Note Bit 5 of the Unit Control register

(6) MII (Media Independent Interface) channel 1 signals

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Signal Name	I/O	Function
MI1TXCLK/GP0	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 1 transmit clock. This pin functions as MI1TXCLK. It inputs the transmit clock necessary for outputting transmit data to a PHY device connected to the port. • In GP mode This pin functions as GP0, a general-purpose I/O port.
MI1TXEN/GP1	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (output) MII channel 1 transmit enable. This pin functions as MI1TXEN. It indicates whether transmit data (TXD) is valid for each port. • In GP mode This pin functions as GP1, a general-purpose I/O port.
MI1TXD0/GP2	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (output) MII channel 1 transmit data. This pin functions as MI1TXD0. It outputs transmit data to the PHY device connected to the port. • In GP mode This pin functions as GP2, a general-purpose I/O port.
MI1TXD1/GP3	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (output) MII channel 1 transmit data. This pin functions as MI1TXD1. It outputs transmit data to the PHY device connected to the port. • In GP mode This pin functions as GP3, a general-purpose I/O port.
MI1TXD2/GP4	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (output) MII channel 1 transmit data. This pin functions as MI1TXD2. It outputs transmit data to the PHY device connected to the port. • In GP mode This pin functions as GP4, a general-purpose I/O port.
MI1TXD3/GP5	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (output) MII channel 1 transmit data. This pin functions as MI1TXD3. It outputs transmit data to the PHY device connected to the port. • In GP mode This pin functions as GP5, a general-purpose I/O port.

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Signal Name	I/O	Function
MI1TXER/GP6	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (output) MII channel 1 transmit coding error. This pin functions as MI1TXER. It indicates that an error has occurred in MAC during transmission. • In GP mode This pin functions as GP6, a general-purpose I/O port.
MI1COL/GP7	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 1 collision. This pin functions as MI1COL. It inputs a collision signal detected by the PHY device connected to the port. If the port is not used, fix MI1COL to the low level. • In GP mode This pin functions as GP7, a general-purpose I/O port.
MI1CRS/GP8	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 1 carrier sense. This pin functions as MI1CRS. It inputs a carrier sense signal from the PHY device connected to the port. If the port is not used, fix MI1CRS to the low level. • In GP mode This pin functions as GP8, a general-purpose I/O port.
MI1RXCLK/GP9	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 1 receive clock. This pin functions as MI1RXCLK. It inputs the clock from the PHY device. • In GP mode This pin functions as GP9, a general-purpose I/O port.
MI1RXDV/GP10	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 1 receive data valid. This pin functions as MI1RXDV. It indicates that the receive data on RXD is valid. If the port is not used, fix MI1RXDV to the high or low level. • In GP mode This pin functions as GP10, a general-purpose I/O port.
MI1RXD0/GP11	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 1 receive data. This pin functions as MI1RXD0. It inputs receive data from the PHY device connected to the port. • In GP mode This pin functions as GP11, a general-purpose I/O port.

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Signal Name	I/O	Function
MI1RXD1/GP12	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 1 receive data. This pin functions as MI1RXD1. It inputs receive data from the PHY device connected to the port. • In GP mode This pin functions as GP12, a general-purpose I/O port.
MI1RXD2/GP13	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 1 receive data. This pin functions as MI1RXD2. It inputs receive data from the PHY device connected to the port. • In GP mode This pin functions as GP13, a general-purpose I/O port.
MI1RXD3/GP14	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 1 receive data. This pin functions as MI1RXD3. It inputs receive data from the PHY device connected to the port. • In GP mode This pin functions as GP14, a general-purpose I/O port.
MI1RXER/GP15	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 1 receive error. This pin functions as MI1RXER. This is an input signal to detect an error that occurs in the PHY device connected to the port during reception. If the port is not used, fix MI1RXER to the low level. • In GP mode This pin functions as GP15, a general-purpose I/O port.
MI1MDCLK/GP16	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode (output) MII channel 1 management data clock. This pin functions as MI1MDCLK. It is a transfer clock of MII serial management data. • In GP mode This pin functions as GP16, a general-purpose I/O port.
MI1MD/GP17	I/O	This signal functions differently depending on the setting of the MI1SEL bit of the GPIO_SEL register. • In MII mode MII channel 1 management data. This pin functions as MI1MD. It is a bidirectional MII serial management data signal. • In GP mode This pin functions as GP17, a general-purpose I/O port.

(7) MII (Media Independent Interface) channel 2 signals

(1/3)

Signal Name	I/O	Function
MI2TXCLK/GP18	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 2 transmit clock. This pin functions as MI2TXCLK. It inputs the transmit clock necessary for outputting transmit data to a PHY device connected to the port. • In GP mode This pin functions as GP18, a general-purpose I/O port.
MI2TXEN/GP19	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (output) MII channel 2 transmit enable. This pin functions as MI2TXEN. It indicates whether transmit data (TXD) is valid for each port. • In GP mode This pin functions as GP19, a general-purpose I/O port.
MI2TXD0/GP20	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (output) MII channel 2 transmit data. This pin functions as MI2TXD0. It outputs transmit data to the PHY device connected to the port. • In GP mode This pin functions as GP20, a general-purpose I/O port.
MI2TXD1/GP21	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (output) MII channel 2 transmit data. This pin functions as MI2TXD1. It outputs transmit data to the PHY device connected to the port. • In GP mode This pin functions as GP21, a general-purpose I/O port.
MI2TXD2/GP22	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (output) MII channel 2 transmit data. This pin functions as MI2TXD2. It outputs transmit data to the PHY device connected to the port. • In GP mode This pin functions as GP22, a general-purpose I/O port.
MI2TXD3/GP23	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (output) MII channel 2 transmit data. This pin functions as MI2TXD3. It outputs transmit data to the PHY device connected to the port. • In GP mode This pin functions as GP23, a general-purpose I/O port.

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Signal Name	I/O	Function
MI2TXER/GP24	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (output) MII channel 2 transmit coding error. This pin functions as MI2TXER. It indicates that an error has occurred in MAC connected to the port during transmission. • In GP mode This pin functions as GP24, a general-purpose I/O port.
MI2COL/GP25	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 2 collision. This pin functions as MI2COL. It inputs a collision signal detected by the PHY device connected to the port. If the port is not used, fix MI2COL to the low level. • In GP mode This pin functions as GP25, a general-purpose I/O port.
MI2CRS/GP26	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 2 carrier sense. This pin functions as MI2CRS. It inputs a carrier sense signal from the PHY device connected to the port. If the port is not used, fix MI2CRS to the low level. • In GP mode This pin functions as GP26, a general-purpose I/O port.
MI2RXCLK/GP27	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 2 receive clock. This pin functions as MI2RXCLK. It inputs the clock from the PHY device. • In GP mode This pin functions as GP27, a general-purpose I/O port.
MI2RXDV/GP28	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 2 receive data valid. This pin functions as MI2RXDV. It indicates that the receive data on RXD is valid. If the port is not used, fix MI2RXDV to the high or low level. • In GP mode This pin functions as GP28, a general-purpose I/O port.
MI2RXD0/GP29	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 2 receive data. This pin functions as MI2RXD0. It inputs receive data from the PHY device connected to the port. • In GP mode This pin functions as GP29, a general-purpose I/O port.

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Signal Name	I/O	Function
MI2RXD1/GP30	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 2 receive data. This pin functions as MI2RXD1. It inputs receive data from the PHY device connected to the port. • In GP mode This pin functions as GP30, a general-purpose I/O port.
MI2RXD2/GP31	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 2 receive data. This pin functions as MI2RXD2. It inputs receive data from the PHY device connected to the port. • In GP mode This pin functions as GP31, a general-purpose I/O port.
MI2RXD3/GP32	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 2 receive data. This pin functions as MI2RXD3. It inputs receive data from the PHY device connected to the port. • In GP mode This pin functions as GP32, a general-purpose I/O port.
MI2RXER/GP33	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 2 receive error. This pin functions as MI2RXER. This is an input signal to detect an error that occurs in the PHY device connected to the port during reception. If the port is not used, fix MI2RXER to the low level. • In GP mode This pin functions as GP33, a general-purpose I/O port.
MI2MDCLK/GP34	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (output) MII channel 2 management data clock. This pin functions as MI2MDCLK. It is the transfer clock of MII serial management data. • In GP mode This pin functions as GP34, a general-purpose I/O port.
MI2MD/GP35	I/O	This signal functions differently depending on the setting of the MI2SEL bit of the GPIO_SEL register. • In MII mode (input) MII channel 2 management data. This pin functions as MI2MD. It is a bidirectional MII serial management data signal. • In GP mode This pin functions as GP35, a general-purpose I/O port.

(8) LocalBus interface signals

Signal Name	I/O	Function
LAD(31:0)	I/O	LocalBus address/data bus. The bus master outputs an address in the address phase and the transmitter device outputs data in the data phase.
LALE	O	LocalBus address latch enable. This is a latch enable signal of the address output from the LAD bus. It is asserted for one bus clock as soon as a bus cycle has been started.
LCS1#	O	LocalBus chip select 1. This signal indicates that a memory area of addresses 0xF F900 0000 to 0xF F9FF FFFF is accessed.
LCS2#	O	LocalBus chip select 2. This signal indicates that a memory area of addresses 0xF FA00 0000 to 0xF FBFF FFFF is accessed.
LCS3#	O	LocalBus chip select 3. This signal indicates that a memory area of addresses 0xF FC00 0000 to 0xF FCFF FFFF or an I/O area of addresses 0x0001 0000 to 0x0001 FFFF is accessed.
LCS4#	O	LocalBus chip select 4. This signal indicates that a memory area of addresses 0xF FD00 0000 to 0xF FDFF FFFF or an I/O area of addresses 0x0002 0000 to 0x0002 FFFF is accessed.
LCS5#	O	LocalBus chip select 5. This signal indicates that a memory area of addresses 0xF FE00 0000 to 0xF FEFF FFFF or an I/O area of addresses 0x0003 0000 to 0x0003 FFFF is accessed.
LCS6#	O	LocalBus chip select 6. This signal indicates that a memory area of addresses 0xF FF00 0000 to 0xF FFFF FFFF is accessed.
LRD#	O	LocalBus read. This signal is asserted during read, reporting a read access to the external device. This signal is kept asserted until LRDY# is asserted.
LWR#	O	LocalBus write. This signal is asserted during write, reporting a write access to the external device. This signal is kept asserted until LRDY# is asserted.
★ LRDY#	I	LocalBus ready. The external device asserts this signal when it gets ready for data transfer. When ready control is performed using this signal, the LocalBus interface does not end the bus cycle until this signal is asserted. Therefore, when accessing any of the LCS areas (including unimplemented areas), be sure to assert this signal.
LBT16#	I	Bus size specification during LocalBus boot. This signal changes the data bus width of the LCS6 area between 32 and 16 bits. LBT16# can be changed only after reset. If it is changed not after reset, the CPU operation is not guaranteed. 0: 32-bit bus width 1: 16-bit bus width
LBCLKOUT	O	LocalBus clock output. Bus clock of the local bus.
LDRQ0	I	LocalBus channel 0 DMA request. This pin inputs a transfer request signal of internal DMA channel 0.
LDRQ1	I	LocalBus channel 1 DMA request. This pin inputs a transfer request signal of internal DMA channel 1.

(9) Asynchronous serial interface channel 1 (UART1) signals

(1/2)

Signal Name	I/O	Function
U1RXD/GP36	I/O	The function of this pin differs depending on the setting of the U1SEL bit of the GPIO_SEL register. • In UART, CSI/UART, or GP/UART mode (input) UART1 receive data. This pin functions as U1RXD. It inputs receive serial data to the VR7701. • In GP mode This pin functions as GP36, a general-purpose I/O port.
U1TXD/GP37	I/O	The function of this pin differs depending on the setting of the U1SEL bit of the GPIO_SEL register. • In UART, CSI/UART, or GP/UART mode (output) UART1 transmit data. This pin functions as U1TXD. It outputs transmit serial data from the VR7701. • In GP mode This pin functions as GP37, a general-purpose I/O port.
U1RTS/GP38	I/O	The function of this pin differs depending on the setting of the U1SEL bit of the GPIO_SEL register. • In UART, CSI/UART, or GP/UART mode (output) UART1 transmission request. This pin functions as U1RTS. This signal is asserted when the VR7701 can receive serial data from the 16550 controller connected to the port. • In GP mode This pin functions as GP38, a general-purpose I/O port.
U1CTS/GP39	I/O	The function of this pin differs depending on the setting of the U1SEL bit of the GPIO_SEL register. • In UART, CSI/UART, or GP/UART mode (input) UART1 transmission request. This pin functions as U1CTS. Assert this signal when the 16550 controller connected to the port can receive the serial data transmitted from the VR7701. • In GP mode This pin functions as GP39, a general-purpose I/O port.
U1DTR/CSI_DO/GP40	I/O	The function of this pin differs depending on the setting of the U1SEL bit of the GPIO_SEL register. • In UART mode (output) UART1 data terminal ready. This pin functions as U1DTR. This signal is asserted when the VR7701 is ready for transmitting/receiving serial data. • In CSI/UART mode (output) CSI serial data output. This pin functions as CSI_DO. It outputs serial data from the VR7701. • In GP or GP/UART mode This pin functions as GP40, a general-purpose I/O port.

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Signal Name	I/O	Function
U1DCD/CSI_DI/GP41	I/O	The function of this pin differs depending on the setting of the U1SEL bit of the GPIO_SEL register. • In UART mode (input) UART1 data carrier detection. This pin functions as U1DCD. Assert this signal while valid serial data is received. • In CSI/UART mode (input) CSI serial data input. This pin functions as CSI_DI. It inputs serial data to the VR7701. • In GP or GP/UART mode This pin functions as GP41, a general-purpose I/O port.
U1DSR/CSI_CLK/GP42	I/O	The function of this pin differs depending on the setting of the U1SEL bit of the GPIO_SEL register. • In UART mode (input) UART1 data set ready. This pin functions as U1DSR. Assert this signal while the 16650 controller connected to the port is ready to transmit/receive serial data to/from the VR7701. • In CSI/UART mode (output) CSI clock. This pin functions as CSI_CLK. It is a serial data transmission/reception clock output from the VR7701. • In GP or GP/UART mode This pin functions as GP42, a general-purpose I/O port.

(10) Asynchronous serial interface channel 2 (UART2) signals

(1/2)

Signal Name	I/O	Function
U2RXD/GP43	I/O	The function of this pin differs depending on the setting of the U2SEL bit of the GPIO_SEL register. • In UART or GP/UART mode (input) UART2 receive data. This pin functions as U2RXD. It inputs receive serial data to the VR7701. • In GP mode This pin functions as GP43, a general-purpose I/O port.
U2TXD/GP44	I/O	The function of this pin differs depending on the setting of the U2SEL bit of the GPIO_SEL register. • In UART or GP/UART mode (output) UART2 transmit data. This pin functions as U2TXD. It outputs transmit serial data from the VR7701. • In GP mode This pin functions as GP44, a general-purpose I/O port.
U2RTS/GP45	I/O	The function of this pin differs depending on the setting of the U2SEL bit of the GPIO_SEL register. • In UART or GP/UART mode (output) UART2 transmission request. This pin functions as U2RTS. This signal is asserted when the VR7701 can receive serial data from the 16550 controller connected to the port. • In GP mode This pin functions as GP45, a general-purpose I/O port.

(2/2)

Signal Name	I/O	Function
U2CTS/GP46	I/O	The function of this pin differs depending on the setting of the U2SEL bit of the GPIO_SEL register. • In UART or GP/UART mode (input) UART2 transmission request. This pin functions as U2CTS. Assert this signal when the 16550 controller connected to the port can receive the serial data transmitted from the VR7701. • In GP mode This pin functions as GP46, a general-purpose I/O port.
U2DTR/GP47	I/O	The function of this pin differs depending on the setting of the U2SEL bit of the GPIO_SEL register. • In UART mode (output) UART2 data terminal ready. This pin functions as U2DTR. This signal is asserted when the VR7701 is ready for transmitting/receiving serial data. • In GP or GP/UART mode This pin functions as GP47, a general-purpose I/O port.
U2DCD/GP48	I/O	The function of this pin differs depending on the setting of the U2SEL bit of the GPIO_SEL register. • In UART mode (input) UART2 data carrier detection. This pin functions as U2DCD. Assert this signal while valid serial data is received. • In GP or GP/UART mode This pin functions as GP48, a general-purpose I/O port.
U2DSR/GP49	I/O	The function of this pin differs depending on the setting of the U2SEL bit of the GPIO_SEL register. • In UART mode (input) UART2 data set ready. This pin functions as U2DSR. Assert this signal while the 16650 controller connected to the port is ready to transmit/receive serial data to/from the VR7701. • In GP or GP/UART mode This pin functions as GP49, a general-purpose I/O port.

(11) Asynchronous serial interface clock signal

The following signal is shared by UART1 and UART2.

Signal Name	I/O	Function
UARTCLK	I	UART clock. This pin inputs a serial clock for UART. Input a serial clock for UART from this pin when an external clock is used.

(12) Clocked serial interface (CSI) signals

Signal Name	I/O	Function
CSI_DO/U1DTR/GP40	O	See **(9) Asynchronous serial interface channel 1 (UART1) signals**.
CSI_DI/U1DCD/GP41	I	
CSI_CLK/U1DSR/GP42	O	

Caution An RTC interface can be created by using one of the GP signals as an RTC chip enable signal (output).

(13) GPIO interface signals

Signal Name	I/O	Function
GP(57:0)	I/O	GPIO. These are general-purpose I/O signals of the VR7701. Usually, they are used as alternate-function pins. For the alternate-function signals, see **(2)**, **(6)**, **(7)**, **(9)**, and **(10)**.

(14) Debug interface signals

Signal Name	I/O	Function
JTCK	I	JTAG clock. Serial clock input for JTAG.
JTDI	I	JTAG data input. Serial data input for JTAG.
JTDO	O	JTAG data output. Serial data output for JTAG.
JTMS	I	JTAG mode selection. JTAG test mode selection.
JTRST#	I	JTAG reset. Reset input for JTAG.
NTrcClk	O	Trace clock. Clock output for test interface.
NTrcData(3:0)	O	Trace data. Data output for test interface.
NTrcEnd	O	Trace end. This signal indicates the end of a trace data packet.
BKTGIO#	I/O	Break trigger I/O. Break or trigger I/O signal.

(15) Power supply

Signal Name	Function
GND	Ground
YPLLGND1	Ground for internal PLL
YPLLGND2	Ground for internal PLL
SPLLGND	Ground for internal PLL
VDD	1.5 V power supply for core
VD2	2.5 V power supply for SDRAM interface
VD3	3.3 V power supply for other I/O
YPLLVDD1	Power supply for internal PLL
YPLLVDD2	Power supply for internal PLL
SPLLVDD	Power supply for internal PLL
MDLLVDD	Power supply for internal DLL
SDLLE1V	Power supply for internal DLL
SDLLN1V	Power supply for internal DLL
SDLLN2V	Power supply for internal DLL
SDLLW1V	Power supply for internal DLL

Caution The VR7701 uses three power supply pins. Power can be applied to these power supply pins in any sequence. However, power must not be applied to one or two pins for 100 ms or longer while it is not applied to the other pins.

★ (16) Test

Signal Name	I/O	Function
IC-PUpR	I	Connect to VD3 via a pull-up resistor.
IC-PDnR	I	It is recommended to connect this pin to GND via a pull-down resistor, however this pin may be directly connected to GND.

1.2 Connection of Unused Pins

The pins shown in Table 1-2 are not used as interface signals during normal operation. Connect these pins as indicated in this table.

Table 1-2. Connecting of Unused Pins (1)

Pin	Connection of Unused Pin
JTCK	Pull up to VD3
JTDI	Pull up to VD3
JTDO	Leave open
JTMS	Pull up to VD3
JTRST#	Pull down
NTrcClk	Leave open
NTrcData(3:0)	Leave open
NtrcEnd	Leave open
BKTGIO#	Pull up to VD3

The pins shown in Table 1-3 may not be used in specific system configuration. Connect these pins as indicated in this table when they are not used.

Table 1-3. Connection of Unused Pins (2)

Pin	Connection of Unused Pin
PCLKIN	Input appropriate clock
PAD(63:32)	Pull up to VD3
PCBE(7:4)#	Pull up to VD3
PREQ64#	Pull up to VD3
PACK64#	Pull up to VD3
PPAR64	Pull up to VD3
MI1/2TXCLK	Pull down or pull up to VD3
MI1/2RXCLK	Pull down or pull up to VD3
MI1/2COL	Pull down
MI1/2CRS	Pull down
MI1/2RXDV	Pull down or pull up to VD3
MI1/2RXER	Pull down
U1/2RXD	Pull down or pull up to VD3
U1/2CTS	Pull down or pull up to VD3
U1/2DSR	Pull down or pull up to VD3
★ LRDY#	Pull down

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

	Parameter	Symbol	Conditions	Ratings	Unit
	Supply voltage	V_{DD}	VDD pin	−0.5 to +2.0	V
		V_{D2}	VD2 pin	−0.5 to +4.6	V
		V_{D3}	VD3 pin	−0.5 to +4.6	V
★	Analog voltage for DLL	V_{DLL}	MDLLVDD, SDLLE1V, SDLLN1V, SDLLN2V, and SDLLW1V pins	−0.5 to +2.0	V
★	Input voltage[Note]	V_{IN}	VD2 pin	−0.5 to V_{D2} +0.5	V
			VD3 pin	−0.5 to V_{D3} +0.5	V
	Operating case temperature	T_C		0 to 85	°C
	Storage temperature	T_{stg}		−40 to +125	°C

Note The upper limit of the input voltage is +4.0 V.

Cautions 1. Do not short-circuit two or more outputs at the same time.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The specifications and conditions shown in the following DC Characteristics and AC Characteristics sections are the ranges within which the product can normally operate and the quality can be guaranteed.

★ Operating Range (T_C = 0 to 85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		1.48	1.56	1.64	V
	V_{D2}	DDR SDRAM	2.3	2.5	2.7	V
	V_{D3}		3.14	3.3	3.47	V
SDRAM reference voltage	MV_{ref}	DDR SDRAM	1.15	1.25	1.35	V
SDRAM termination voltage	V_{TT}		MV_{ref} − 0.04		MV_{ref} + 0.04	V
Operating current	I_{CC_Core}	Core block, **Note**			2.55	A
	I_{CC2}	2.5 V I/O block, **Note**			0.45	A
	I_{CC3}	3.3 V I/O block, **Note**			0.23	A
Power consmption	P_D	**Note**			5.84	W
Operating temperature	T_C	Case temperature	0		85	°C

Note When V_{DD} = 1.56 V, V_{D2} = 2.5 V, V_{D3} = 3.3 V, and other conditions are the maximum values (High temperature, process: first).

Caution The V_R7701 uses three power supply pins. Power can be applied to these power supply pins in any sequence. However, power must not be applied to one or two pins for 100 ms or longer while it is not applied to the other pins.

DC Characteristics (T_C = 0 to 85°C, V_{DD} = 1.48 to 1.64 V, V_{D3} = 3.14 to 3.47 V)

★ **(1) LVTTL interface block**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output voltage, high	V_{OH}	I_{OH} = –2 mA	2.4		V
Output voltage, low	V_{OL}	I_{OL} = 2 mA		0.4	V
Input voltage, high	V_{IH}		2.0	V_{D3} + 0.5	V
	V_{IHR}	COLDRESET#, RESET# pins	2.5	V_{D3} + 0.5	V
Input voltage, low	V_{IL}		–0.5	+0.8	V
Output current, high	I_{OH}	V_{OH} = 2.4 V	–2.0		mA
Output current, low	I_{OL}	V_{OL} = 0.4 V	2.0		mA
Input capacitance	C_{in}	V_{D3} = 0 V, T_J = 25°C, F = 1 MHz	4.0	6.0	pF
Input/output capacitance	C_{io}	V_{D3} = 0 V, T_J = 25°C, F = 1 MHz	4.0	6.0	pF
Input current leakage	I_{Leak}		–10.0	+10.0	μA
Output current leakage	I_{OLeak}		–10.0	+10.0	μA

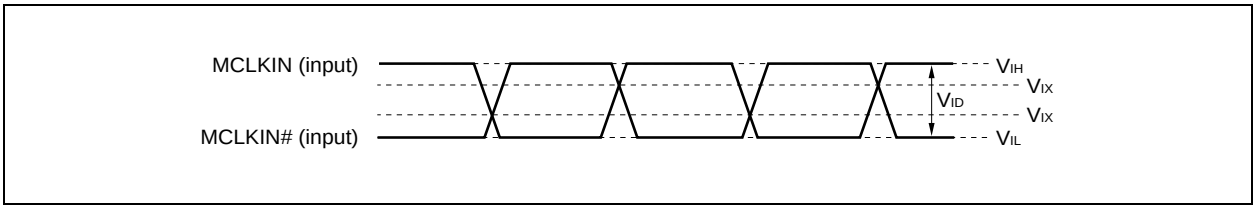
Remark These parameters apply to signals other than those for the SDRAM interface and PCI-X interface.

(2) SSTL_2 interface block (V_{D2} = 2.3 to 2.7 V)

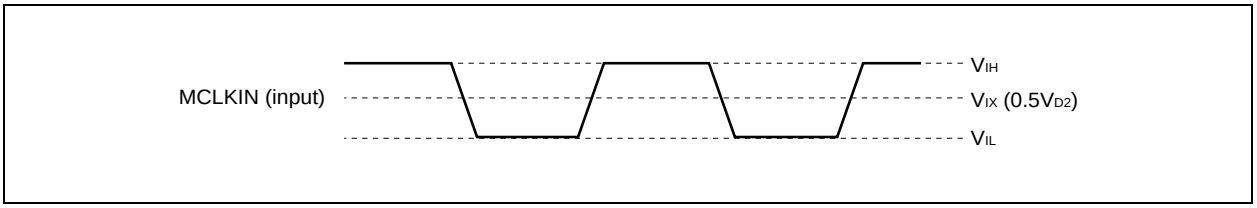
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output voltage, high	V_{OH}	I_{OH} = – 15.2 mA	0.85V_{D2}		V
Output voltage, low	V_{OL}	I_{OL} = 15.2 mA		0.15V_{D2}	V
Input voltage, high	V_{IH} (DC)		MV_{ref} + 0.18	V_{D2} + 0.3	V
Input voltage, low	V_{IL} (DC)		– 0.3	MV_{ref} – 0.18	V
Input differential voltage	V_{ID} (DC)		0.36	V_{D2} + 0.6	V
Input cross point voltage	V_{IX}		0.5V_{D2} – 0.2	0.5V_{D2} + 0.2	V
★ Output current, high	I_{OH}	V_{D2} = 2.3 V, V_{OH} = V_{D2} – 0.35 V	–15.2		mA
Output current, low	I_{OL}	V_{D2} = 2.3 V, V_{OL} = 0.35 V	15.2		mA
Input capacitance	C_{in}		2.0	4.0	pF
Input/output capacitance	C_{io}		4.0	6.0	pF
Input current leakage	I_{Leak}		–5.0	+5.0	μA
Output current leakage	I_{OLeak}		–5.0	+5.0	μA

Remark These parameters apply to the SDRAM interface signals only.

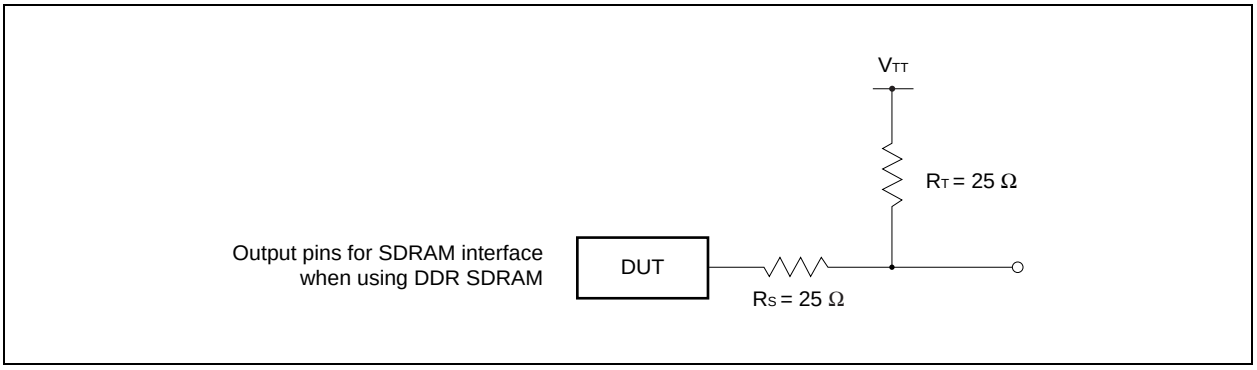
Differential input level



Single-ended input level



Example of connection of external resistors



★ **(3) PCI-X interface block**

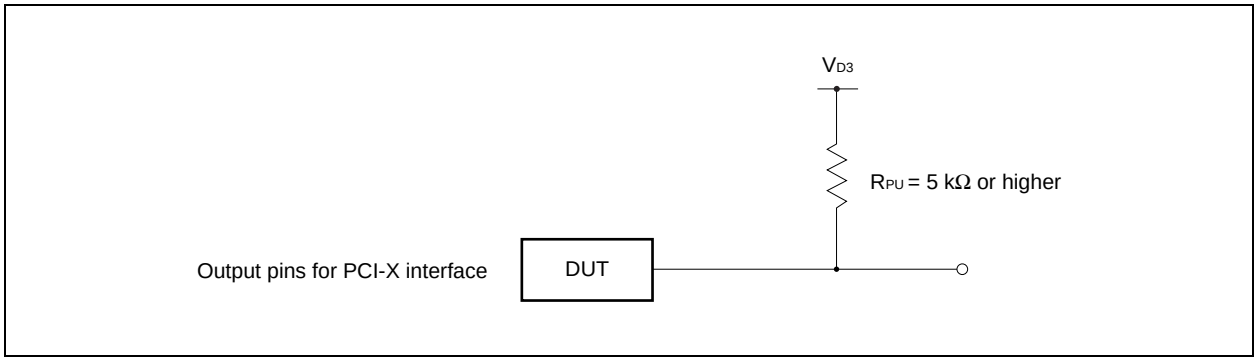
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output voltage, high	V_{OH}	I_{OH} = – 0.5 mA	$0.9V_{D3}$		V
Output voltage, low	V_{OL}	I_{OL} = 1.5 mA		$0.1V_{D3}$	V
Input voltage, high	V_{IH}		$0.5V_{D3}$	V_{D3} + 0.5	V
	V_{IHCM}	**Note 1**	2.0	V_{D3} + 0.5	V
Input voltage, low	V_{IL}		–0.5	$+0.35V_{D3}$	V
	V_{ILCM}	**Note 1**	–0.5	0.8	V
Reference voltage for PCI-X interface	V_{test}	Input	$0.4V_{D3}$		V
		Output (rising) Note 2	$0.285V_{D3}$		V
		Output (falling) Note 2	$0.615V_{D3}$		V
Output current, high	I_{OH}	$V_{OH} = 0.9V_{D3}$ V	–0.5		mA
Output current, low	I_{OL}	$V_{OL} = 0.1V_{D3}$ V	1.5		mA
Input capacitance	C_{in}			8.0	pF
Input/output capacitance	C_{io}			8.0	pF
Input current leakage	I_{Leak}		–10.0	+10.0	μA
Output current leakage	I_{OLeak}		–10.0	+10.0	μA

Notes 1. Applies to the PCLKIN, PCIMODE, PCIFREQ(1:0), PCIBUS64, and HOSTMODE pins.

2. This is specified for measurement use only. Refer to PCI-X Specification for details.

Remark These parameters apply to the PCI-X interface signals only.

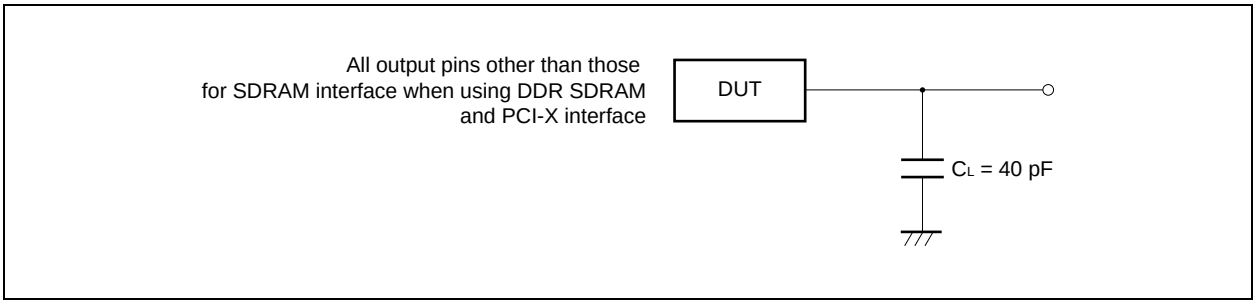
Example of connection of external resistors



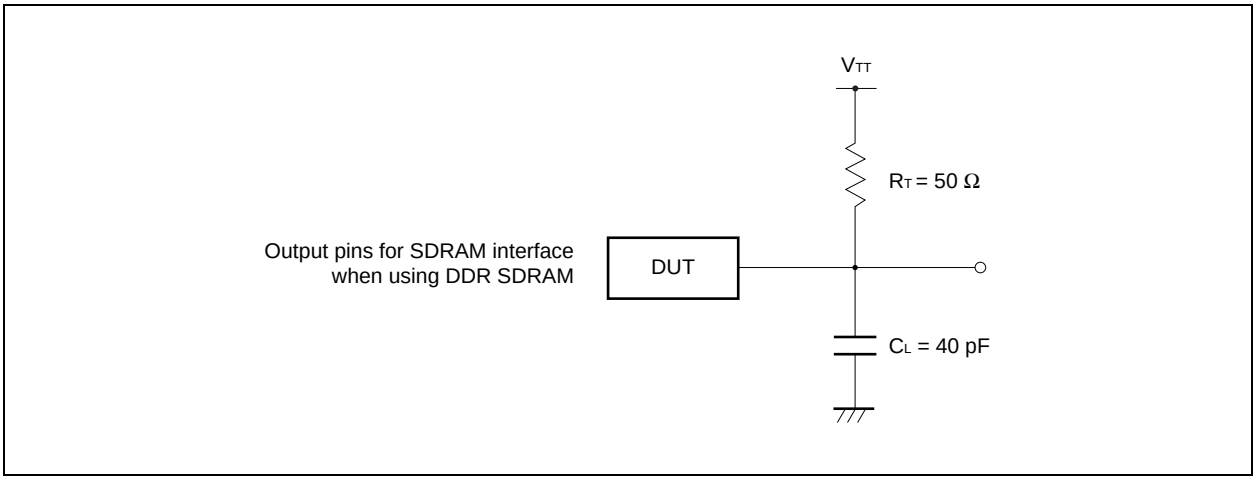
AC Characteristics (T_C = 0 to 85°C, V_{DD} = 1.48 to 1.64 V, V_{D3} = 3.14 to 3.47 V)

Load conditions

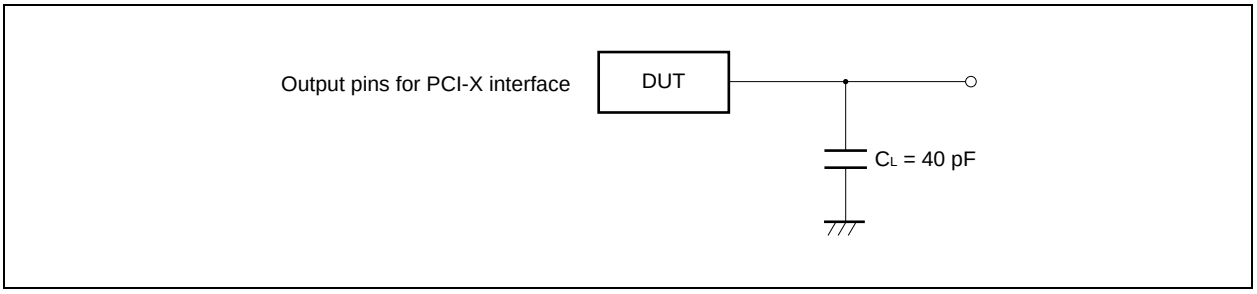
★ **(a) LVTTL interface block**



(b) SSTL_2 interface block



(c) PCI-X interface block



★ **(1) Clock parameters**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Pipeline clock frequency				400	MHz
Pipeline clock period	$t_{PipeClkPer}$		2.5		ns
SysClk period	$t_{SysClkPer}$		5.0		ns
ebclk period	$t_{ebclkPer}$		30		ns
Dclk period	$t_{DclkPer}$		7.5	10	ns
TCLKIN period	$t_{TclkinPer}$		40		ns
LBCLKOUT period	$t_{LBclkPer}$		30		ns
PCLKIN period	$t_{PClkPer}$		7.5 Note 1	20	ns
Ethernet interface clock Note 2 period	$t_{EtheClkPer}$	At 100 Mbps operation	40		ns
		At 10 Mbps operation	400		ns
MCLKIN period	t_{MCK}		7.5	10	ns
MCLKIN high-level width	t_{MCH}		$0.45t_{MCK}$	$0.55t_{MCK}$	ns
MCLKIN low-level width	t_{MCL}		$0.45t_{MCK}$	$0.55t_{MCK}$	ns
MCLKIN rise time	t_{MCRise}		1		V/ns
MCLKIN fall time	t_{MCFall}		1		V/ns
MCLKIN cycle-to-cycle jitter	t_{MJI}			±150	ps
JTCK period	$t_{JTAGPer}$		25	1000	ns

Notes 1. This is the value for the VR7701 operating in PCI-X mode. The value for the VR7701 operating in PCI mode is 30.

2. 'Ethernet interface clock' means MInTXCLK and MInRXCLK (n = 1 or 2).

★ **(2) Interrupt interface parameters (C_L = 40 pF)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI/INTP active level width	$t_{nmi/int}$		$2t_{LBclkPer}$		ns

★ **(3) SDRAM interface parameters (V_{D2} = 2.3 to 2.7 V, V_{ID}(AC) = 0.7 V, V_{IH}(AC) = MV_{ref} + 0.35 V (MIN.), V_{IL}(AC) = MV_{ref} – 0.35 V (MAX.), C_L = 40 pF, R_T = 50 Ω)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MCLKIN frequency			100	133	MHz
MCLKIN period	t_{MCK}		7.5	10	ns
MCLKIN high-level width	t_{MCH}		0.45t_{MCK}	0.55t_{MCK}	ns
MCLKIN low-level width	t_{MCL}		0.45t_{MCK}	0.55t_{MCK}	ns
MCLKIN rise time	t_{MCRise}		1		V/ns
MCLKIN fall time	t_{MCFall}		1		V/ns
MCLKIN cycle-to-cycle jitter	t_{MJI}			±150	ps
Address/command output delay time	t_{ACO}	**Note 1**	0.5	3.0	ns
MMD/MDQM setup time to MDQS on memory write	t_{DDWs}		0.95		ns
MMD/MDQM hold time from MDQS on memory write	t_{DDWh}		0.95		ns
MDQS/MDQSP output delay	t_{DQSO}	**Note 2**	5.9	8.2	ns
Write preamble setup time	t_{PREs}	Guaranteed by design.	0.8		ns
Write postamble	t_{PST}	Guaranteed by design.	3.0	4.5	ns
MDQS falling edge setup time to MCLKIN rising edge	t_{DQSs}	**Note 2**	2.8		ns
MDQS falling edge hold time from MCLKIN rising edge	t_{DQSh}	**Note 2**	1.8		ns
MMD setup time to MDQS on memory read	t_{DDRs}	**Note 2**		0.95	ns
MMD hold time from MDQS on memory read	t_{DDRh}	**Note 2**	2.25		ns
MDQS/MDQSP output delay on memory read	t_{DQSD}		−0.25	3.1	ns

Notes 1. This parameter applies to the MMA(14:0), MMBA(1:0), MCS(7:0)#, MCKE(3:0), MRAS#, MCAS#, and MWE# pins.

In the 2-cycle mode, this applies to the MMA(14:0), MMBA(1:0), MRAS#, MCAS#, and MWE# pins only.

2. When the DLLTRM bit of the SDCNT register is 11011.

(4) PCI-X interface parameters (C_L = 40 pF)

Parameter	Symbol	Conditions	PCI-X Mode		PCI Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
PCLKIN frequency			50	133		33	MHz
PCLKIN period	$t_{PClkPer}$		7.5	20	30		ns
PCLKIN high-level width	$t_{PClkHigh}$		3		11		ns
PCLKIN low-level width	$t_{PClkLow}$		3		11		ns
Data output delay time to valid	t_{DO_PCI}		0.7	3.8	1	10	ns
	$t_{DO\_PCI(PTP)}$	**Note**	0.7	3.8	1	11	ns
Data output delay time to active	t_{ON}		0		1		ns
Data output delay time to float	t_{OFF}			7		28	ns
Data input setup time	t_{DS_PCI}		1.2		7		ns
	$t_{DS\_PCI(PTP)}$	**Note**	1.2		7		ns
Data input hold time	t_{DH_PCI}		0.5		0		ns

Note This parameter applies to the PREQ(3:0)# and PGNT(3:0)# pins when they are connected point to point.

★ (5) Asynchronous serial interface (UART) parameters (C_L = 40 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
UnTXD pulse width	t_{TXD}			125	ns
UnRXD pulse width	t_{RXD}			125	ns

Remark n = 1 or 2

★ (6) Clocked serial interface (CSI) parameters (C_L = 40 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
CSI_CLK frequency				16.6	MHz
CSI_CLK period	$t_{CSIclkPer}$		60		ns
CSI_CLK high-level width	$t_{CSIclkHigh}$		24		ns
CSI_CLK low-level width	$t_{CSIclkLow}$		24		ns
CSI_CLK rise time	$t_{CSIclkRise}$	**Note**		1.4	ns
CSI_CLK fall time	$t_{CSIclkFall}$	**Note**		0.8	ns
CSI_CLK cycle-to-cycle jitter	$t_{CSIclkJitter}$			±150	ps
Data output delay time	t_{DO_CSI}			10	ns
Data input setup time	t_{DS_CSI}		10		ns
Data input hold time	t_{DH_CSI}		0		ns

Note C_L = 10 pF, 0.1V_{D3} to 0.9V_{D3}, guaranteed by design.

★ **(7) Ethernet interface parameters (C_L = 40 pF)**

(a) Transmit interface block

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MInTXCLK frequency		At 100 Mbps operation		25	MHz
		At 10 Mbps operation		2.5	MHz
MInTXCLK period	$t_{TXclkPer}$	At 100 Mbps operation	40		ns
		At 10 Mbps operation	400		ns
MInTXCLK high-level width	$t_{TXclkHigh}$	At 100 Mbps operation	$0.35t_{TXclkPer}$	$0.65t_{TXclkPer}$	ns
		At 10 Mbps operation	$0.35t_{TXclkPer}$	$0.65t_{TXclkPer}$	ns
MInTXCLK low-level width	$t_{TXclkLow}$	At 100 Mbps operation	$0.35t_{TXclkPer}$	$0.65t_{TXclkPer}$	ns
		At 10 Mbps operation	$0.35t_{TXclkPer}$	$0.65t_{TXclkPer}$	ns
MInTXD output delay time	t_{DO_TX}		0	15	ns
Control signal assertion delay time	t_{AS_TX}	MInTXEN and MInTXER pins	0	15	ns
Control signal deassertion delay time	t_{DAS_TX}	MInTXEN and MInTXER pins	0	15	ns

Remark n = 1 or 2

(b) Receive interface block

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MInRXCLK frequency		At 100 Mbps operation		25	MHz
		At 10 Mbps operation		2.5	MHz
MInRXCLK period	$t_{RXclkPer}$	At 100 Mbps operation	40		ns
		At 10 Mbps operation	400		ns
MInRXCLK high-level width	$t_{RXclkHigh}$	At 100 Mbps operation	$0.35t_{TXclkPer}$	$0.65t_{TXclkPer}$	ns
		At 10 Mbps operation	$0.35t_{TXclkPer}$	$0.65t_{TXclkPer}$	ns
MInRXCLK low-level width	$t_{RXclkLow}$	At 100 Mbps operation	$0.35t_{TXclkPer}$	$0.65t_{TXclkPer}$	ns
		At 10 Mbps operation	$0.35t_{TXclkPer}$	$0.65t_{TXclkPer}$	ns
MInRXD input setup time	t_{DS_RXD}		10		ns
MInRXD input hold time	t_{DH_RXD}		5		ns
Control signal setup time	t_{DS_RX}	MInRXDV and MInRXER pins	5		ns
Control signal hold time	t_{DH_RX}	MInRXDV and MInRXER pins	5		ns

Remark n = 1 or 2

(c) Management interface block

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MInMDCLK frequency				15	MHz
MInMDCLK period	$t_{MDclkPer}$		66		ns
★ MInMD output delay time	t_{DO_MD}		3		ns
MInMD input setup time	t_{DS_MD}		10		ns
★ MInMD input hold time	t_{DH_MD}		0		ns

Remark n = 1 or 2

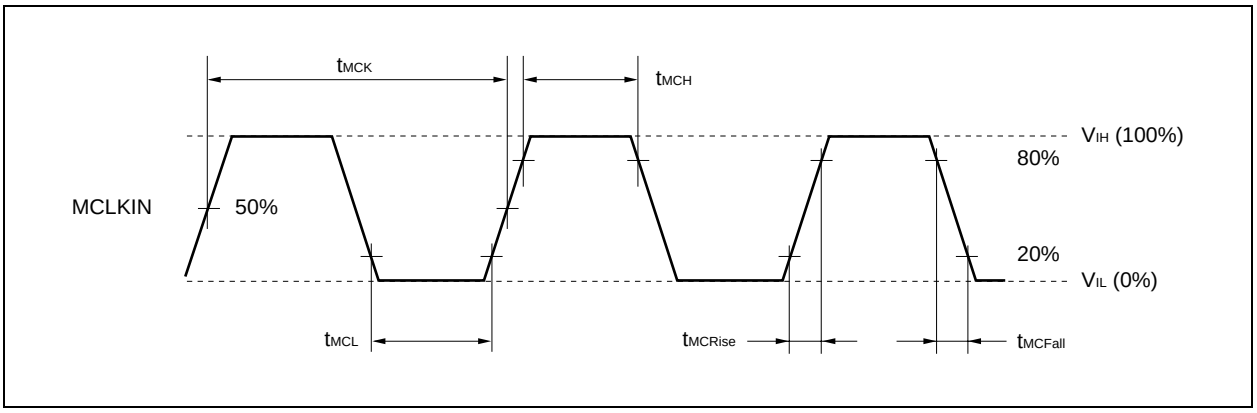
★ **(8) LocalBus interface parameters (C_L = 40 pF)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
LBCLKOUT frequency				33	MHz
LBCLKOUT period	$t_{LBclkPer}$		30		ns
LBCLKOUT high-level width	$t_{LBclkHigh}$		12		ns
LBCLKOUT low-level width	$t_{LBclkLow}$		12		ns
LBCLKOUT rise time	$t_{LBclkRise}$	**Note**		1.4	ns
LBCLKOUT fall time	$t_{LBclkFall}$	**Note**		0.8	ns
LBCLKOUT cycle-to-cycle jitter	$t_{LBclkJitter}$			±150	ps
Data output delay time	t_{DO_LB}			6.2	ns
Data input setup time	t_{DS_LB}		4.8		ns
Data input hold time	t_{DH_LB}		0		ns

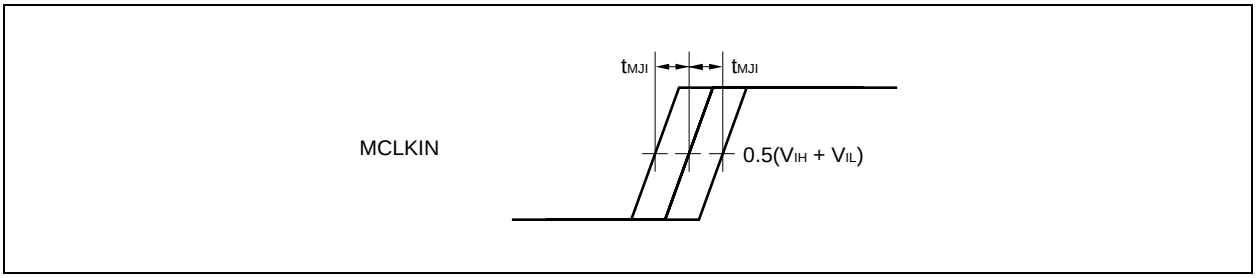
Note C_L = 10 pF, 0.1 V_{D3} to 0.9 V_{D3}, guaranteed by design.

Timing Charts

MCLKIN waveform

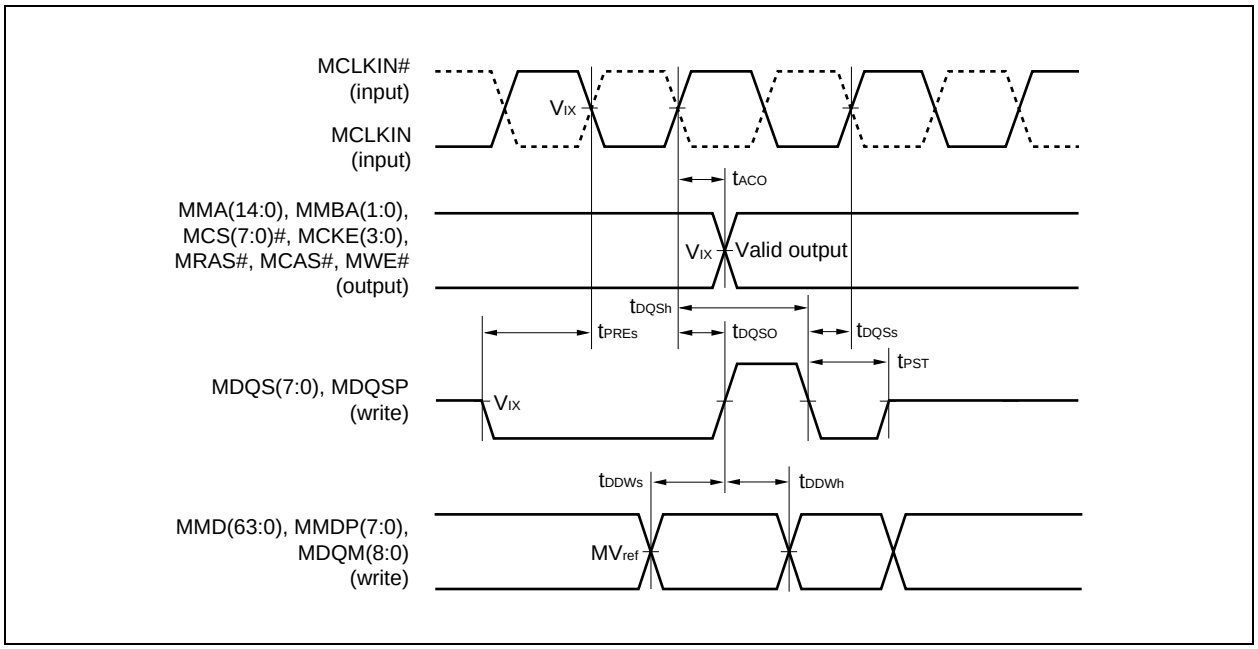


MCLKIN cycle-to-cycle jitter

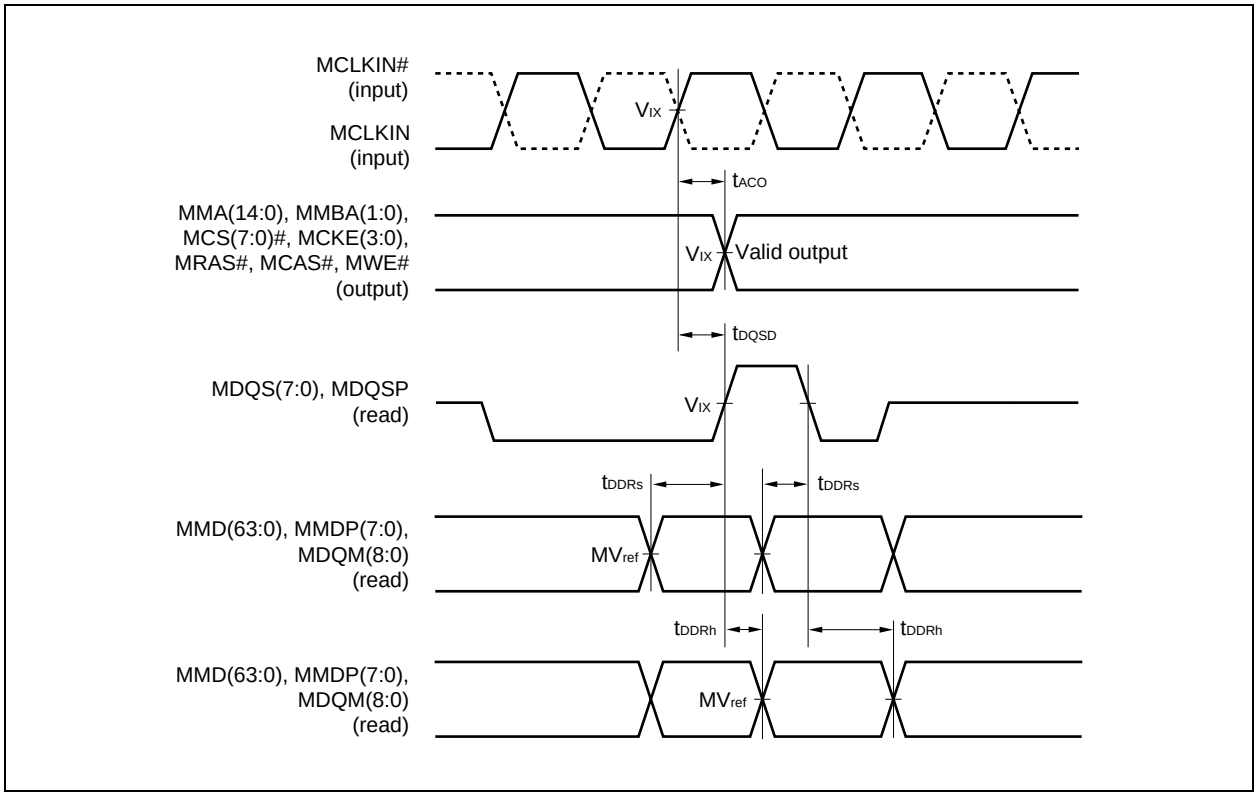


SDRAM interface edge timing

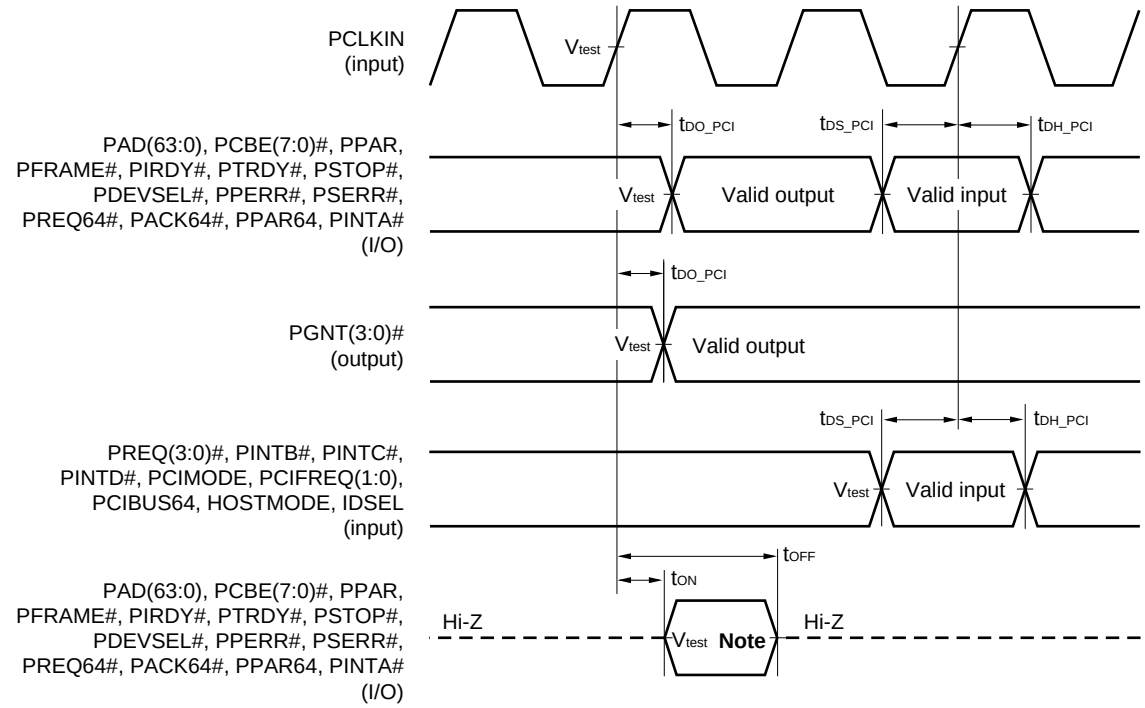
★ **(a) When using DDR SDRAM (write)**



(b) When using DDR SDRAM (read)

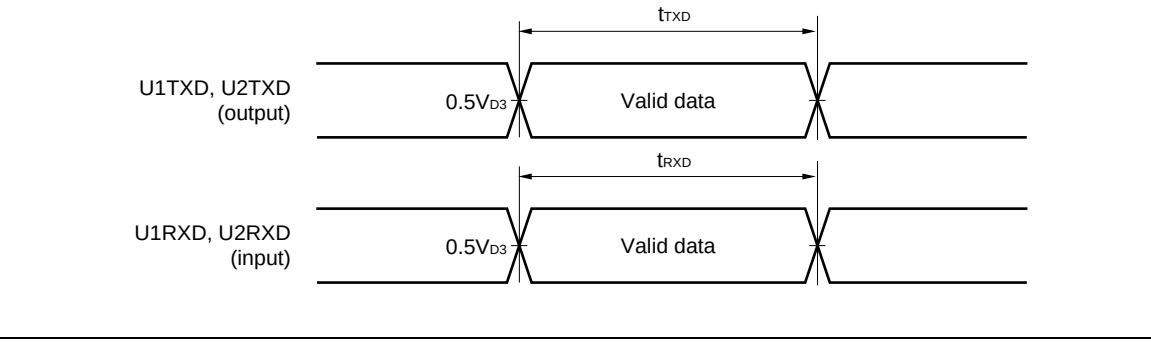


PCI-X interface edge timing

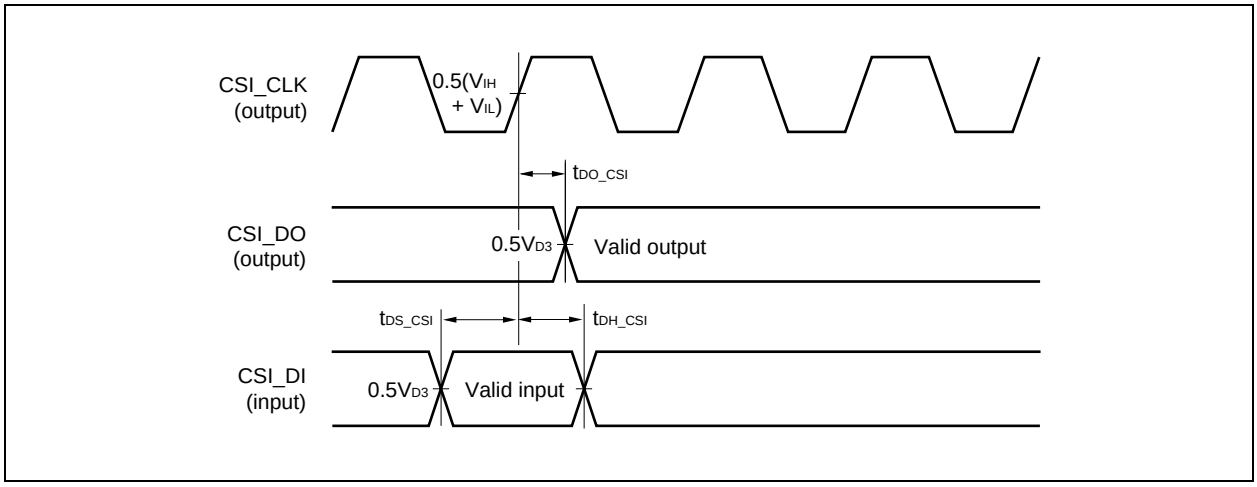


Note Valid output

Asynchronous serial interface (UART) edge timing

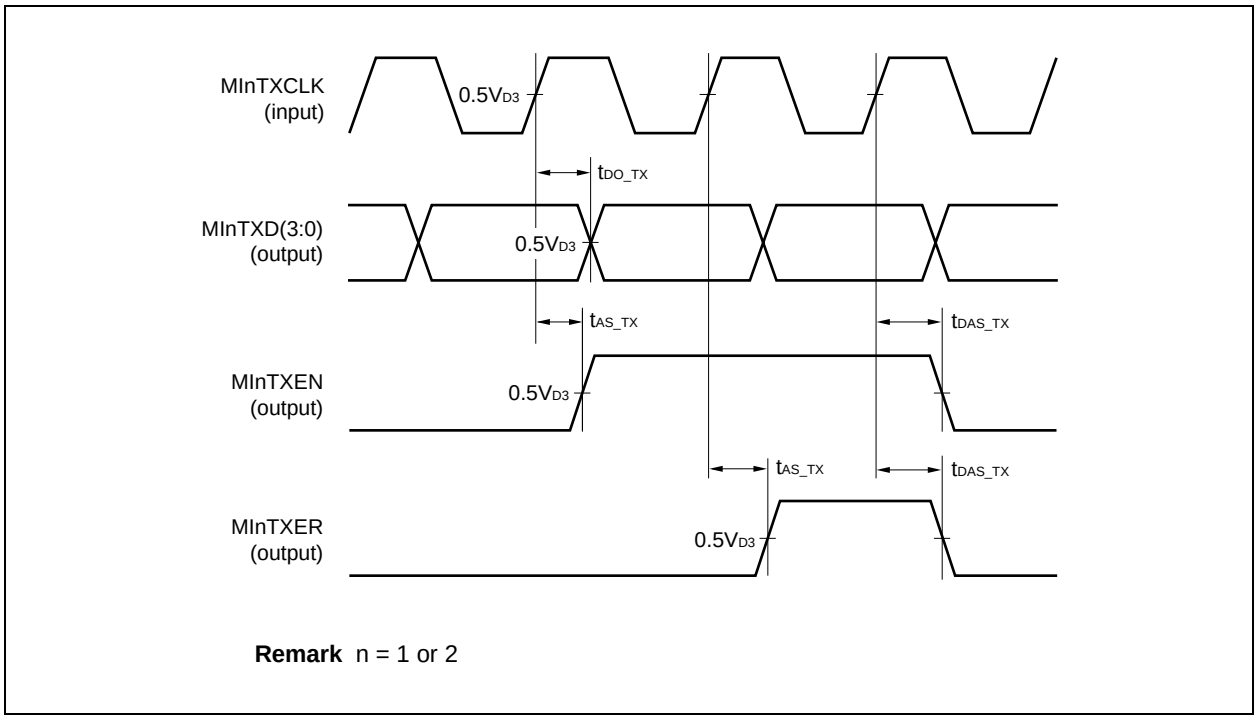


Clocked serial interface (CSI) edge timing



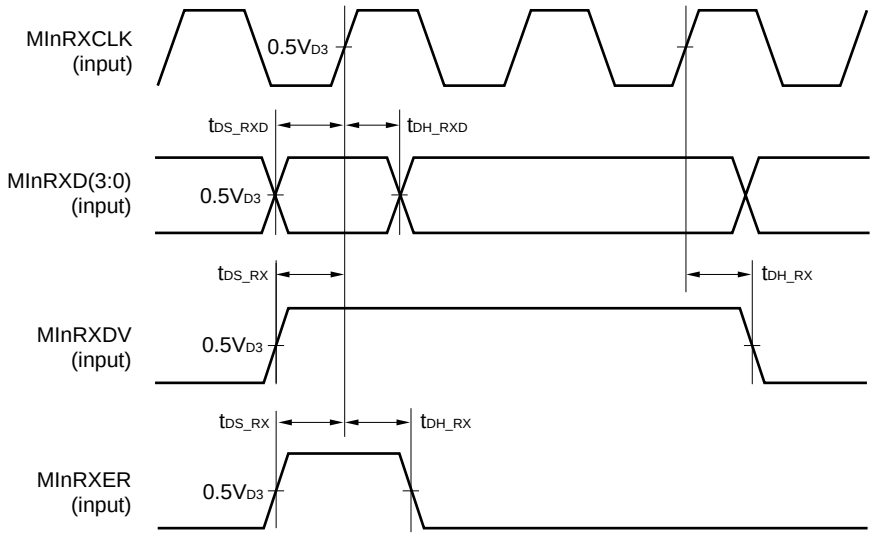
Ethernet interface edge timing

(a) Transmit interface block



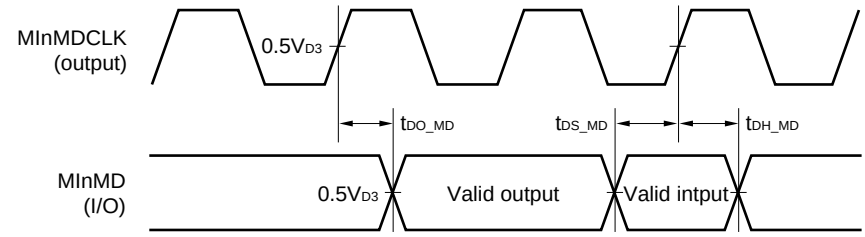
Remark n = 1 or 2

(b) Receive interface block



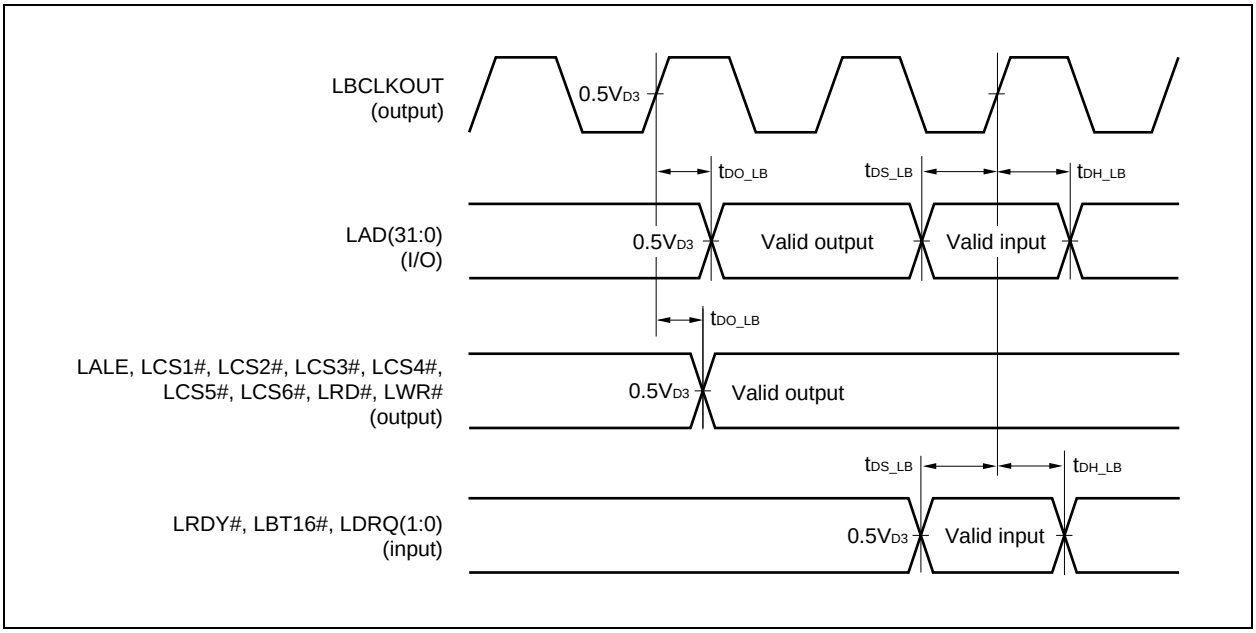
Remark n = 1 or 2

(c) Management interface block



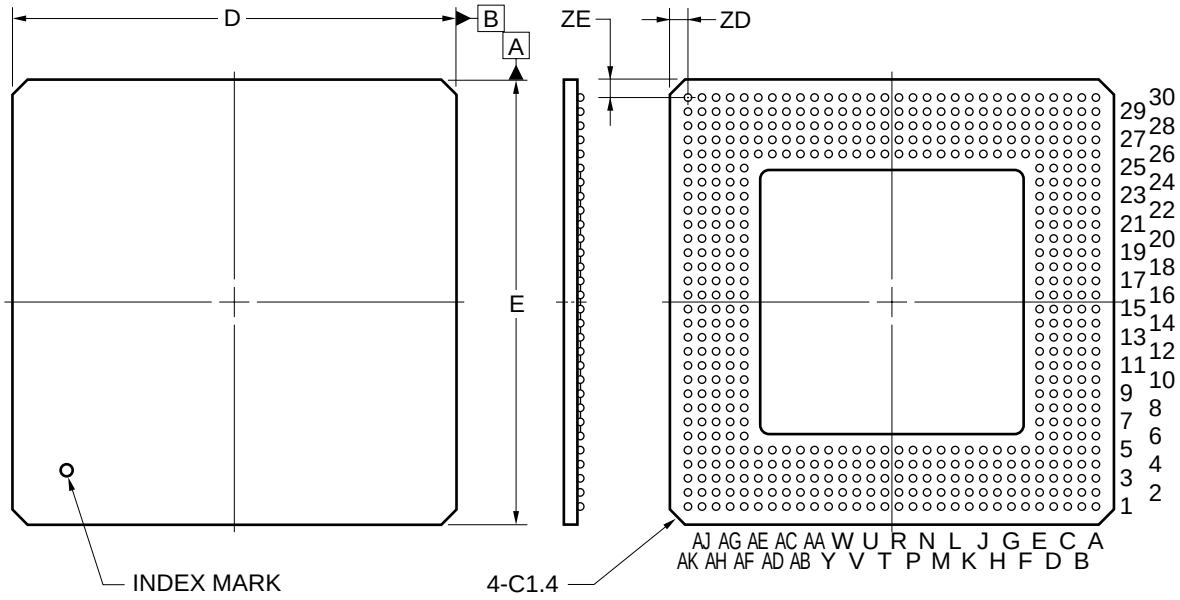
Remark n = 1 or 2

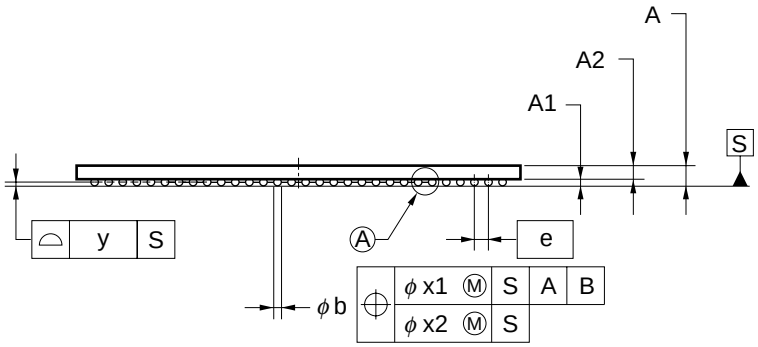
LocalBus interface edge timing

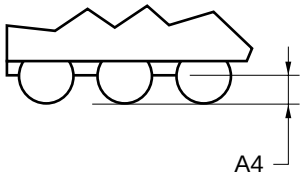


3. PACKAGE DRAWING

500-PIN PLASTIC BGA (CAVITY DOWN ADVANCED TYPE) (40x40)







ITEM	MILLIMETERS
D	40.00±0.20
E	40.00±0.20
e	1.27
A	1.75±0.20
A1	0.60±0.10
A2	1.15
A4	0.25 MIN.
b	0.75±0.15
x1	0.30
x2	0.15
y	0.20
ZD	1.585
ZE	1.585

P500F2-127-UA5-1

★ 4. RECOMMENDED SOLDERING CONDITIONS

The μPD30671 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Table 4-1. Surface Mounting Type Soldering Conditions

μPD30671F2-400-UA5-A[Note 1]: 500-pin plastic BGA (C/D advanced type) (40 × 40)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 250°C, Time: 60 seconds max. (at 220°C or higher), Count: 3 times max., Exposure limit: 3 days[Note 2] (after that, prebake at 125°C for 20 to 72 hours.)	IR50-203-3

Notes 1. Lead-free product

2. After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Related documents μPD30550 (V_R5500) Data Sheet (U15700E)
V_R5500 User's Manual (U16044E)
V_R5000, V_R10000 Instruction User's Manual (U12754E)

Reference document Electrical Characteristics for Microcomputer (U15170J)[Note]

Note This document number is that of Japanese version.

The related documents indicated in the publication may include preliminary versions. However, preliminary versions are not marked as such.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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