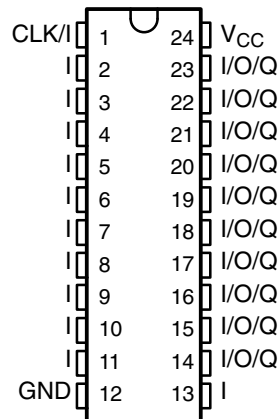


TIBPAL22V10C, TIBPAL22V10AC, TIBPAL22V10AM HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

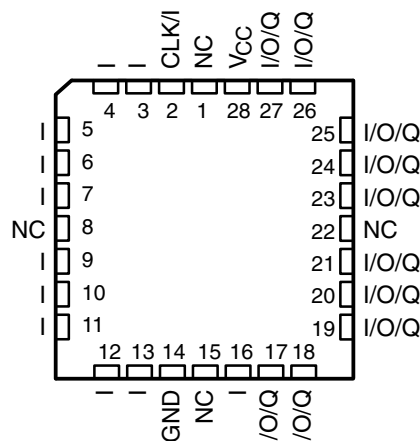
SRPS024A – OCTOBER 1986 – REVISED APRIL 2010

- **Second-Generation PLD Architecture**
- **Choice of Operating Speeds**
 TIBPAL22V10AC . . . 25 ns Max
 TIBPAL22V10AM . . . 30 ns Max
 TIBPAL22V10C . . . 35 ns Max
- **Increased Logic Power – Up to 22 Inputs and 10 Outputs**
- **Increased Product Terms – Average of 12 Per Output**
- **Variable Product Term Distribution Allows More Complex Functions to Be Implemented**
- **Each Output Is User Programmable for Registered or Combinational Operation, Polarity, and Output Enable Control**
- **TTL-Level Preload for Improved Testability**
- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**
- **Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses**
- **AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features**
- **Dependable Texas Instruments Quality and Reliability**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Functionally Equivalent to AMDs AMPAL22V10 and AMPAL22V10A**

C SUFFIX . . . NT PACKAGE
M SUFFIX . . . JT OR W PACKAGE
 (TOP VIEW)



C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
 (TOP VIEW)



NC – No internal connection
 Pin assignments in operating mode

description

The TIBPAL22V10 and TIBPAL22V10A are programmable array logic devices featuring high speed and functional equivalency when compared to presently available devices. They are implemented with the familiar sum-of-products (AND-OR) logic structure featuring the new concept "Programmable Output Logic Macrocell". These *IMPACT*™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic.

These devices contain up to 22 inputs and 10 outputs. They incorporate the unique capability of defining and programming the architecture of each output on an individual basis. Outputs may be registered or nonregistered and inverting or noninverting as shown in the output logic macrocell diagram. The ten potential outputs are enabled through the use of individual product terms.

These devices are covered by U.S. Patent 4,410,987.
IMPACT is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date.
 Products conform to specifications per the terms of Texas Instruments
 standard warranty. Production processing does not necessarily include
 testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2010, Texas Instruments Incorporated

TIBPAL22V10C, TIBPAL22V10AC, TIBPAL22V10AM
HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC CIRCUITSSRPS024A – OCTOBER 1986 – REVISED APRIL 2010

description (continued)

Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

With features such as programmable output logic macrocells and variable product term distribution, the TIBPAL22V10 and TIBPAL22V10A offer quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power up with their outputs high. Registered outputs selected as active-high power up with their outputs low.

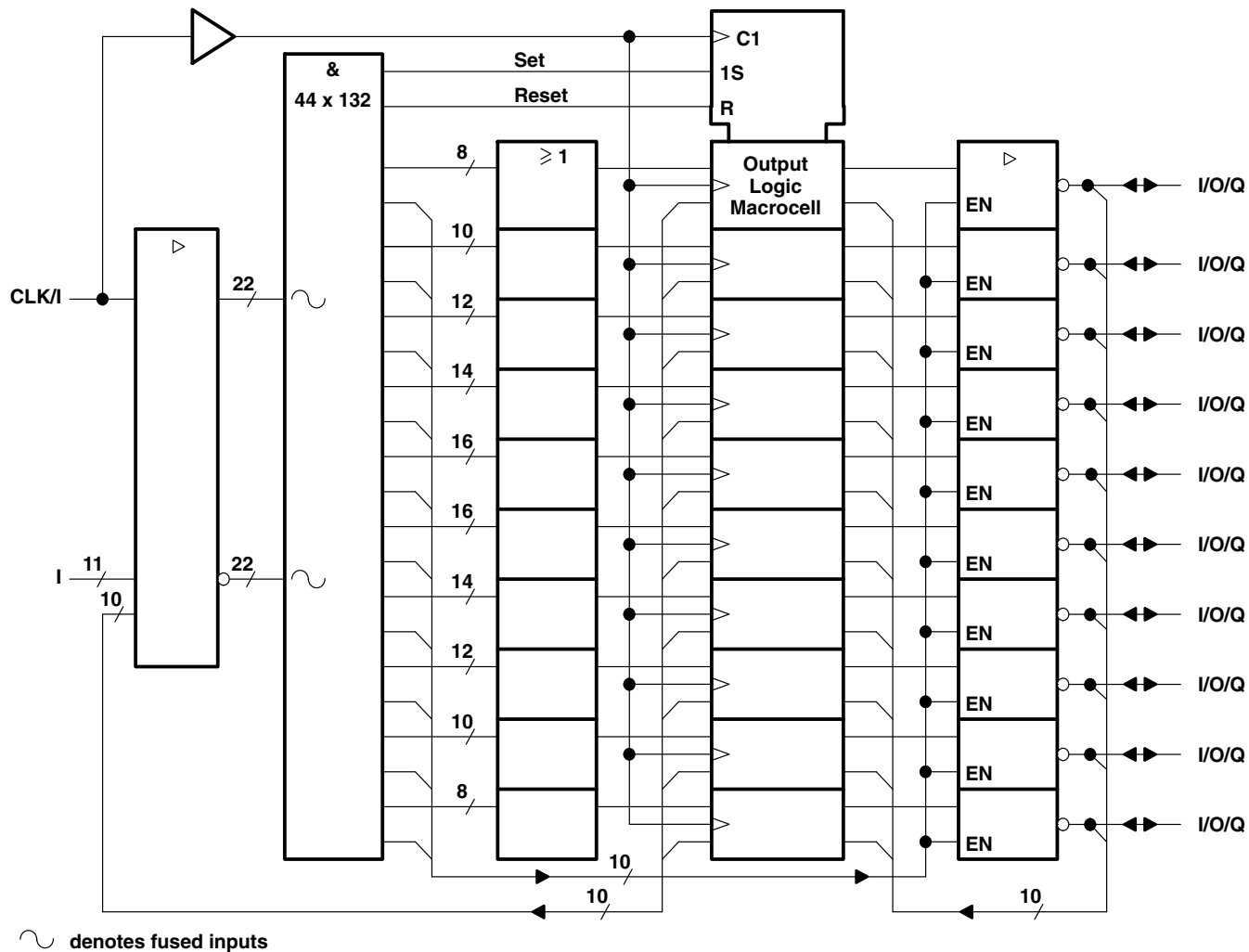
A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will appear to be open.

The TIBPAL22V10C and TIBPAL22V10AC are characterized for operation from 0°C to 75°C. The TIBPAL22V10AM is characterized for operation over the full military temperature range of –55°C to 125°C.

TIBPAL22V10C, TIBPAL22V10AC, TIBPAL22V10AM HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

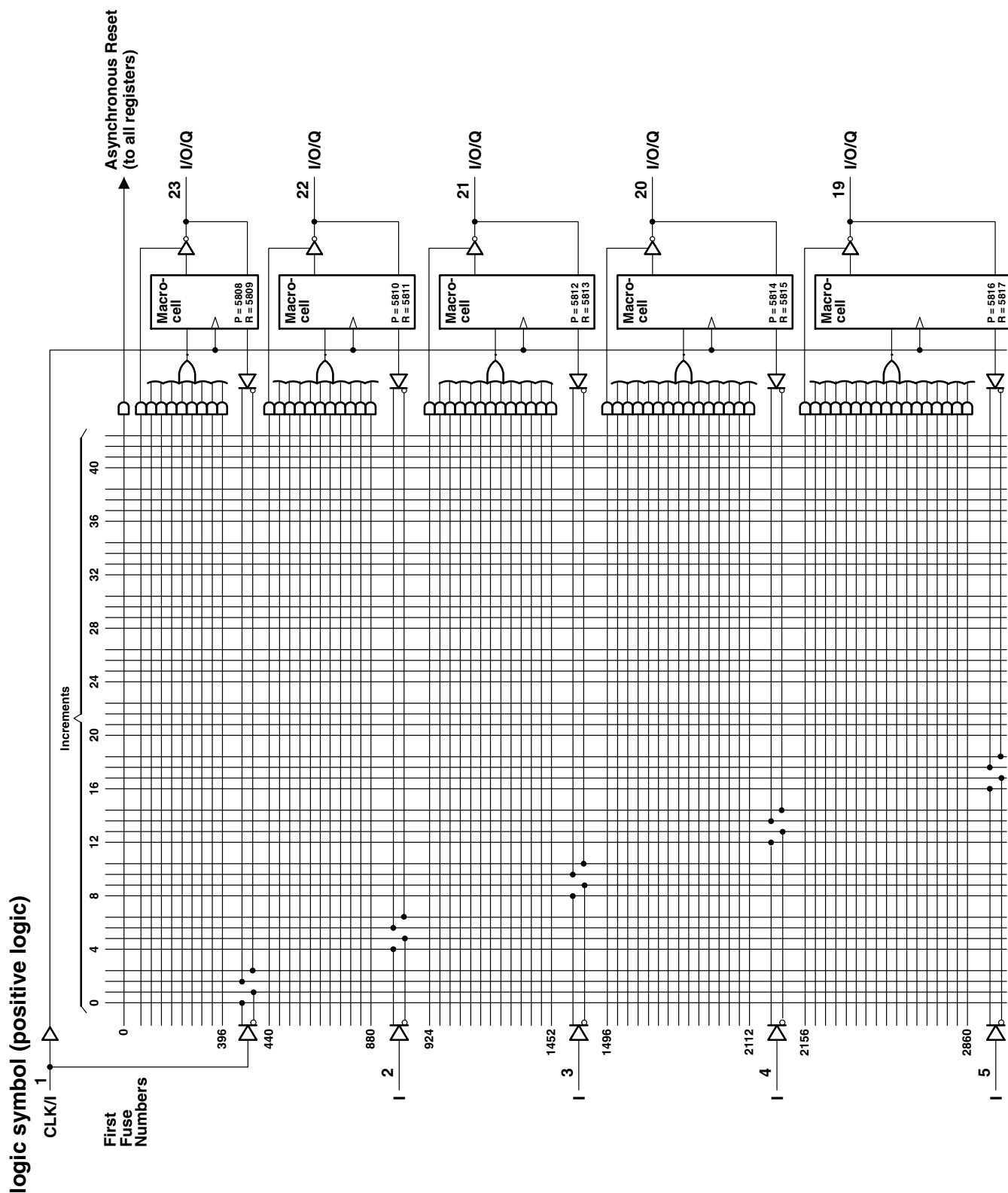
SRPS024A – OCTOBER 1986 – REVISED APRIL 2010

functional block diagram (positive logic)



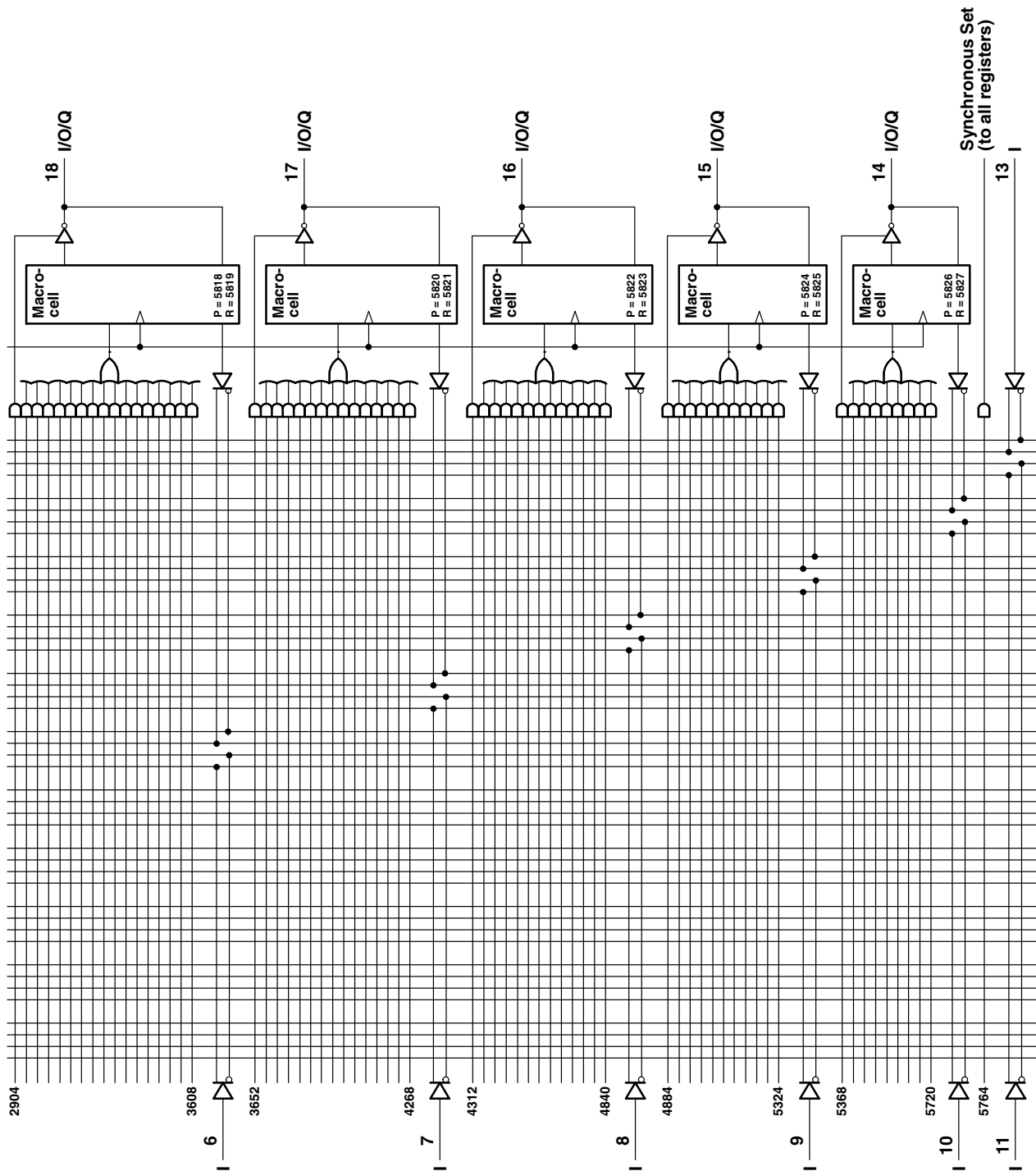
TIBPAL22V10C, TIBPAL22V10AC, TIBPAL22V10AM HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

SRPS024A – OCTOBER 1986 – REVISED APRIL 2010



TIBPAL22V10C, TIBPAL22V10AC, TIBPAL22V10AM HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

SRPS024A – OCTOBER 1986 – REVISED APRIL 2010



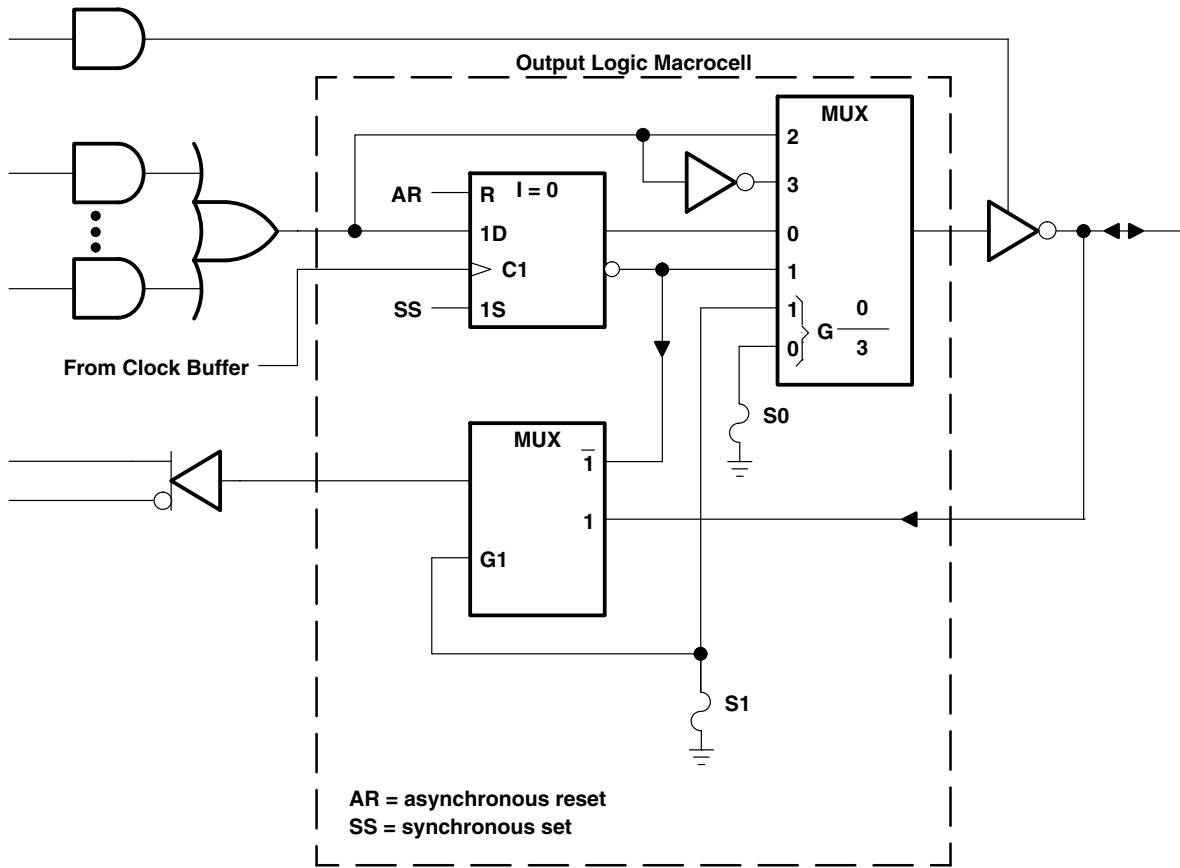
Fuse number = First fuse number + Increment
 Inside each MACROCELL the "P" fuse is the polarity fuse and the "R" fuse is the register fuse.



TIBPAL22V10C, TIBPAL22V10AC, TIBPAL22V10AM HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

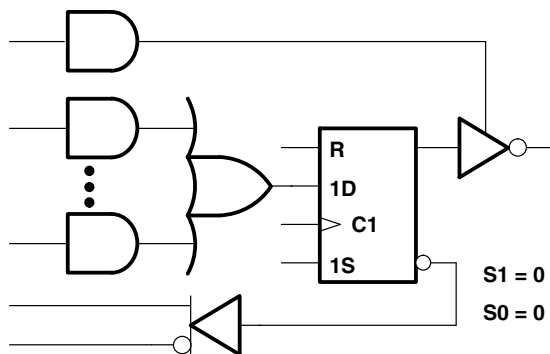
SRPS024A – OCTOBER 1986 – REVISED APRIL 2010

output logic macrocell diagram

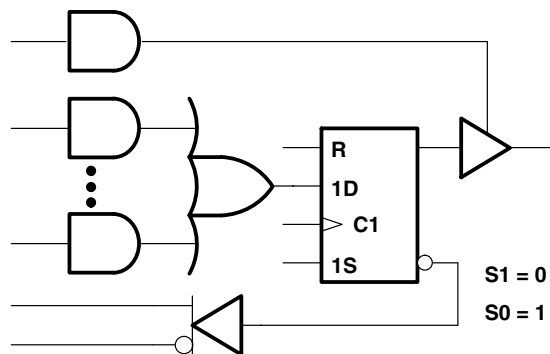


TIBPAL22V10C, TIBPAL22V10AC, TIBPAL22V10AM HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

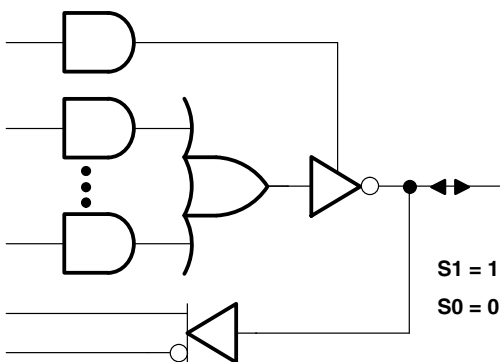
SRPS024A – OCTOBER 1986 – REVISED APRIL 2010



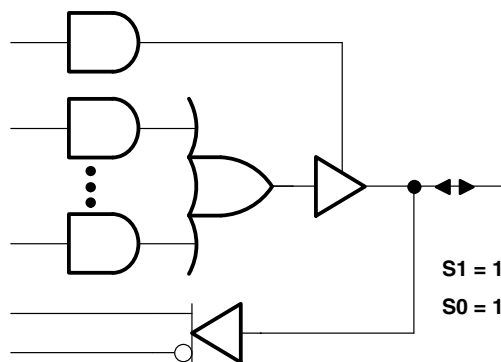
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUUSE SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse

S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

Figure 1. Resultant Macrocell Feedback and Output Logic After Programming

TIBPAL22V10C, TIBPAL22V10AC

HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

SRPS024A – OCTOBER 1986 – REVISED APRIL 2010

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	-5.5 V
Voltage range applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	-65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

		TIBPAL22V10C			TIBPAL22V10AC			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.75	5	5.25	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-3.2			-3.2	mA
I_{OL}	Low-level output current			16			16	mA
f_{clock}	Clock frequency†			18			28.5	MHz
t_w	Pulse duration	Clock high or low		25	15		ns	
		Asynchronous reset high or low		35	25			
t_{su}	Setup time before clock↑	Input		30	20		ns	
		Feedback		30	20			
		Synchronous set		30	25			
		Asynchronous reset low (inactive)		35	25			
t_h	Hold time, input, set, or feedback after clock↑	0			0			ns
T_A	Operating free-air temperature	0			75			°C

$$\dagger f_{clock} \text{ (with feedback)} = \frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}, \quad f_{clock} \text{ (without feedback)} = \frac{1}{t_w(\text{low}) + t_w(\text{high})}$$

TIBPAL22V10C, TIBPAL22V10AC HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

SRPS024A – OCTOBER 1986 – REVISED APRIL 2010

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS	TIBPAL22V10C		TIBPAL22V10AC		UNIT		
		MIN	TYP†	MAX	MIN		TYP†	MAX
V_{IK}	$V_{CC} = 4.75\text{ V}$, $I_I = -18\text{ mA}$			-1.2		-1.2	V	
V_{OH}	$V_{CC} = 4.75\text{ V}$, $I_{OH} = -3.2\text{ mA}$	2.4	3.5		2.4	3.5	V	
V_{OL}	$V_{CC} = 4.75\text{ V}$, $I_{OL} = 16\text{ mA}$		0.35	0.5		0.35	0.5	V
I_{OZH}	$V_{CC} = 5.25\text{ V}$, $V_O = 2.7\text{ V}$			0.1		0.1	mA	
I_{IL}	Any output			-100		-100	μA	
	Any I/O			-250		-250		
I_I	$V_{CC} = 5.25\text{ V}$, $V_I = 5.5\text{ V}$			1		1	mA	
I_{IH}	$V_{CC} = 5.25\text{ V}$, $V_I = 2.7\text{ V}$			25		25	μA	
I_{IL}	$V_{CC} = 5.25\text{ V}$, $V_I = 0.4\text{ V}$			-0.25		-0.25	mA	
I_{OS}^\ddagger	$V_{CC} = 5.25\text{ V}$, $V_O = 0.5\text{ V}$	-30		-90	-30	-90	mA	
I_{CC}	$V_{CC} = 5.25\text{ V}$, $V_I = \text{GND}$, Outputs open	120	180		120	180	mA	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TIBPAL22V10C		TIBPAL22V10AC		UNIT
				MIN	TYP†	MAX	MIN	
f_{max}^{\S}	With feedback		R1 = 300 Ω , R2 = 390 Ω , See Figure 4	18		28.5		MHz
t_{pd}	I, I/O	I/O		15	35	15	25	ns
t_{pd}	I, I/O (reset)	Q		15	40	15	30	ns
t_{pd}	CLK	Q		10	25	10	15	ns
t_{en}	I, I/O	I/O, Q		15	35	15	25	ns
t_{dis}	I, I/O	I/O, Q		15	35	15	25	ns

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

$$\S f_{max} \text{ (with feedback)} = \frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}, f_{max} \text{ (without feedback)} = \frac{1}{t_w(\text{low}) + t_w(\text{high})}$$

TIBPAL22V10AM**HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS**

SRPS024A – OCTOBER 1986 – REVISED APRIL 2010

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	-5.5 V
Voltage range applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	-55°C to 125°C
Storage temperature range	-65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-2	mA
I_{OL}	Low-level output current			12	mA
f_{clock}	Clock frequency†			22	MHz
t_w	Pulse duration	Clock high or low		20	ns
		Asynchronous reset high or low		30	
t_{su}	Setup time before clock↑	Input		25	ns
		Feedback		25	
		Synchronous set		25	
		Asynchronous reset low (inactive)		30	
t_h	Hold time, input, set, or feedback after clock↑	0			ns
T_A	Operating free-air temperature	-55		125	°C

$$\dagger f_{clock} \text{ (with feedback)} = \frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}; f_{clock} \text{ (without feedback)} = \frac{1}{t_w(\text{low}) + t_w(\text{high})}$$

TIBPAL22V10AM

HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

SRPS024A – OCTOBER 1986 – REVISED APRIL 2010

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -2\text{ mA}$	2.4	3.5		V
V_{OL}	$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 12\text{ mA}$		0.25	0.5	V
I_{OZH}	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.7\text{ V}$			0.1	mA
I_{OZL}	$V_{CC} = 5.5\text{ V}$,	$V_O = 0.4\text{ V}$			-100	μA
I_I	$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V}$			1	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			25	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$			-0.25	mA
I_{OS}^\ddagger	$V_{CC} = 5.5\text{ V}$,	$V_O = 0.5\text{ V}$	-30		-90	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$,	$V_I = \text{GND}$, Outputs open		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{\max}^{\S}	With feedback		$R1 = 390\ \Omega$, $R2 = 750\ \Omega$, See Figure 4	22			MHz
t_{pd}	I, I/O	I/O		15	30		ns
t_{pd}	I, I/O (reset)	Q		15	35		ns
t_{pd}	CLK	Q		10	20		ns
t_{en}	I, I/O	I/O, Q		15	30		ns
t_{dis}	I, I/O	I/O, Q		15	30		ns

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

$$\S f_{\max} (\text{with feedback}) = \frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}, \quad f_{\max} (\text{without feedback}) = \frac{1}{t_w(\text{low}) + t_w(\text{high})}$$

TIBPAL22V10C, TIBPAL22V10AC, TIBPAL22V10AM

HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

SRPS024A – OCTOBER 1986 – REVISED APRIL 2010

preload procedure for registered outputs (see Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below:

- Step 1. With V_{CC} at 5 V and pin 1 at V_{IL} , raise pin 13 to V_{IHH} .
- Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
- Step 3. Pulse pin 1, clocking in preload data.
- Step 4. Remove output voltage, then lower pin 13 to V_{IL} . Preload can be verified by observing the voltage level at the output pin.

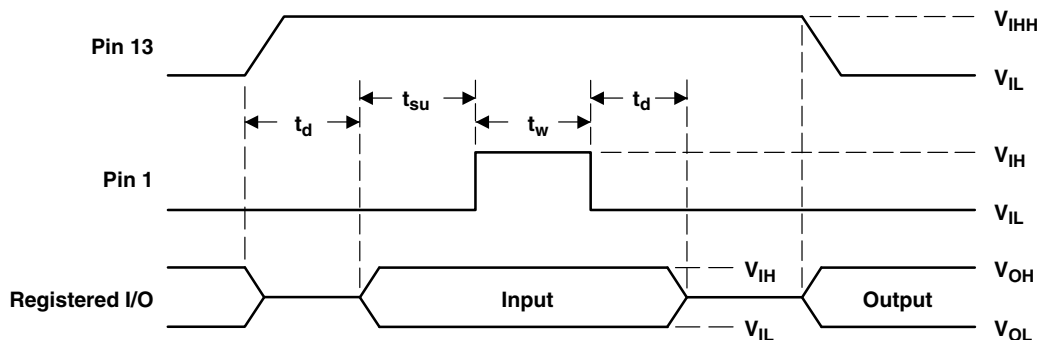


Figure 2. Preload Waveforms

NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip-carrier socket adapter is not used, pin numbers must be changed accordingly.

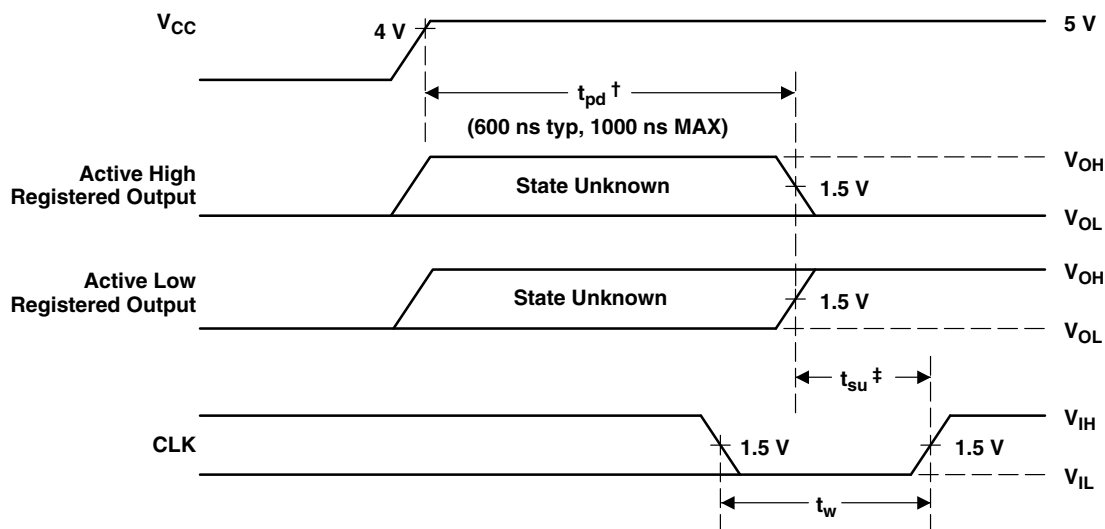
3. $t_d = t_{su} = t_w = 100$ ns to 1000 ns. $V_{IHH} = 10.25$ V to 10.75 V.

TIBPAL22V10C, TIBPAL22V10AC, TIBPAL22V10AM HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

SRPS024A – OCTOBER 1986 – REVISED APRIL 2010

power-up reset

Following power up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.

‡ This is the setup time for input or feedback.

Figure 3. Power-Up Reset Waveforms

programming information

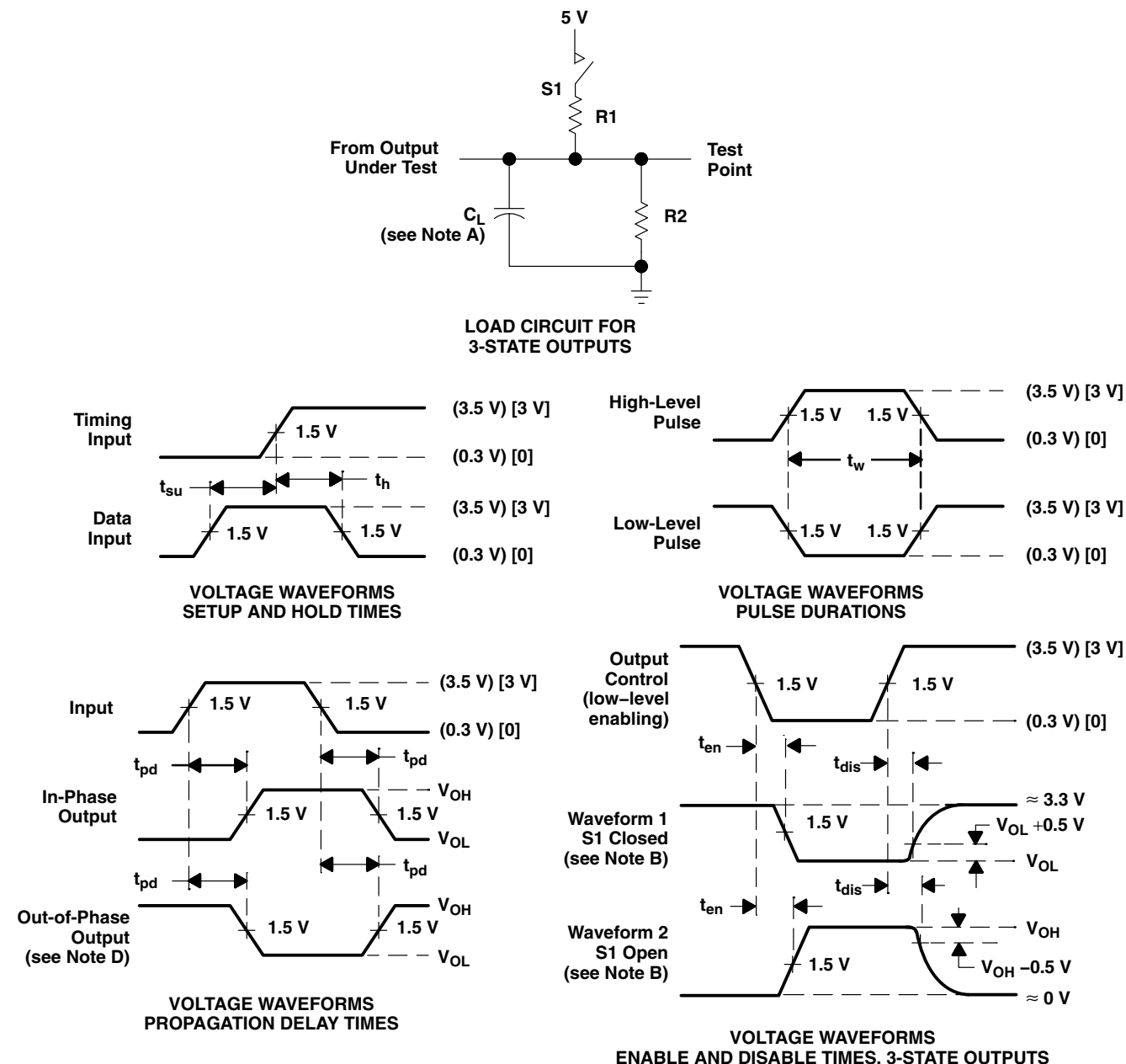
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

TIBPAL22V10C, TIBPAL22V10AC, TIBPAL22V10AM HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

SRPS024A – OCTOBER 1986 – REVISED APRIL 2010

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses have the following characteristics: For C suffix, use the voltage levels indicated in parentheses (). PRR \leq 1 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%. For M suffix, use the voltage levels indicated in brackets []. PRR \leq 10 MHz, t_r and $t_f \leq 2$ ns, duty cycle = 50%.
- D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
- E. Equivalent loads may be used for testing.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-86053013A	LIFEBUY	LCCC	FK	28		TBD	Call TI	Call TI	-55 to 125	5962- 86053013A TIBPAL22 V10AMFKB	
5962-8605301KA	LIFEBUY	CFP	W	24		TBD	Call TI	Call TI	-55 to 125	5962-8605301KA TIBPAL22V10AMW B	
TIBPAL22V10AMFKB	LIFEBUY	LCCC	FK	28		TBD	Call TI	Call TI	-55 to 125	5962- 86053013A TIBPAL22 V10AMFKB	
TIBPAL22V10AMJT	LIFEBUY	CDIP	JT	24		TBD	Call TI	Call TI	-55 to 125	TIBPAL22V10AMJ T	
TIBPAL22V10AMWB	LIFEBUY	CFP	W	24		TBD	Call TI	Call TI	-55 to 125	5962-8605301KA TIBPAL22V10AMW B	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

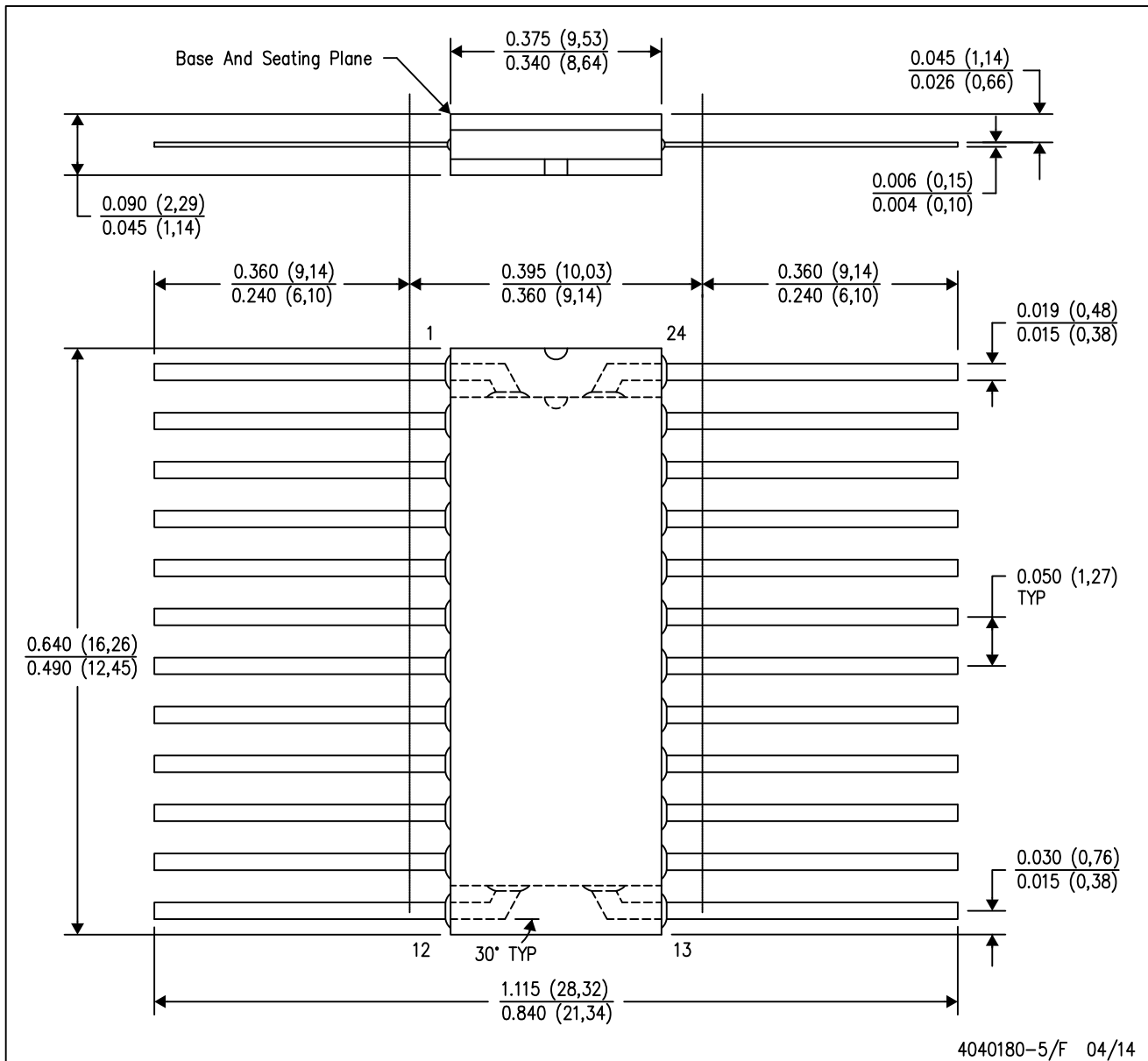


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.