CY7C332

Registered Combinatorial EPLD

Features

- 12 I/O macrocells each having:
  - Registered, latched, or transparent array input
  - A choice of two clock sources
  - Global or local output enable (OE)
  - Up to 19 product terms (PTs) per output
  - Product term (PT) output polarity control
- 192 product terms with variable distribution to macrocells
  - An average of 14 PTs per macrocell sum node
- Two clock inputs with configurable polarity control
- 13 input macrocells, each having:
  - Complementary input
  - Register, latch, or transparent access
  - Two clock sources
- 15 ns t_{PD} max.
- Low power
  - 120 mA typical I_{CC} quiescent
  - 180 mA max.
  - Power-saving "Miser Bit" feature
- Security fuse
- 28-pin slim-line package; also available in 28-pin PLCC
- UV-erasable and reprogrammable
- Programming and operation 100% testable

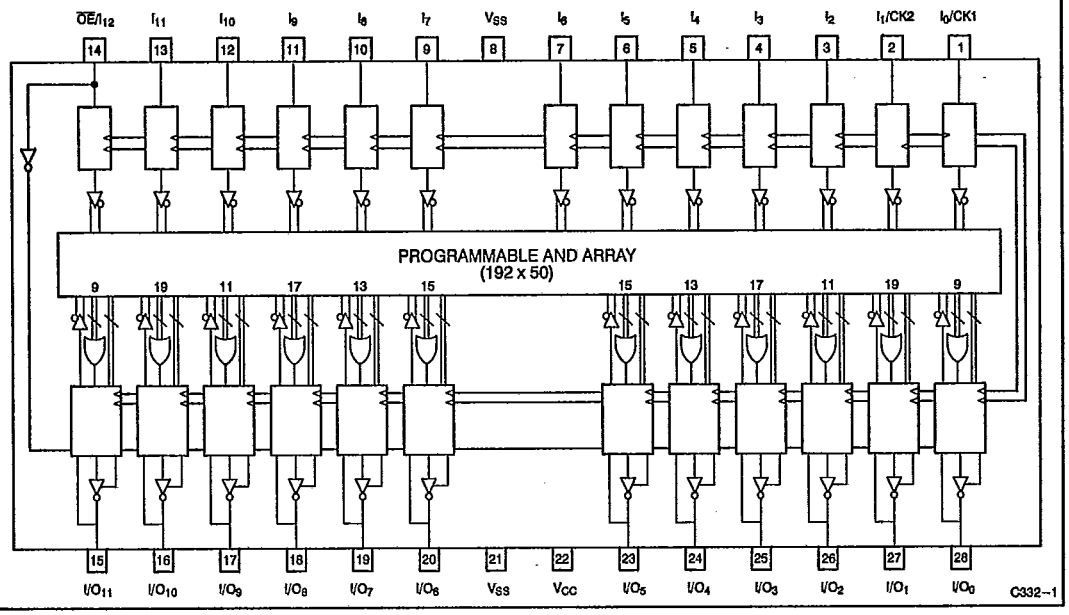
Functional Description

The CY7C332 is a versatile combinatorial PLD with I/O registers on-board. There are 25 array inputs; each has a macrocell that may be configured as a register, latch, or simple buffer. Outputs have polarity and three-state control product terms. The allocation of product terms to I/O macrocells is varied so that functions of up to 19 product terms can be accommodated.

I/O Resources

Pins 1 through 7 and 9 through 14 function as dedicated array inputs. Pins 1 and 2 function as input clocks as well as normal inputs. Pin 14 functions as a global output enable as well as a normal input.

Logic Block Diagram

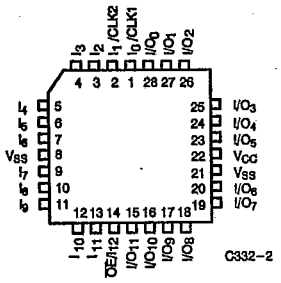


Selection Guide

Generic Part Number	I_{CC1} (mA)		t_{ICO}/t_{PD} (ns)		t_{IS} (ns)	
	Commercial	Military	Commercial	Military	Commercial	Military
7C332–15	130		18/15		3	
7C332–20	120	160	20	23/20	3	4
7C332–25	120	150	25	25	3	4
7C332–30		150		30		4

Pin Configuration

LCC/PLCC
Top View



I/O Resources (continued)

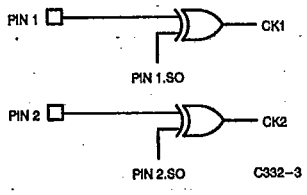
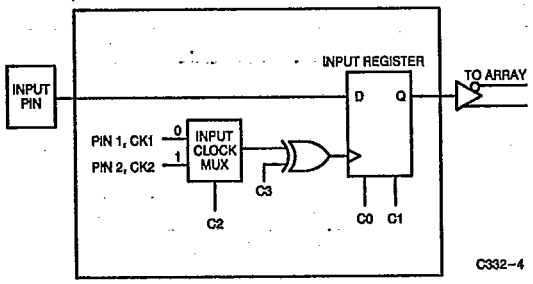


Figure 1. CK1 and CK2

Pins 15 through 20 and 23 through 28 are connected to I/O macrocells and may be combinatorial outputs as well as registered or direct inputs.

Input Macrocell



C3	C2	C1	C0	Input Register Option
X	X	0	0	Combinatorial
X	X	0	1	Illegal
0	0	1	1	Registered, CLK1, Rising Edge
0	1	1	1	Registered, CLK2, Rising Edge
1	0	1	1	Registered, CLK1, Falling Edge
1	1	1	1	Registered, CLK2, Falling Edge
0	0	1	0	Latched, CLK1, LOW Transparent
0	1	1	0	Latched, CLK2, LOW Transparent
1	0	1	0	Latched, CLK1, HIGH Transparent
1	1	1	0	Latched, CLK2, HIGH Transparent

Figure 2. Input Macrocell

There are 13 input macrocells, corresponding to pins 1 through 7 and 9 through 14. Each macrocell has a clock that is selected to come from either pin 1 or pin 2 by configuration bit C2. Pins 1 and 2 are clocks as well as normal inputs. There is no C2 configuration bit for either of these two input macrocells. Macrocells connected to pins 1 and 2 do not have a clock choice, but each has a clock coming from the other pin.

Each input macrocell can be configured as a register, latch, or simple buffer (transparent path) to the product term array. For a register the configuration bit, C0, is 1 (programmed) and C1 is 1. For a latch, C0 is 0 and C1 is 1. If both C0 and C1 are 0 (unprogrammed), then the macrocell is completely transparent.

Configurationbit C3 determines the clock edge on which the register is triggered or the polarity for which the latch is asserted. This clock polarity can be programmed independently for each input register. These confirmation options are available on all inputs, including those in the I/O macrocell.

If C3 is 0 (unprogrammed), the clock will be rising-edge triggered (register mode) or HIGH asserted (latch mode). If C3 is 1 (programmed), the clock will be falling-edge triggered (register mode) or LOW asserted (latch mode).

I/O Macrocell

There are 12 I/O macrocells corresponding to pins 15 through 20 and 23 through 28. Each macrocell has a three-state output control and XOR product term to dynamically control polarity, and a configurable feedback path.

For each I/O macrocell, the three-state control for the output may be configured two ways. If the configuration bit, C4, is a 1 (programmed), then the global OE signal is selected. Otherwise, the OE product term is used.

For each I/O macrocell, the input/feedback path may be configured as a register, latch, or shunt. There are two configuration bits per I/O macrocell that configure the feedback path. These are programmed in the same way as for the input macrocells.

For each I/O macrocell, the input register clock (or Latch Enable) that is used for the input/feedback path may be selected as pin 1 (select bit, C2, not programmed) or pin 2 (select bit, C2, programmed).

Array Allocation to Output Macrocell

The number of product terms in each output macrocell sum is position dependent. *Table 1* summarizes the allocation.

Table 1. Product Term Allocation in Output Macrocell

Macrocell	Pin Number	Product Terms
0	28	9
1	27	19
2	26	11
3	25	17
4	24	13
5	23	15
6	20	15
7	19	13
8	18	17
9	17	11
10	16	19
11	15	9

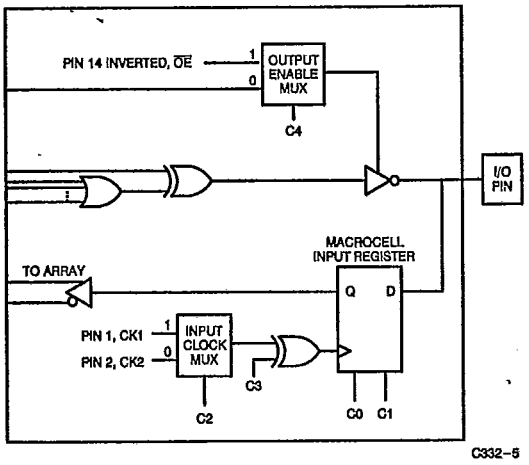


Figure 3. Input Macrocell

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pins 8 and 21) ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 12 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

DC Programming Voltage 13.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ± 10%
Military[1]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = – 3.2 mA	Commercial	2.4		V
			I_{OH} = – 2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA	Commercial		0.5	V
			I_{OL} = 8 mA	Military			
V_{IH}	Input HIGH Voltage	Guaranteed HIGH Input, all Inputs[2]			2.2		V
V_{IL}	Input LOW Voltage	Guaranteed LOW Input, all Inputs[3]				0.8	V
I_{IX}	Input Leakage Current	V_{SS} < V_{IN} < V_{CC}, V_{CC} = Max.			– 10	+10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{SS} < V_{OUT} < V_{CC},			– 40	+40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3]			– 30	– 90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open		Commercial		120	mA
				Commercial – 15		130	
				Military		150	
				Military – 20		160	
I_{CC2}	Power Supply Current at Frequency[4, 5]	V_{CC} = Max. Outputs Disabled (In High Z State) Device Operating at f_{MAX} External (f_{MAX1})		Commercial		180	mA
				Military		200	

Notes:

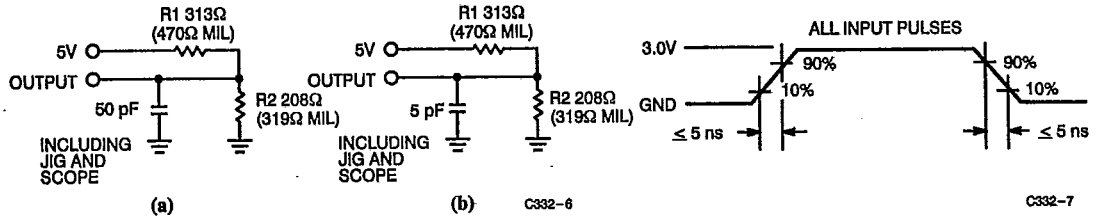
1. T_A is the "instant on" case temperature.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested by periodic sampling of production product.
5. Refer to *Figure 4* configuration 2.

Capacitance[6]

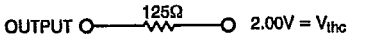
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz	10	pF

Note:
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

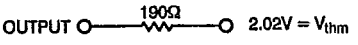


Equivalent to: THÉVENIN EQUIVALENT (Commercial)

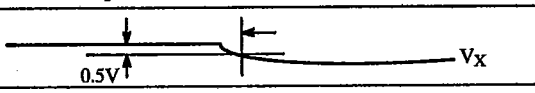
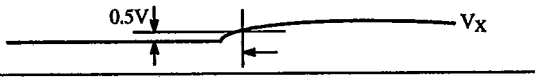
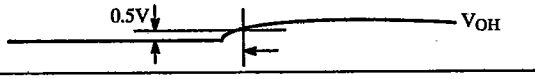
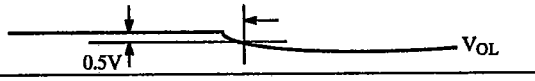
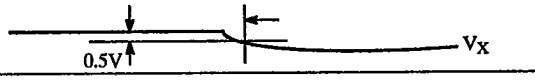
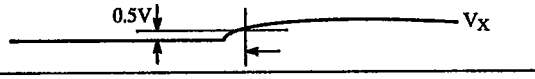
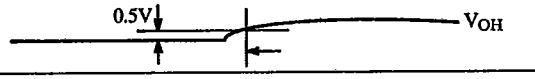
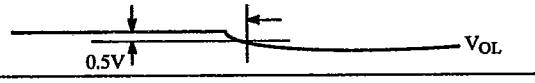


C332-8

Equivalent to: THÉVENIN EQUIVALENT (Military)



C332-9

Parameter	V_X	Output Waveform—Measurement Level
$t_{PXZ(-)}$	1.5V	 C332-10
$t_{PXZ(+)}$	2.6V	 C332-11
$t_{PZX(+)}$	V_{thc}	 C332-12
$t_{PZX(-)}$	V_{thc}	 C332-13
$t_{ER(-)}$	1.5V	 C332-14
$t_{ER(+)}$	2.6V	 C332-15
$t_{EA(+)}$	V_{thc}	 C332-16
$t_{EA(-)}$	V_{thc}	 C332-17

(c) Test Waveforms and Measurement Levels

Switching Characteristics Over the Operating Range[3]

Parameters	Description	Commercial						Commercial						Units
		−15[7]		−20		−25		−20[7]		−25		−30		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[8]		15		20		25		20		25		30	ns
t_{ICO}	Input Register Clock to Output Delay[6]		18		20		25		23		25		30	ns
t_{IS}	Input or Feedback Set-Up Time to Input Register Clock[6]	3		3		3		4		4		4		ns
t_{IH}	Input Register Hold Time[6]	3		3		3		4		4		4		ns
t_{EA}	Input to Output Enable Delay[9, 10]		20		20		25		25		25		30	ns
t_{ER}	Input to Output Disable Delay[9, 10]		20		20		25		25		25		30	ns
t_{PZX}	Pin 14 Enable to Output Enable Delay[9, 11]		15		15		20		20		20		25	ns
t_{PXZ}	Pin 14 Disable to Output Disable Delay[9, 11]		15		15		20		20		20		25	ns
t_{WH}	Input Clock Width High[4, 6]	9		10		10		10		10		12		ns
t_{WL}	Input Clock Width Low[4, 6]	9		10		10		10		10		12		ns
t_{IOH}	Output Data Stable Time from Input Register Clock Input[6, 7]	3		3		3		3		4		4		ns
$t_{IOH} - t_{IH}$	Output Data Stable Time This Device Minus I/P Reg Hold Time Same Device[7, 12, 13]	0		0		0		0		0		0		ns
$t_{IOH} - t_{IH}$ 33x	Output Data Stable Time Minus I/P Reg Hold Time 7C330 and 7C332 Device[7, 14]	0		0		0		0		0		0		ns
t_{PE}	External Clock Period ($t_{ICO} + t_{IS}$)[6]	21		23		28		27		29		34		ns
f_{MAX1}	Maximum External Operating Frequency ($1/(t_{ICO} + t_{IS})$)[6]	47.6		43.4		35.7		37		34.4		29.4		MHz
f_{MAX}	Maximum Frequency Data Path[6]	55.5		50.0		40.0		50.0		40.0		33.3		MHz

Notes:

7. Preliminary specifications.
8. Refer to *Figure 3* configuration 1.
9. Part (a) of AC Test Loads and Waveforms is used for all parameters except t_{EA}, t_{ER}, t_{PZX}, and t_{PXZ}, which use part (b). Part (c) shows test waveform and measurement reference levels.
10. Refer to *Figure 4* configuration 3.
11. Refer to *Figure 4* configuration 4.
12. Refer to *Figure 4* configuration 5.
13. This specification is intended to guarantee that configuration 5 of *Figure 4* with input registered feedback can be operated with all input register clocks controlled by the same source. These parameters are tested by periodic sampling of production product.
14. This specification is intended to guarantee interface compatibility of the other members of the CY7C330 family with the CY7C332. This specification is met for the devices noted operating at the same ambient temperature and at the same power supply voltage. These parameters are tested periodically by sampling of production product.

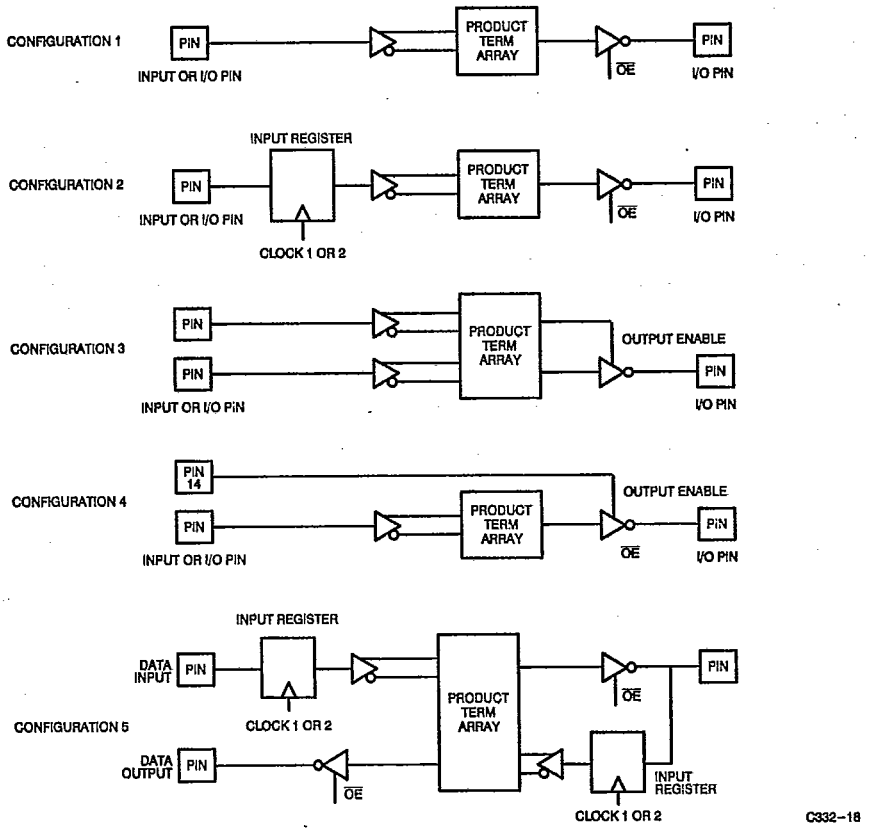
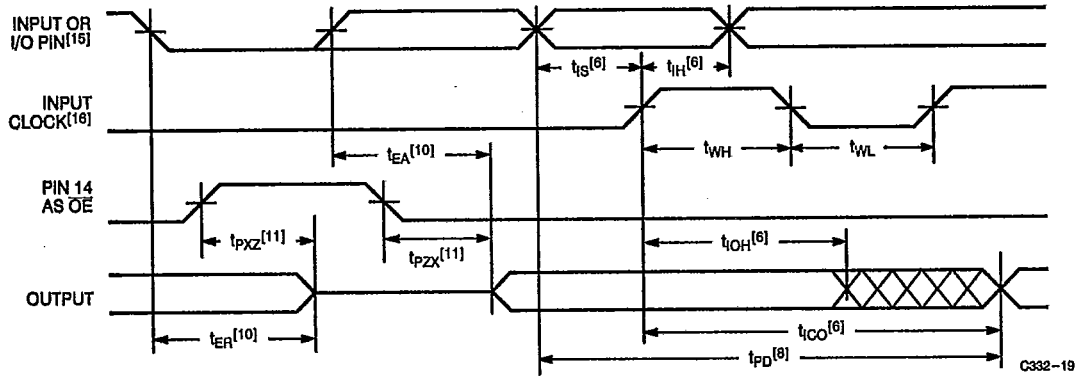


Figure 4. Timing Configurations

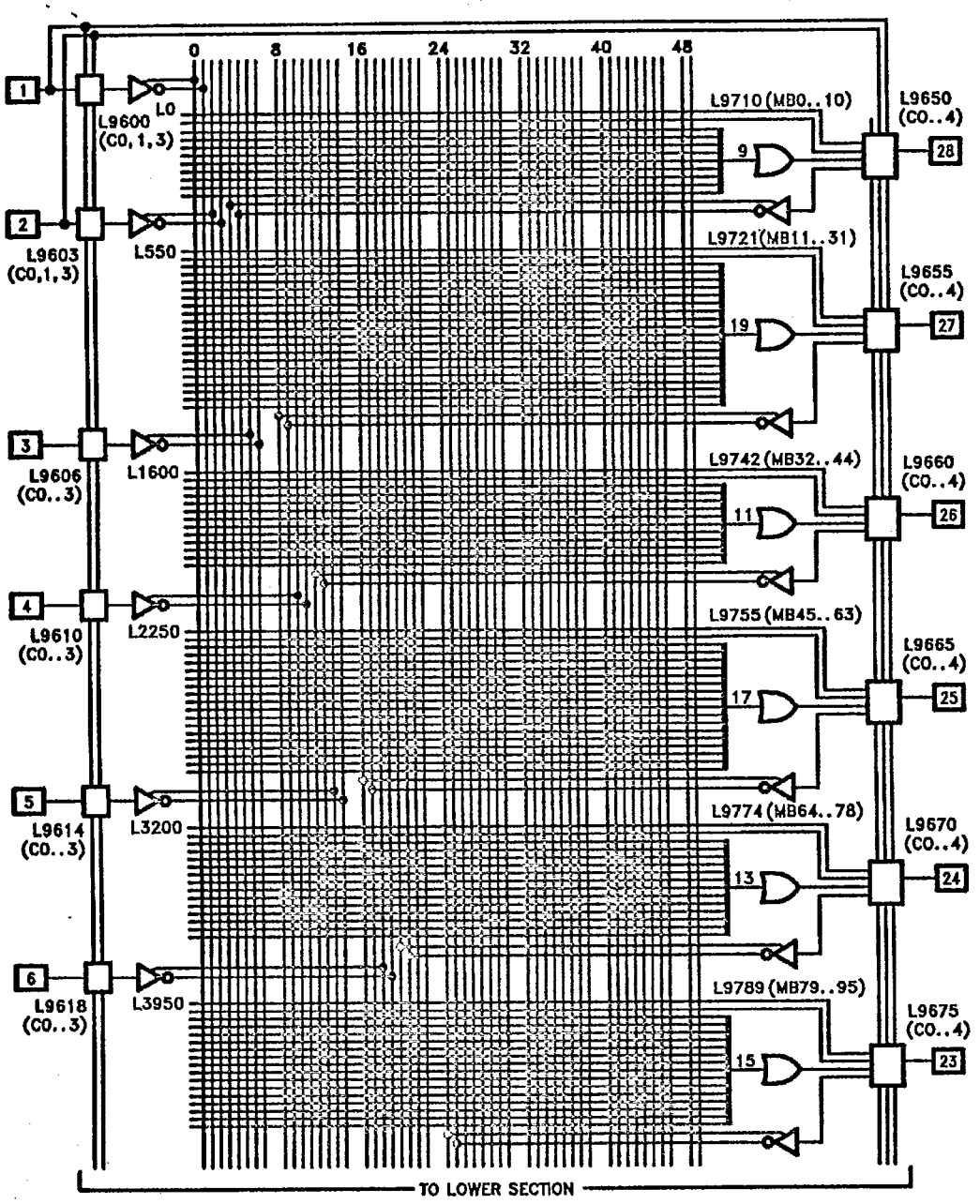
Switching Waveforms



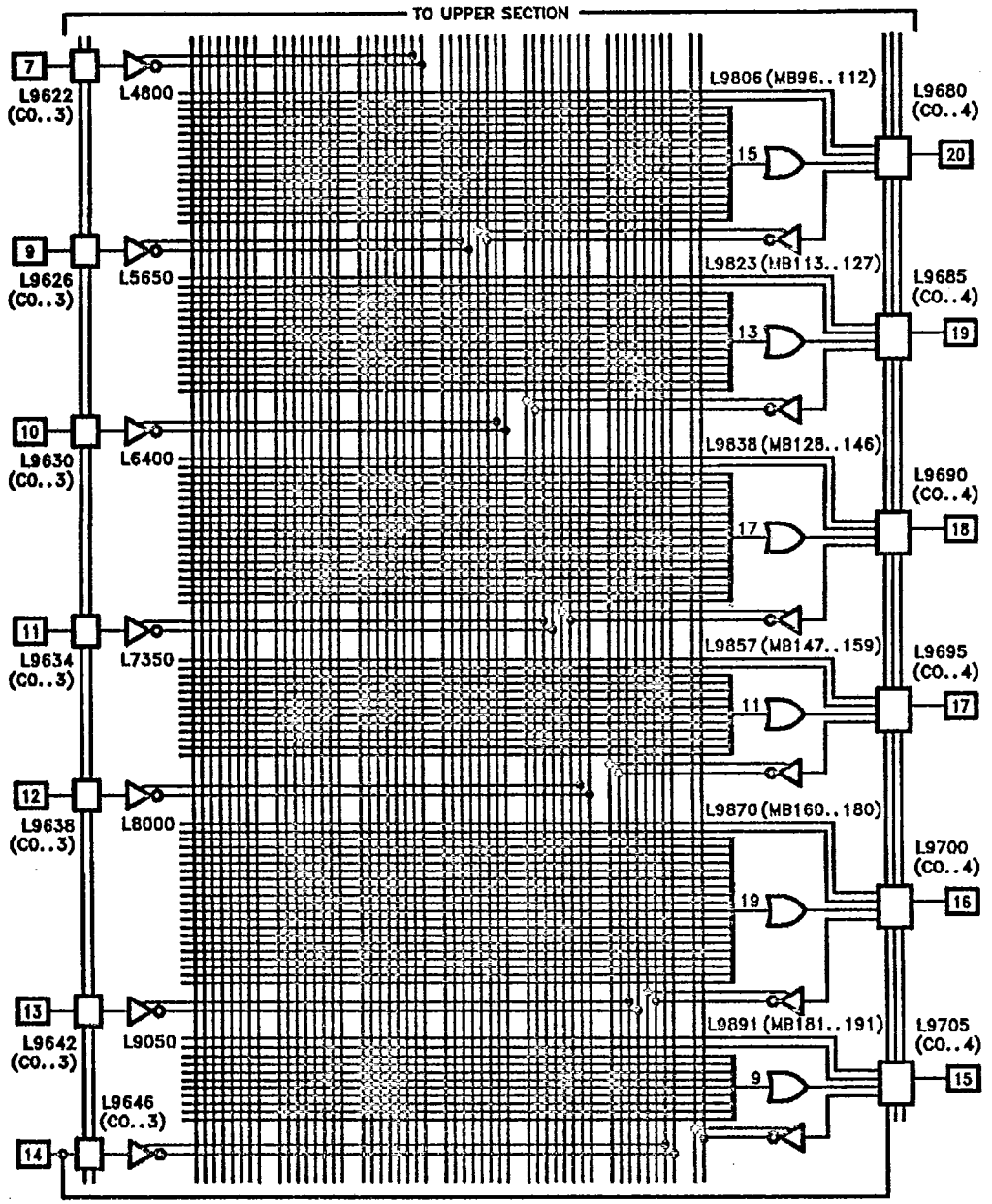
Notes:

15. Because OE can be controlled by the $\overline{OE}$ product term, input signal polarity for control of OE can be of either polarity. Internally the product term $\overline{OE}$ signal is active HIGH.
16. Since the input register clock polarity is programmable, the input clock may be rising- or falling-edge triggered.

CY7C332 Logic Diagram (Upper Half)



CY7C332 Logic Diagram (Lower Half)



PLDs

Ordering Information

I_{CC1} (max)	t_{ICO}/t_{PD} (ns)	t_{IS} (ns)	t_{IH} (ns)	Ordering Code	Package Type	Operating Range
120	18/15	3	3	CY7C332–15HC	H64	Commercial
				CY7C332–15JC	J64	
				CY7C332–15PC	P21	
				CY7C332–15WC	W22	
120	20	3	3	CY7C332–20HC	H64	Commercial
				CY7C332–20JC	J64	
				CY7C332–20PC	P21	
				CY7C332–20WC	W22	
160	23/20	4	4	CY7C332–20DMB	D22	Military
				CY7C332–20HMB	H64	
				CY7C332–20LMB	L64	
				CY7C332–20QMB	Q64	
				CY7C332–20TMB	T74	
				CY7C332–20WMB	W22	
120	25	3	3	CY7C332–25HC	H64	Commercial
				CY7C332–25JC	J64	
				CY7C332–25PC	P21	
				CY7C332–25WC	W22	
150	25	4	4	CY7C332–25DMB	D22	Military
				CY7C332–25HMB	H64	
				CY7C332–25LMB	L64	
				CY7C332–25QMB	Q64	
				CY7C332–25TMB	T74	
				CY7C332–25WMB	W22	
150	30	4	4	CY7C332–30DMB	D22	Military
				CY7C332–30HMB	H64	
				CY7C332–30LMB	L64	
				CY7C332–30QMB	Q64	
				CY7C332–30TMB	T74	
				CY7C332–30WMB	W22	

T-46-19-09

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{IS}	7, 8, 9, 10, 11
t_{IH}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{WL}	7, 8, 9, 10, 11
t_{ICO}	7, 8, 9, 10, 11
t_{PD}	7, 8, 9, 10, 11
t_{PXZ}	7, 8, 9, 10, 11
t_{PZX}	7, 8, 9, 10, 11
t_{ER}	7, 8, 9, 10, 11
t_{EA}	7, 8, 9, 10, 11

Document #: 38–00067–C