

### **Rochester Electronics Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

### **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

# TIBPAL20L10-30C, TIBPAL20X4-30C, TIBPAL20X8-30C, TIBPAL20X10-30C HIGH-PERFORMANCE EXCLUSIVE-OR *IMPACT™* PAL® CIRCUITS

D2920, DECEMBER 1987

- Functionally Equivalent to MMI PAL<sup>®</sup> Series 24XA
- Preload Capability on Output Registers Simplifies Testing
- Power-Up Clear on Registered Devices
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
*PAL20L10	12	2	0	8
*PAL20X4	10	0	4 (3-state buffers)	6
*PAL20X8	10	0	8 (3-state buffers)	2
*PAL20X10	10	0	10 (3-state buffers)	0

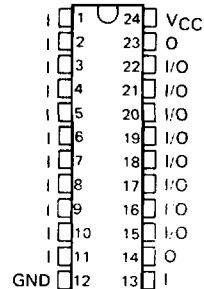
## description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These *IMPACT™* circuits combine the latest Advanced Low-Power Schottky<sup>†</sup> technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

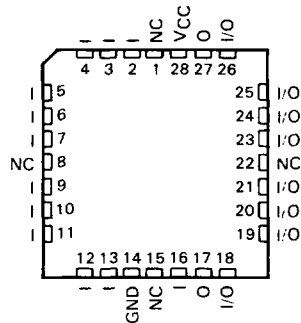
All of the registered outputs are set to a low level during power-up. In addition, extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20' C suffix devices are characterized for operation from 0°C to 75°C.

TIBPAL20L10'  
C SUFFIX . . . JT OR NT PACKAGE  
(TOP VIEW)



TIBPAL20L10'  
C SUFFIX . . . FN PACKAGE  
(TOP VIEW)



NC—No internal connection  
Pin assignments in operating mode

2

Data Sheets

IMPACT is a trademark of Texas Instruments Incorporated.

PAL is a registered trademark of Monolithic Memories Inc.

<sup>†</sup>Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS  
INSTRUMENTS

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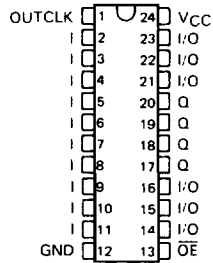
2-127

**TIBPAL20X4-30C, TIBPAL20X8-30C, TIBPAL20X10-30C  
HIGH-PERFORMANCE EXCLUSIVE-OR *IMPACT™* PAL® CIRCUITS**

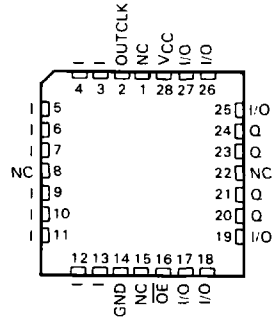
**2**

**Data Sheets**

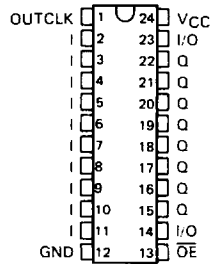
**TIBPAL20X4'**  
C SUFFIX . . . JT OR NT PACKAGE  
(TOP VIEW)



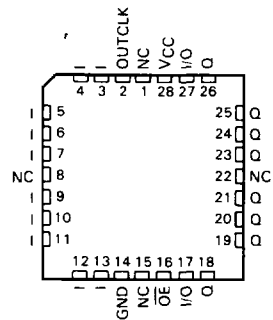
**TIBPAL20X4'**  
C SUFFIX . . . FN PACKAGE  
(TOP VIEW)



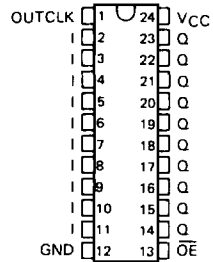
**TIBPAL20X8'**  
C SUFFIX . . . JT OR NT PACKAGE  
(TOP VIEW)



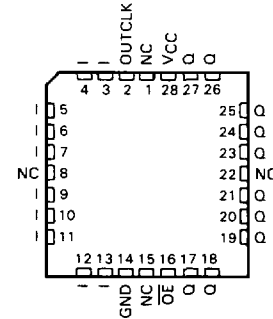
**TIBPAL20X8'**  
C SUFFIX . . . FN PACKAGE  
(TOP VIEW)



**TIBPAL20X10'**  
C SUFFIX . . . JT OR NT PACKAGE  
(TOP VIEW)



**TIBPAL20X10'**  
C SUFFIX . . . FN PACKAGE  
(TOP VIEW)

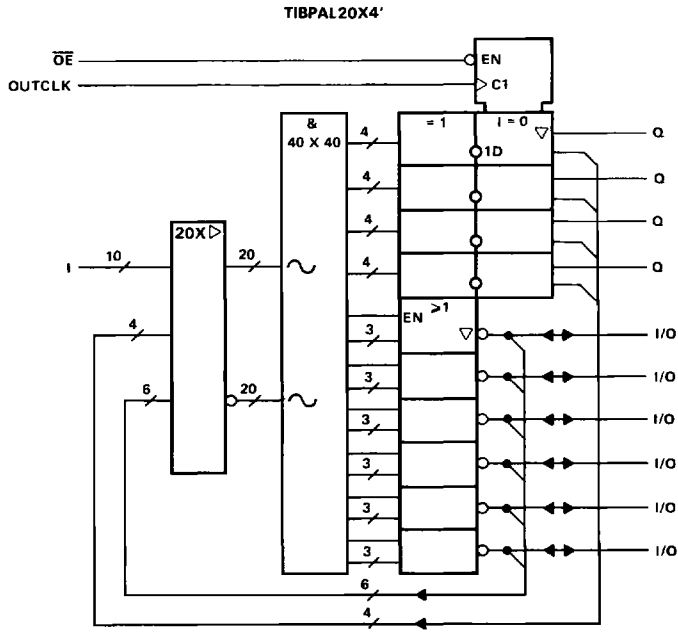
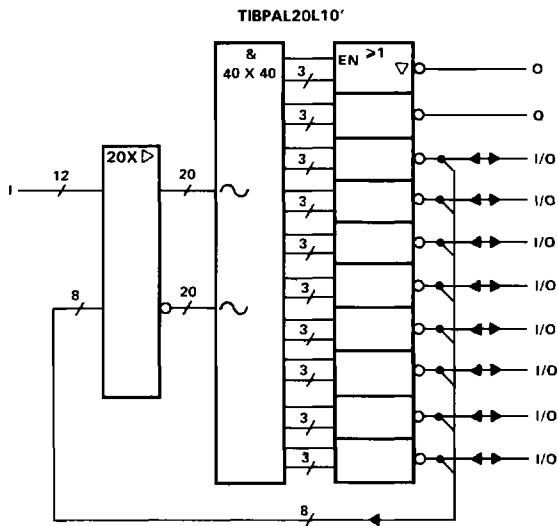


Pin assignments in operating mode

NC—No internal connection

**TIBPAL20L10-30C, TIBPAL20X4-30C**  
**HIGH-PERFORMANCE EXCLUSIVE-OR IMPACT™ PAL® CIRCUITS**

functional block diagrams (positive logic)



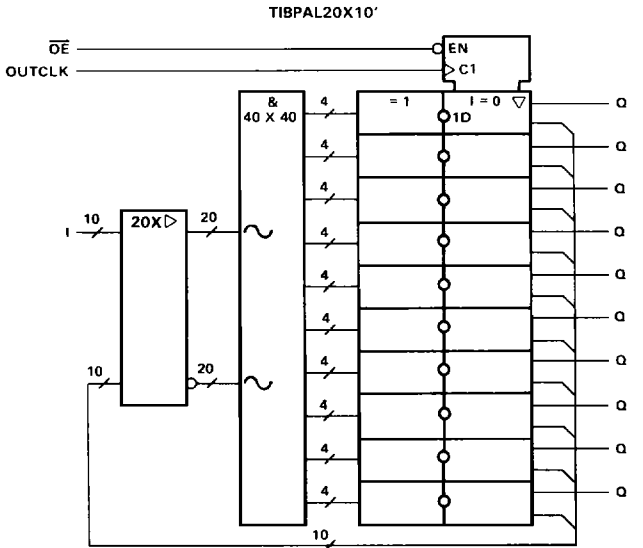
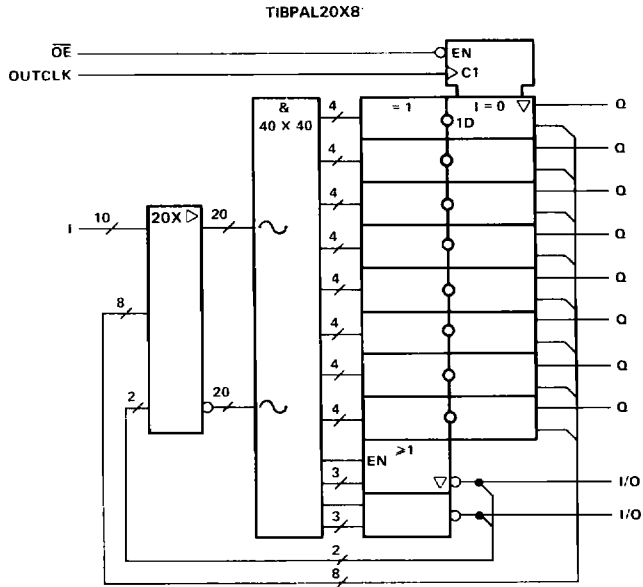
~ denotes fused inputs

**2**  
Data Sheets

**TIBPAL20X8-30C, TIBPAL20X10-30C  
HIGH-PERFORMANCE EXCLUSIVE-OR IMPACT™ PAL® CIRCUITS**

functional block diagrams (positive logic)

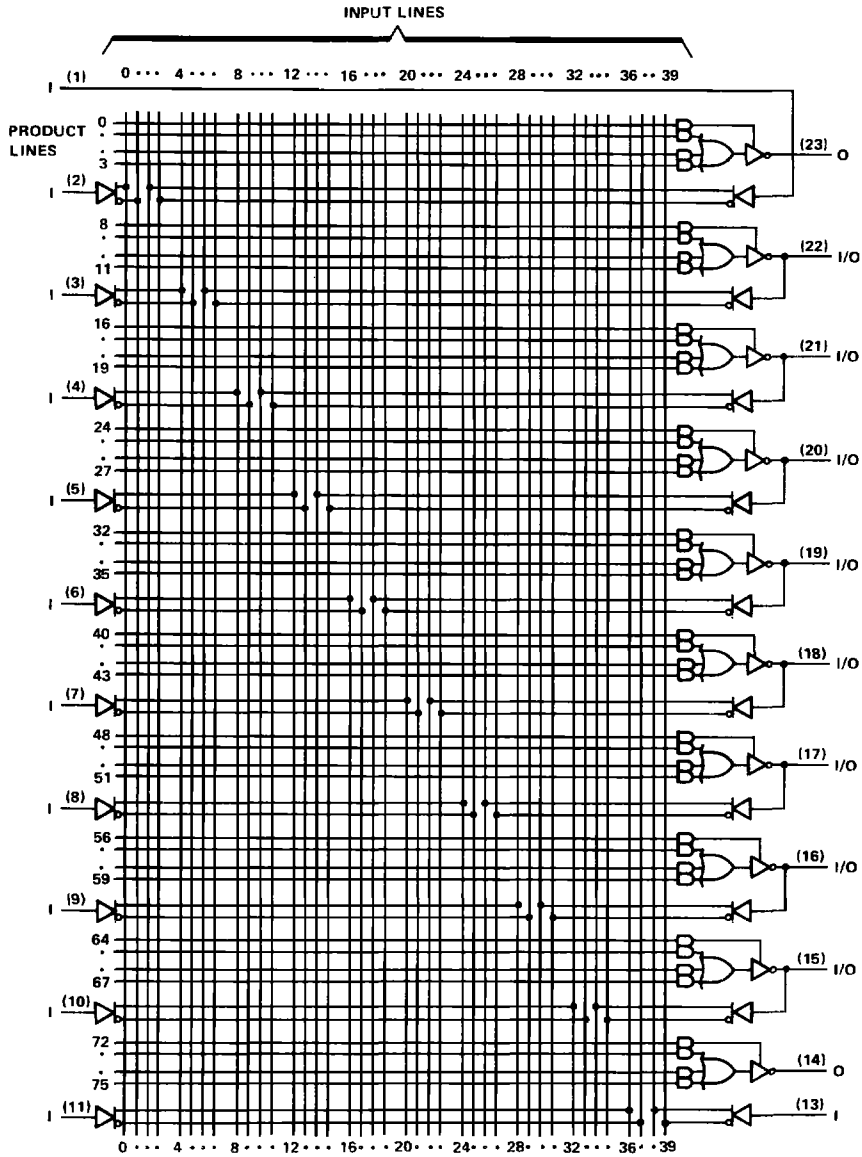
**2**  
Data Sheets



~ denotes fused inputs

**TIBPAL20L10-30C**  
**HIGH-PERFORMANCE EXCLUSIVE-OR IMPACT™ PAL® CIRCUITS**

logic diagram (positive logic)

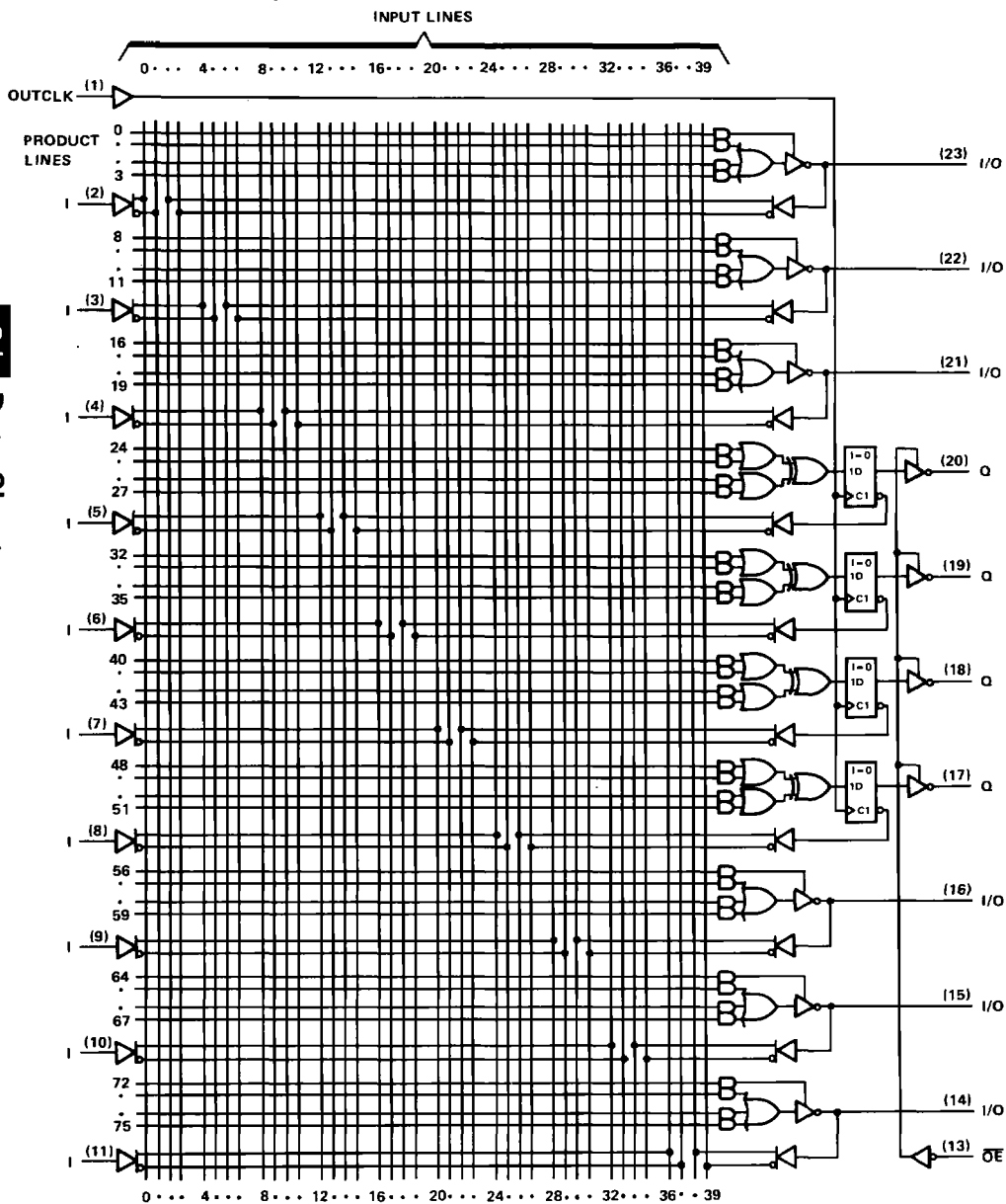


Pin numbers shown are for JT and NT packages.

**2**  
Data Sheets

**TIBPAL20X4-30C**  
**HIGH-PERFORMANCE EXCLUSIVE-OR IMPACT™ PAL® CIRCUITS**

logic diagram (positive logic)

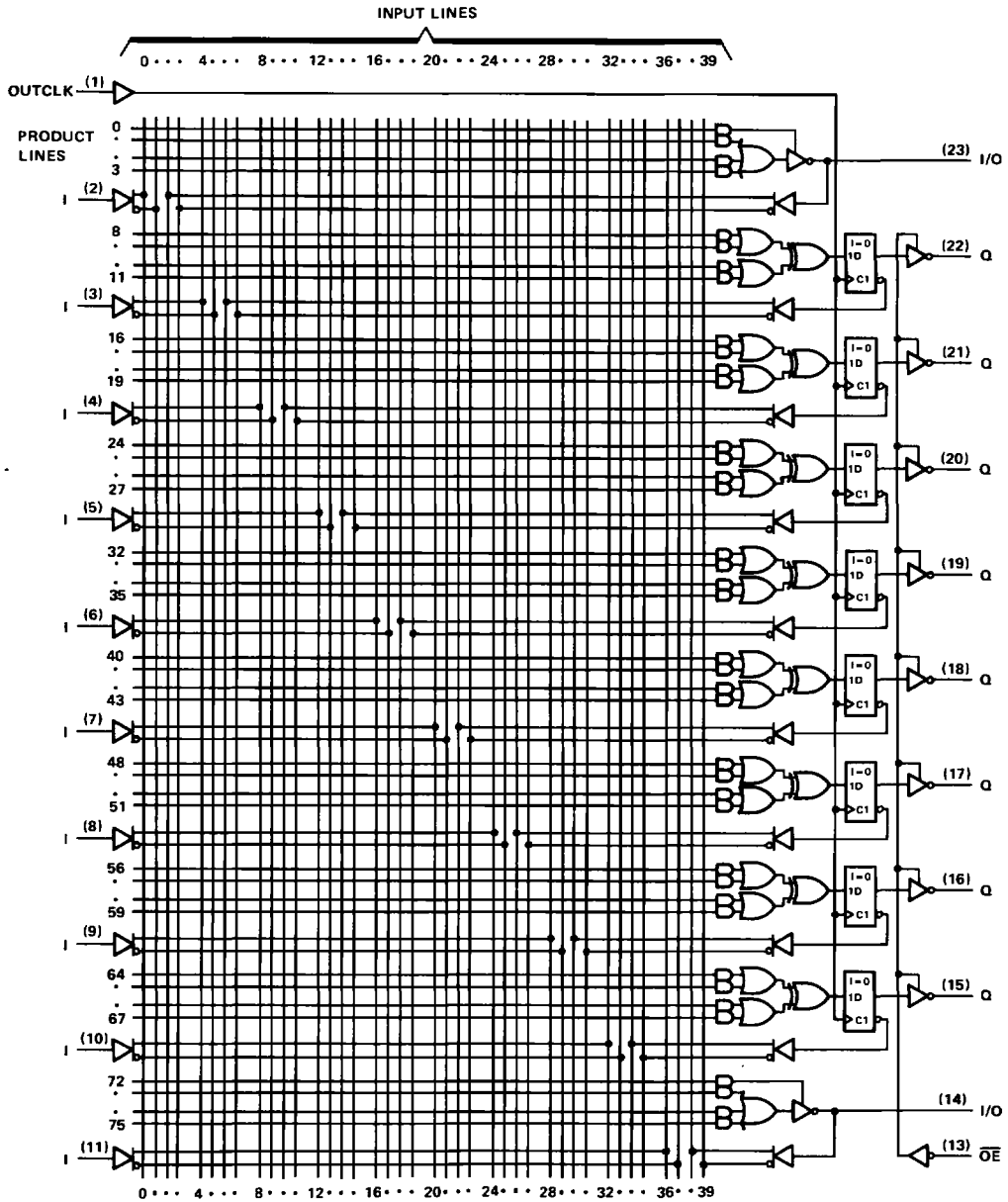


Pin numbers shown are for JT and NT packages.

**2**  
**Data Sheets**

**TIBPAL20X8-30C**  
**HIGH-PERFORMANCE EXCLUSIVE-OR IMPACT™ PAL® CIRCUITS**

logic diagram (positive logic)



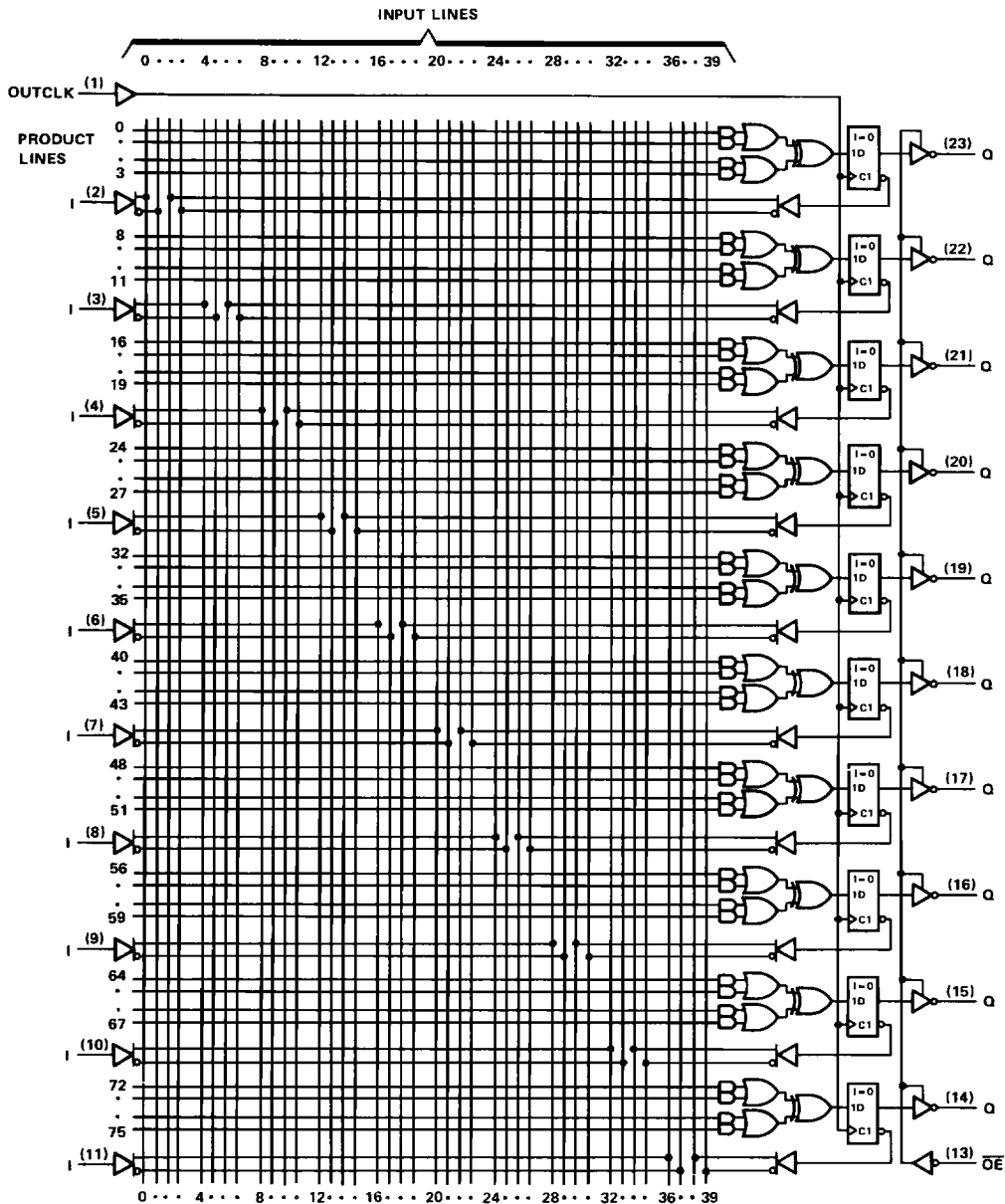
Pin numbers shown are for JT and NT packages.

**2**  
Data Sheets



**TIBPAL20X10-30C**  
**HIGH-PERFORMANCE EXCLUSIVE-OR *IMPACT™* PAL® CIRCUITS**

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

**2**  
**Data Sheets**

# TIBPAL20L10-30C, TIBPAL20X4-30C, TIBPAL20X8-30C, TIBPAL20X10-30C HIGH-PERFORMANCE EXCLUSIVE-OR *IMPACT™* PAL® CIRCUITS

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . .	7 V
Input voltage (see Note 1) . . . . .	5.5 V
Voltage applied to a disabled output (see Note 1) . . . . .	5.5 V
Operating free-air temperature range: C suffix . . . . .	0°C to 75°C
Storage temperature range . . . . .	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

## recommended operating conditions

PARAMETER		–30C			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2		5.5	V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			–3.2	mA
$I_{OL}$	Low-level output current			24	mA
$f_{clock}$	Clock frequency	0		22.2	MHz
$t_w$	Pulse duration, clock, see Note 2	High		15	ns
		Low		25	
$t_{su}$	Setup time, input or feedback before OUTCLK†	30			ns
$t_h$	Hold time, input or feedback after OUTCLK†	0			ns
$T_A$	Operating free-air temperature	0		75	°C

NOTE 2: The high and low clock pulse durations cannot both be at the minimum values specified. Their sum must be equal to or greater than the minimum clock period, which is the reciprocal of the maximum recommended clock frequency.

## electrical characteristics over recommended free-air operating temperature range

PARAMETER	TEST CONDITIONS†	–30C			UNIT
		MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			–1.2	V
$V_{OH}$	$V_{CC} = \text{MIN}, I_{OH} = \text{MAX}$	2.4	3.3		V
$V_{OL}$	$V_{CC} = \text{MIN}, I_{OL} = \text{MAX}$		0.35	0.5	V
$I_{OZH}$	Outputs			20	$\mu\text{A}$
	I/O ports	$V_{CC} = \text{MAX}, V_O = 2.7 \text{ V}$		100	
$I_{OZL}$	Outputs			–20	$\mu\text{A}$
	I/O ports	$V_{CC} = \text{MAX}, V_O = 0.4 \text{ V}$		–250	
$I_I$	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			0.1	mA
$I_{IH}$	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			–0.25	mA
$I_{OS}^{\S}$	$V_{CC} = 5 \text{ V}, V_O = 0$	–30		–130	mA
$I_{CC}$	'20X4, '20X8, '20X10			120	mA
	'20L10	$V_{CC} = \text{MAX}, V_I = 0$		180	
				120	165

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

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Data Sheets

# TIBPAL20L10-30C, TIBPAL20X4-30C, TIBPAL20X8-30C, TIBPAL20X10-30C HIGH-PERFORMANCE EXCLUSIVE-OR *IMPACT™* PAL® CIRCUITS

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	-30C			UNIT
				MIN	TYP†	MAX	
f <sub>max</sub> ‡	With Feedback		R1 = 200 Ω, R2 = 390 Ω, C <sub>L</sub> = 50 pF	22.2			MHz
t <sub>pd</sub>	I, I/O	O, I/O		23	30		ns
t <sub>pd</sub>	OUTCLK†	Q		10	15		ns
t <sub>en</sub>	$\overline{OE}$	Q		11	20		ns
t <sub>dis</sub>	$\overline{OE}$ †	Q		10	20		ns
t <sub>en</sub>	I, I/O	O, I/O		19	30		ns
t <sub>dis</sub>	I, I/O	O, I/O		15	30		ns

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 °C.

$$‡ f_{\max} \text{ (with feedback)} = \frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}, f_{\max} \text{ without feedback can be calculated as } f_{\max} \text{ (without feedback)} = \frac{1}{t_{whigh} + t_{wlow}}$$

2

Data Sheets

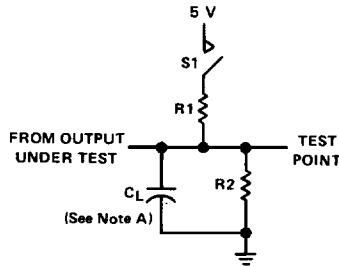
## programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

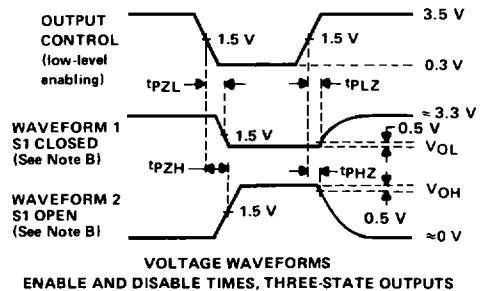
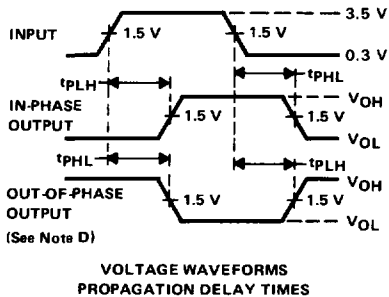
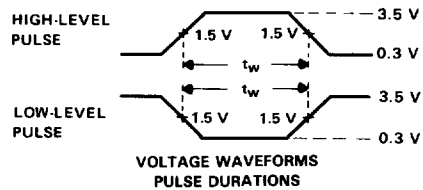
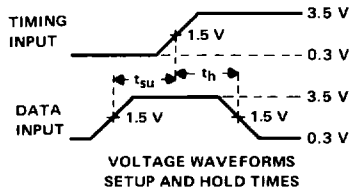
Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

**TIBPAL20L10-30C, TIBPAL20X4-30C, TIBPAL20X8-30C, TIBPAL20X10-30C  
HIGH-PERFORMANCE EXCLUSIVE-OR *IMPACT™* PAL® CIRCUITS**

**PARAMETER MEASUREMENT INFORMATION**



**LOAD CIRCUIT FOR  
THREE-STATE OUTPUTS**



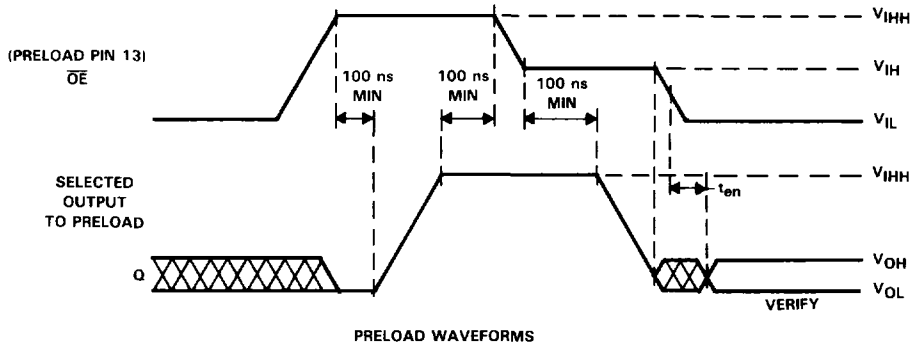
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

**TIBPAL20L10-30C, TIBPAL20X4-30C, TIBPAL20X8-30C, TIBPAL20X10-30C  
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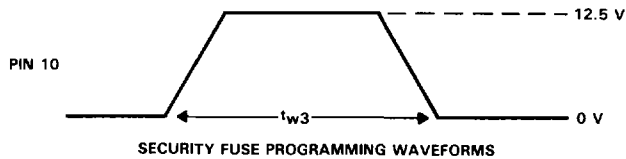
**preload procedures**

**preload procedure for registered outputs**

- Step 1 With  $V_{CC}$  at 5 volts, raise Pin 13 ( $\overline{OE}$ ) to  $V_{IH}$  to disable the outputs and clear the registers (output goes low). Since the outputs are low, only high levels need be preloaded.
- Step 2 Raise the selected output to be preloaded high to  $V_{IH}$ .
- Step 3 Lower Pin 13 to  $V_{IH}$ .
- Step 4 Remove the voltages applied to the outputs. (At least a 100-ns wait is required between step 3 and step 4)
- Step 5 Lower Pin 13 to  $V_{IL}$  to verify preload.



**security fuse programming**



NOTE: Pin numbers shown apply only for the DIP package. If a chip carrier socket adaptor is not used, pin numbers must be changed accordingly.