8-Mbit (512K Words × 16-Bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed
  - t_{AA} = 10 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Low active and standby currents
  - I_{CC} = 90-mA typical at 100 MHz
  - I_{SB2} = 20-mA typical
- Operating voltage range: 2.2 V to 3.6 V.
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Available in Pb-free 44-pin TSOP II and Pb-free 48-ball FBGA packages

Functional Description

CY7C1051H is a high-performance CMOS fast static RAM device with embedded ECC[1].

To access device, assert the chip enable ($\overline{CE}$) input LOW. To perform data writes, assert the Write Enable ($\overline{WE}$) input LOW, and provide the data and address on the device data pins (I/O_0 through I/O_{15}) and address pins (A_0 through A_{18}) respectively. The Byte High Enable ($\overline{BHE}$) and Byte Low Enable ($\overline{BLE}$) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. $\overline{BHE}$ controls I/O_8 through I/O_{15} and $\overline{BLE}$ controls I/O_0 through I/O_7.

To perform data reads, assert the Output Enable ($\overline{OE}$) input and provide the required address on the address lines. Read data is accessible on I/O lines (I/O_0 through I/O_{15}). You can perform byte accesses by asserting the required byte enable signal ($\overline{BHE}$ or $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), or control signals are de-asserted ($\overline{OE}$, $\overline{BLE}$, $\overline{BHE}$).

See the Truth Table on page 13 for a complete description of read and write modes.

The logic block diagrams are provided on page 2.

The CY7C1051H is available in 44-pin TSOP II package.

For a complete list of related documentation, click here.

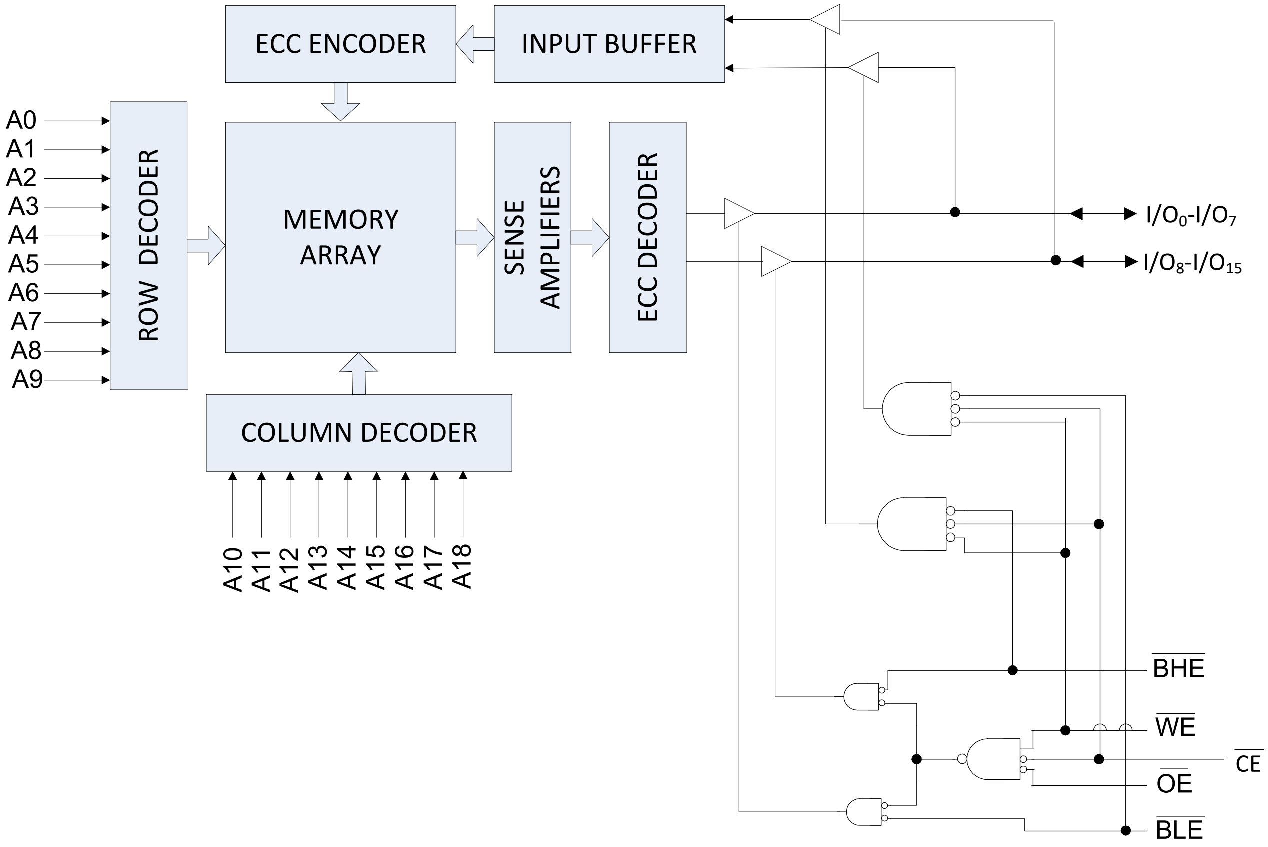
Product Portfolio

Product	Features and Options (see Pin Configurations on page 4)	Range	V_{CC} Range (V)	Speed (ns)	Current Consumption			
					Operating I_{CC}, (mA)		Standby, I_{SB2} (mA)	
					f = f_{max}			
					Typ[2]	Max	Typ[2]	Max
CY7C1051H30	Single chip enables	Industrial	2.2 V–3.6 V	10	90	110	20	30

Notes

1. This device does not support automatic write-back on error detection.
2. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V) T_A = 25 °C.

Logic Block Diagram – CY7C1051H



Contents

Pin Configurations

Figure 1. 44-pin TSOP II pinout

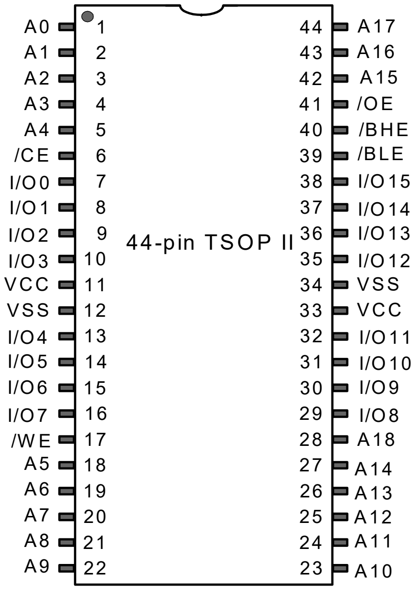
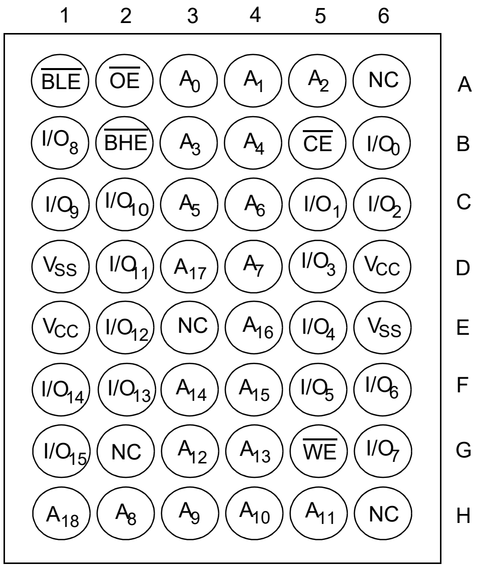


Figure 2. 48-ball FBGA pinout (Top View)



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature
with power applied .... –55 °C to +125 °C

Supply voltage
on V_{CC} relative to GND .... –0.5 V to V_{CC} + 0.5 V

DC voltage applied to outputs
in High Z State[3] .... –0.5 V to V_{CC} + 0.5 V

DC input voltage[3] .... –0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) .... > 2001 V

Latch-up current .... > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description		Test Conditions	10 ns			Unit
				Min	Typ [4]	Max	
V_{OH}	Output HIGH voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –1.0 mA	2.0	–	–	V
		2.7 V to 3.0 V	V_{CC} = Min, I_{OH} = –4.0 mA	2.2	–	–	
		3.0 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	–	
V_{OL}	Output LOW voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA	–	–	0.4	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA	–	–	0.4	
V_{IH}[3]	Input HIGH voltage	2.2 V to 2.7 V		2.0	–	V_{CC} + 0.3	V
		2.7 V to 3.6 V		2.0	–	V_{CC} + 0.3	
V_{IL}[3]	Input LOW voltage	2.2 V to 2.7 V		–0.3	–	0.6	V
		2.7 V to 3.6 V		–0.3	–	0.8	
I_{IX}	Input leakage current		GND $\leq V_{IN} \leq V_{CC}$	–1.0	–	+1.0	µA
I_{OZ}	Output leakage current		GND $\leq V_{OUT} \leq V_{CC}$, Output disabled	–1.0	–	+1.0	µA
I_{CC}	Operating supply current		V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels f = 100 MHz	–	90.0	110.0	mA
I_{SB1}	Automatic CE power down current – TTL inputs		Max V_{CC}, $\overline{CE} \geq V_{IH}$ [4], $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	–	–	40.0	mA
I_{SB2}	Automatic CE power down current – CMOS inputs		Max V_{CC}, $\overline{CE} \geq V_{CC}$ – 0.2 V[5], $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0	–	20.0	30.0	mA

Notes

3. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
4. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.
5. This parameter is guaranteed by design and is not tested.

Capacitance

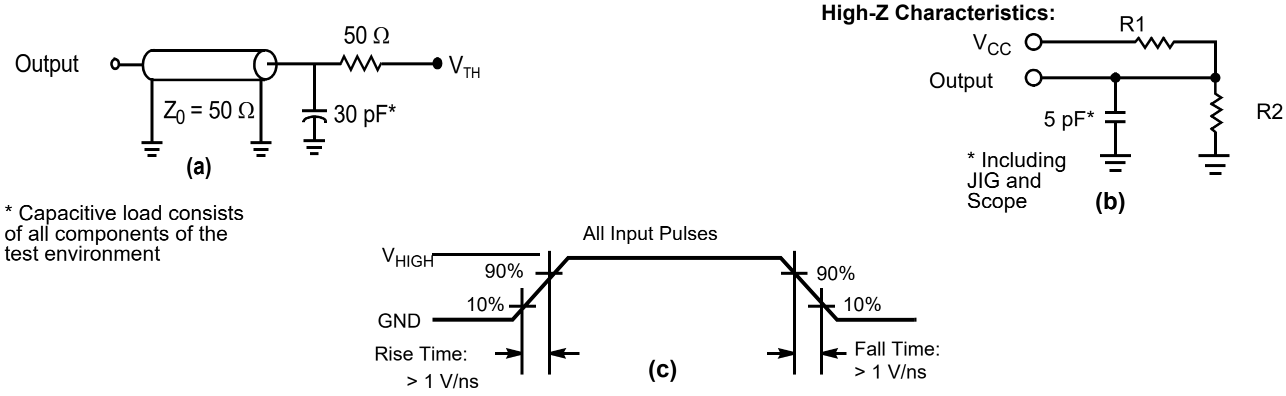
Parameter [6]	Description	Test Conditions	44-pin TSOP II	48-ball VFBGA	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	10	pF
C_{OUT}	I/O capacitance		10	10	pF

Thermal Resistance

Parameter [6]	Description	Test Conditions	44-pin TSOP II	48-ball VFBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	66.93	31.50	°C/W
Θ_{JC}	Thermal resistance (junction to case)		13.09	15.75	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [7]



* Capacitive load consists of all components of the test environment

Parameters	3.0 V	Unit
R1	317	Ω
R2	351	Ω
V_{TH}	1.5	V
V_{HIGH}	3	V

Notes

6. Tested initially and after any design or process changes that may affect these parameters.
7. Full-device AC operation assumes a 100-µs ramp time from 0 to $V_{CC(min)}$ and 100-µs wait time after V_{CC} stabilizes to its operational value.

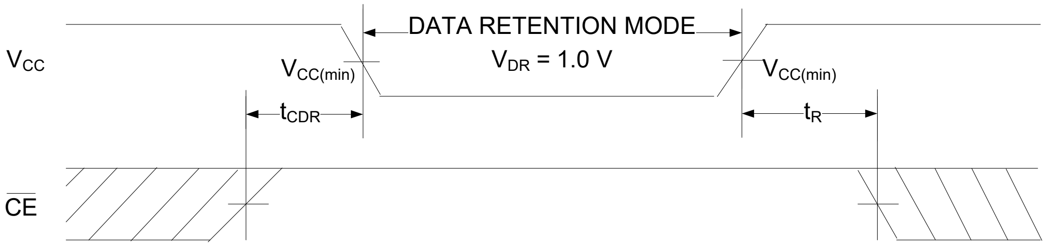
Data Retention Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	1.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V[8], $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	30.0	mA
t_{CDR}[8]	Chip deselect to data retention time	–	0	–	ns
t_R[8, 9]	Operation recovery time	$V_{CC} \geq 2.2$ V	10.0	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

8. This parameter is guaranteed by design and is not tested.
9. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

AC Switching Characteristics

Over the operating range of –40 °C to 85 °C

Parameter [10]	Description	10 ns		Unit
		Min	Max	
Read Cycle				
t_{POWER}	V_{CC} (stable) to the first access [11, 12]	100.0	–	µs
t_{RC}	Read cycle time	10.0	–	ns
t_{AA}	Address to data valid	–	10.0	ns
t_{OHA}	Data hold from address change	3.0	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	10.0	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5.0	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [13, 14, 15]	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [13, 14, 15]	–	5.0	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z 13, 14, 15]	3.0	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [13, 14, 15]	–	5.0	ns
t_{PU}	$\overline{CE}$ LOW to power-up [12]	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down [12]	–	10.0	ns
t_{DBE}	Byte enable to data valid	–	5.0	ns
t_{LZBE}	Byte enable to low Z [13, 14]	0	–	ns
t_{HZBE}	Byte disable to high Z [13, 14]	–	6.0	ns
Write Cycle [16, 17]				
t_{WC}	Write cycle time	10.0	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	7.0	–	ns
t_{AW}	Address setup to write end	7.0	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7.0	–	ns
t_{SD}	Data setup to write end	5.0	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [13, 14, 15]	3.0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [13, 14, 15]	–	5.0	ns
t_{BW}	Byte Enable to write end	7.0	–	ns

Notes

[10] Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$V). Test conditions for the read cycle use the output loading, shown in part (a) of Figure 3 on page 6, unless specified otherwise.

[11] t_{POWER} gives the minimum amount of time that the power supply is at stable V_{CC} until the first memory access is performed.

[12] These parameters are guaranteed by design and are not tested.

[13] t_{HZOE}, t_{HZCE}, t_{HZWE}, and t_{HZBE} are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 3 on page 6. Hi-Z, Lo-Z transition is measured ±200 mV from steady state voltage.

[14] At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.

[15] Tested initially and after any design or process changes that may affect these parameters.

[16] The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

[17] The minimum write pulse width for Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms

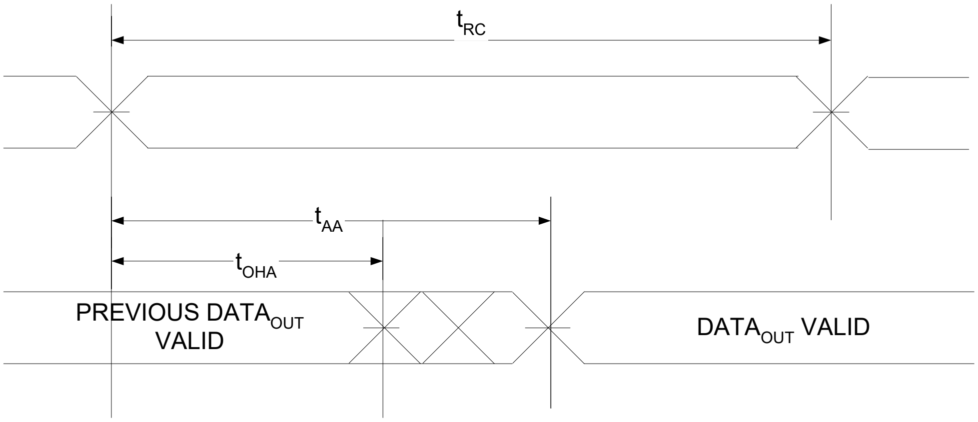


Figure 5. Read Cycle No. 1 of CY7C1051H (Address Transition Controlled) [18, 19]

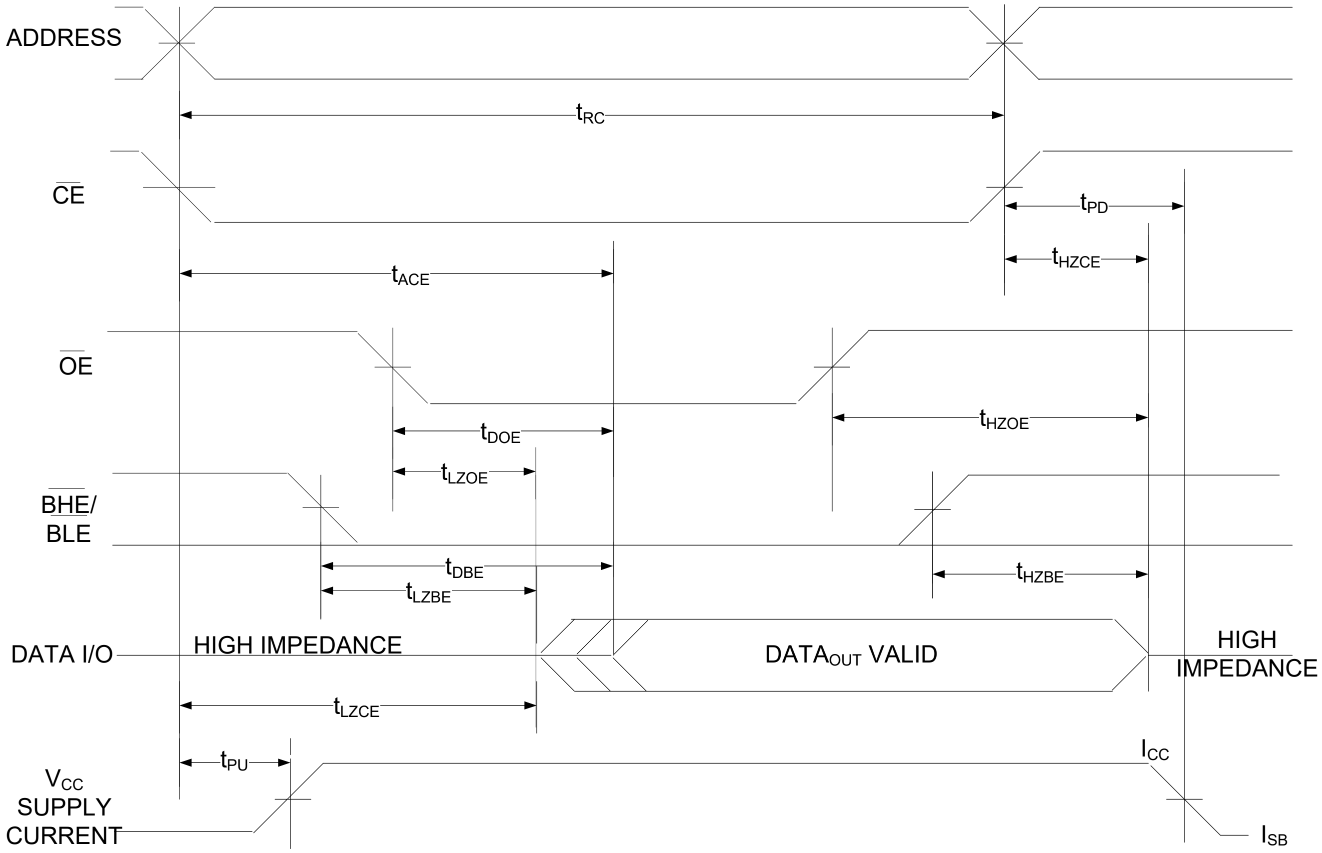


Figure 6. Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled) [19, 20]

Notes

[18] The device is continuously selected, $\overline{\text{OE}} = V_{IL}$, $\overline{\text{CE}} = V_{IL}$, $\overline{\text{BHE}}$ or $\overline{\text{BLE}}$ or both = V_{IL}.

[19] $\overline{\text{WE}}$ is HIGH for read cycle.

[20] Address valid prior to or coincident with $\overline{\text{CE}}$ LOW transition.

Switching Waveforms (continued)

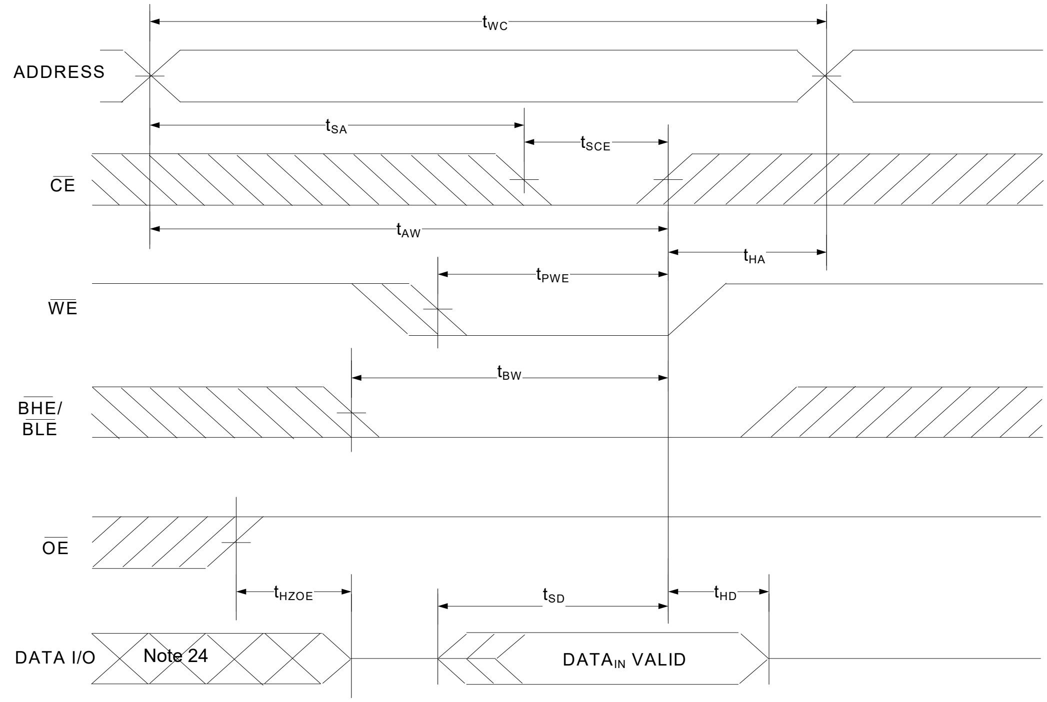


Figure 7. Write Cycle No. 1 ($\overline{CE}$ Controlled) [21, 22]

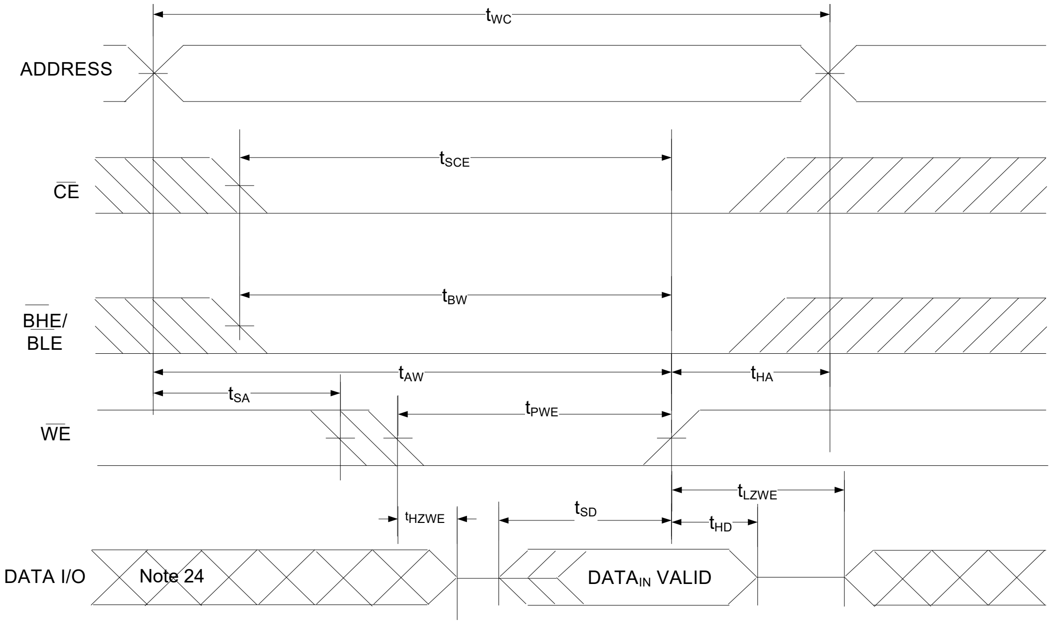


Figure 8. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [21, 22, 23]

Notes

[21] The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$ and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

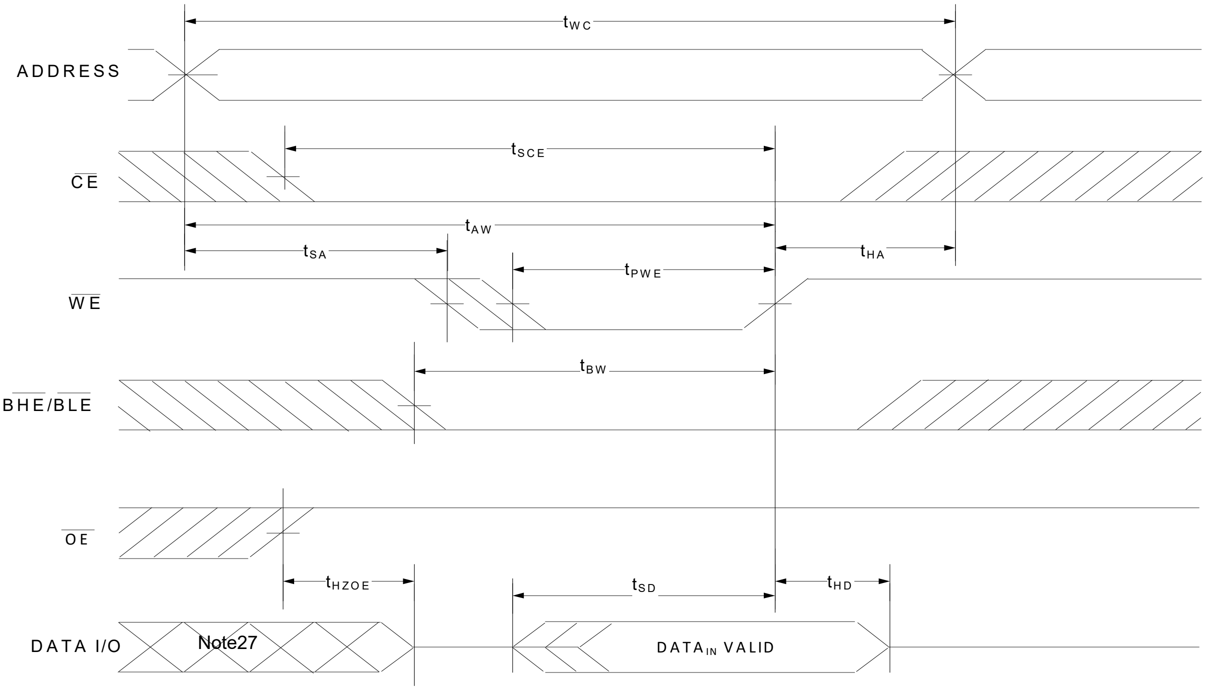
[22] Data I/O is in high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.

[23] The minimum write cycle pulse width should be equal to sum of t_{HZWE} and t_{SD}.

[24] During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{WE}$ controlled) [25, 26]



Notes

25. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$ and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
26. Data I/O is in high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
27. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

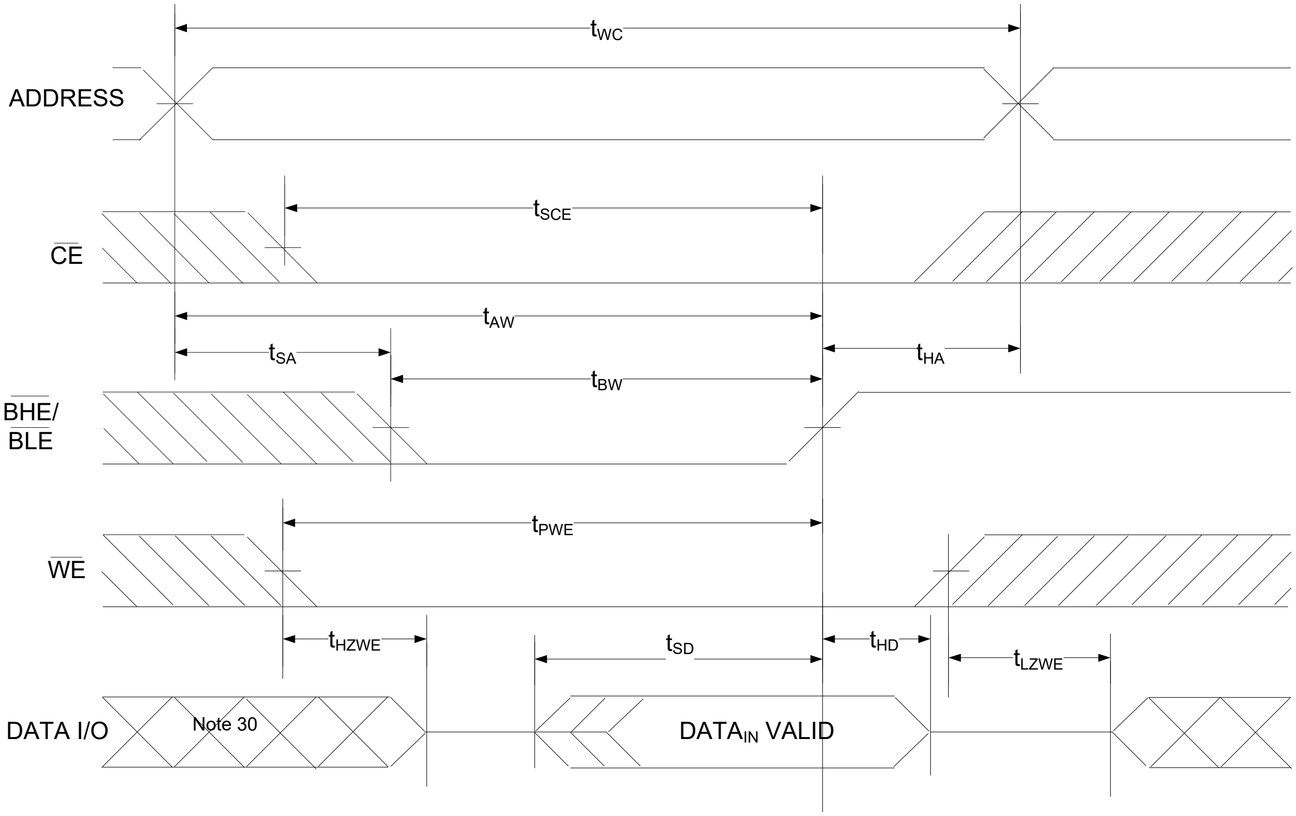


Figure 10. Write Cycle No. 4 ($\overline{BLE}$ or $\overline{BHE}$ Controlled) [28, 29]

Notes

[28] The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

[29] Data I/O is in high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$, or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.

[30] During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O$_0$–I/O$_7$	I/O$_8$–I/O$_{15}$	Mode	Power
H	X[31]	X[31]	X[31]	X[31]	High-Z	High-Z	Power down	Standby (I_{SB})
L	L	H	L	L	Data out	Data out	Read all bits	Active (I_{CC})
L	L	H	L	H	Data out	High-Z	Read lower bits only	Active (I_{CC})
L	L	H	H	L	High-Z	Data out	Read upper bits only	Active (I_{CC})
L	X	L	L	L	Data in	Data in	Write all bits	Active (I_{CC})
L	X	L	L	H	Data in	High-Z	Write lower bits only	Active (I_{CC})
L	X	L	H	L	High-Z	Data in	Write upper bits only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, outputs disabled	Active (I_{CC})
L	X	X	H	H	High-Z	High-Z	Selected, outputs disabled	Active (I_{CC})

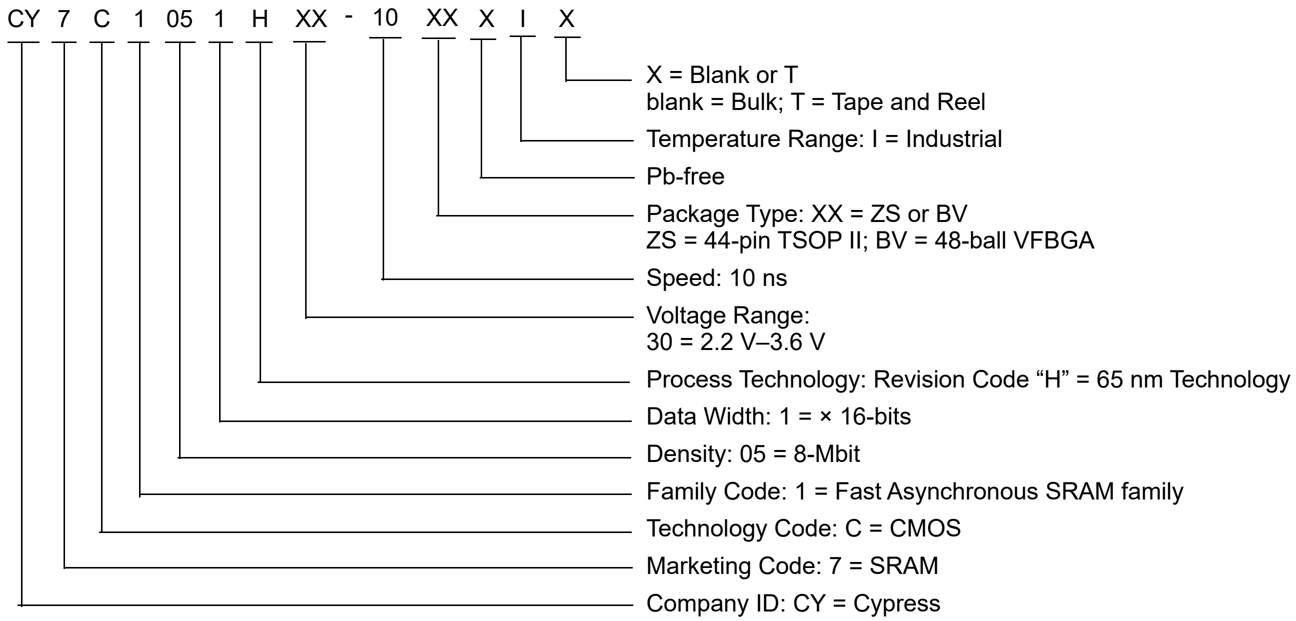
Note

31. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Key Features / Differentiators	Operating Range
10	2.2 V–3.6 V	CY7C1051H30-10ZSXI	51-85087	44-pin TSOP II	Single Chip Enable	Industrial
		CY7C1051H30-10ZSXIT				
		CY7C1051H30-10BVXI	51-85150	48-ball VFBGA		

Ordering Code Definitions



CY 7 C 1 05 1 H XX - 10 XX X I X

X = Blank or T
blank = Bulk; T = Tape and Reel

Temperature Range: I = Industrial

Pb-free

Package Type: XX = ZS or BV
ZS = 44-pin TSOP II; BV = 48-ball VFBGA

Speed: 10 ns

Voltage Range:
30 = 2.2 V–3.6 V

Process Technology: Revision Code “H” = 65 nm Technology

Data Width: 1 = × 16-bits

Density: 05 = 8-Mbit

Family Code: 1 = Fast Asynchronous SRAM family

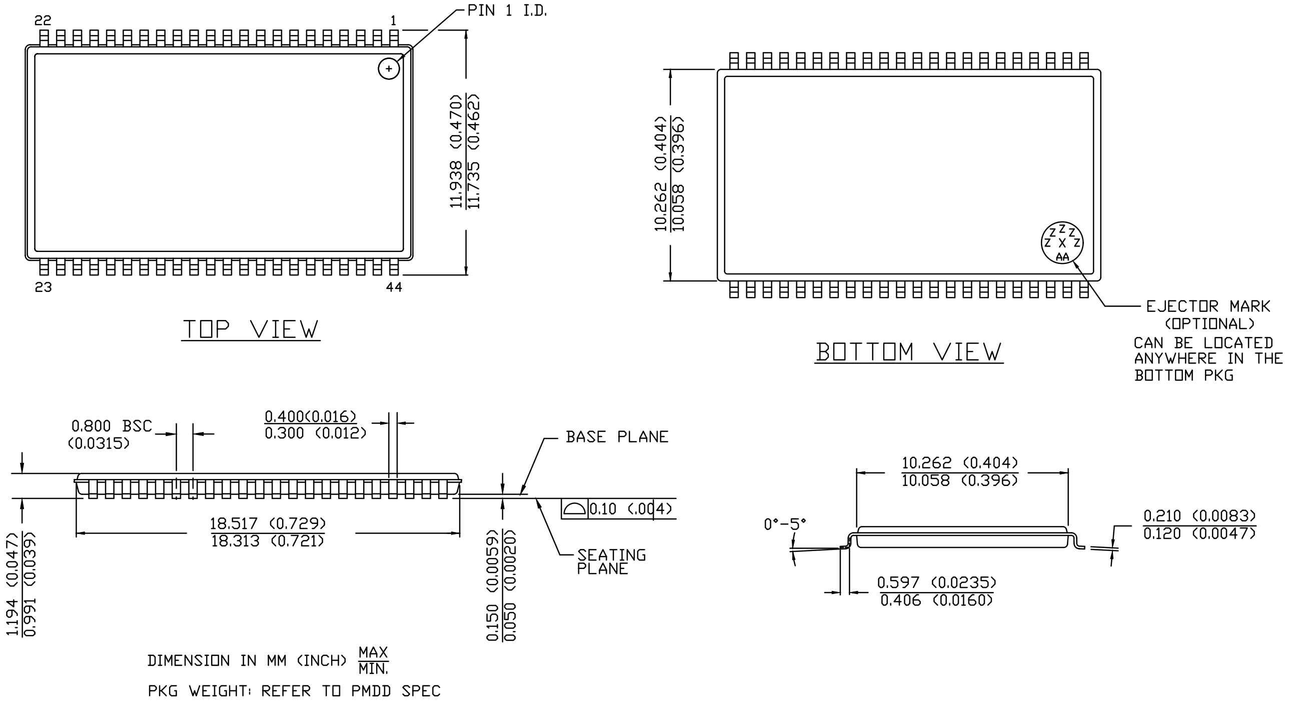
Technology Code: C = CMOS

Marketing Code: 7 = SRAM

Company ID: CY = Cypress

Package Diagram

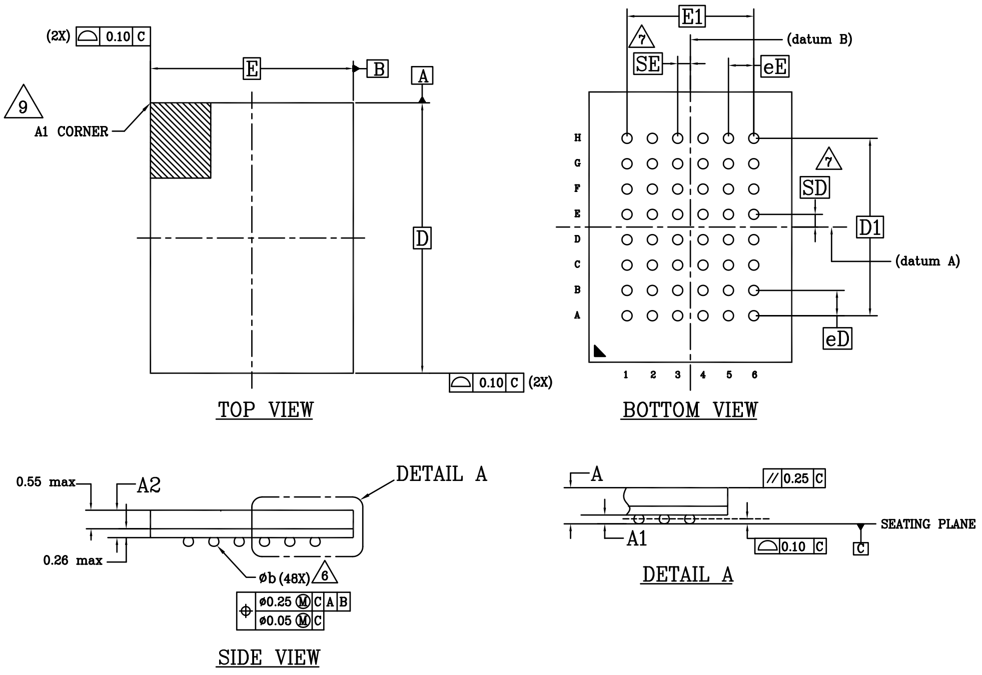
Figure 11. 44-pin TSOP II (18.4 × 10.2 × 1.194 mm) Package Outline, 51-85087



51-85087 *F

Package Diagram (continued)

Figure 12. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
A2	-	-	0.81
D	8.00 BSC		
E	6.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
MD	8		
ME	6		
n	48		
Ø b	0.25	0.30	0.35
eE	0.75 BSC		
eD	0.75 BSC		
SD	0.375 BSC		
SE	0.375 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *I

Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1051H, 8-Mbit (512K Words × 16-Bit) Static RAM with Error-Correcting Code (ECC) Document Number: 002-03314			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	4943606	10/09/2015	New data sheet.
*A	5258628	05/27/2016	Changed status from Preliminary to Final. Updated to new template.
*B	5435280	09/13/2016	Updated Maximum Ratings: Updated Note 3 (Replaced “2 ns” with “20 ns”). Updated DC Electrical Characteristics: Removed Operating Range “2.7 V to 3.6 V” and all values corresponding to V_{OH} parameter. Included Operating Ranges “2.7 V to 3.0 V” and “3.0 V to 3.6 V” and all values corresponding to V_{OH} parameter. Updated Ordering Information: Updated part numbers. Updated Ordering Code Definitions. Updated to new template. Completing Sunset Review.
*C	5975928	11/27/2017	Updated Cypress Logo and Copyright.
*D	7023423	11/13/2020	Added 48-ball VFBGA package related information in all instances across the document. Updated Ordering Information: Updated part numbers. Updated Package Diagram: spec 51-85087 – Changed revision from *E to *F. Added spec 51-85150 *I. Updated to new template. Completing Sunset Review.

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