NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE (YYMMDD)	Form Approved OMB No. 0704-0188
98-08-06	

2. PROCURING ACTIVITY NO.	
3. DODAAC	

4. ORIGINATOR	b. ADDRESS *(Street, City, State, Zip Code)*	5. CAGE CODE	6. NOR NO.
a. TYPED NAME *(First, Middle Initial, Last)*	Defense Supply Center Columbus 3990 East Broad Street Columbus, OH 43216-5000	7. CAGE CODE 67268	8. DOCUMENT NO. **5962-90869**
		67268	

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 64K x 8 ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY (EEPROM) , MONOLITHIC SILICON	a. CURRENT A	b. NEW B	Verbal coordination record on file.

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "B".
Revisions description column; add "Changes in accordance with NOR 5962-R160-98".
Revisions date column; add "98-08-06".
Revision level block; add "B".
Rev status of sheets; for sheets 12 and 33, add "B".

Sheet 12: Footnote 5/, under "Timing measurement reference levels:", for Inputs delete 1 V and 2 V and replace with 1.5 V; for Outputs delete 0.8 V and 2.0 V and replace with 1.5 V.

Revision level block; add "B".

Sheet 33: Add note beneath Table III to read: "For V_{OH} and V_{OL}, the logic output compare levels shall be 1.5 V for subgroups 9, 10, and 11 only."

Revision level block; add "B".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME *(First, Middle Initial, Last)*
DSCC-VAS	

d. TITLE	e. SIGNATURE	f. DATE SIGNED (YYMMDD)
Chief, Microelectronics Team	Raymond Monnin	98-08-06

15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED *(Signature)*	c. DATE SIGNED (YYMMDD)
DSCC-VAS	Gary L. Gross	98-08-06

NOTICE OF REVISION (NOR)

(See MIL-STD-480 for instructions)
This revision described below has been authorized for the document listed.

DATE (YYMMDD)	Form Approved OMB No. 0704-0188
92-01-22	

1. ORIGINATOR NAME AND ADDRESS	2. CAGE CODE	3. NOR NO.
Defense Electronics Supply Center Dayton, Ohio 45444-5277	67268	5962-R114-92
	4. CAGE CODE	**5. DOCUMENT NO.**
	67268	5962-90869

6. TITLE OF DOCUMENT	7. REVISION LETTER	
Microcircuit, Memory, Digital, CMOS, 64K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM), Monolithic Silicon	(Current) Basic	(New) A
	8. ECP NO.	
	No registered users.	

9. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES

All

10. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "A"
Revisions description column; add "Changes in accordance with NOR 5962-R114-92".
Revisions date column; add "92-01-22".

Sheet 8: Table IA, $\overline{OE}$ high voltage (V_H), Limits (Min) column delete "12" and substitute "15" and Limits (Max) column delete "13" and substitute "16".

Sheet 32: Table IIA, Electrical test requirements footnote 5/, delete "4.4.1e" and substitute "4.4.1d".

11. THIS SECTION FOR GOVERNMENT USE ONLY

a. CHECK ONE

[X] EXISTING DOCUMENT SUPPLEMENTED BY THIS NOR MAY BE USED IN MANUFACTURE.

[ ] REVISED DOCUMENT MUST BE RECEIVED BEFORE MANUFACTURER MAY INCORPORATE THIS CHANGE.

[ ] CUSTODIAN OF MASTER DOCUMENT SHALL MAKE ABOVE REVISION AND FURNISH REVISED DOCUMENT TO:

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	SIGNATURE AND TITLE	DATE (YYMMDD)
DESC-ECS	Michael A. Frye BRANCH CHIEF	92-01-22
12. ACTIVITY ACCOMPLISHING REVISION DESC-ECS	REVISION COMPLETED (Signature) Gary L. Gross	DATE (YYMMDD) 92-01-22

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET	35	36	37	38	39	40													
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
91-10-18

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS
64K x 8 ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY (EEPROM), MONOLITHIC SILICON

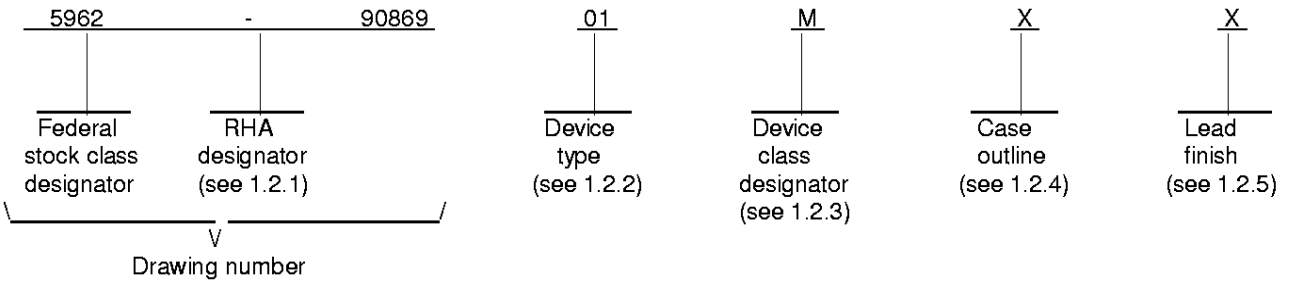
SIZE	CAGE CODE	
A	**67268**	**5962-90869**

SHEET 1 OF 40

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time	Write speed	Write mode	Endurance
01	28C512	64K x 8 EEPROM	250 ns	10 ms	Byte/Page	10,000 cycle
02	"	64K x 8 EEPROM	250 ns	5 ms	Byte/Page	10,000 cycle
03	"	64K x 8 EEPROM	200 ns	10 ms	Byte/Page	10,000 cycle
04	"	64K x 8 EEPROM	200 ns	5 ms	Byte/Page	10,000 cycle
05	"	64K x 8 EEPROM	150 ns	10 ms	Byte/Page	10,000 cycle
06	"	64K x 8 EEPROM	150 ns	5 ms	Byte/Page	10,000 cycle
07	"	64K x 8 EEPROM	120 ns	10 ms	Byte/Page	10,000 cycle
08	"	64K x 8 EEPROM	120 ns	5 ms	Byte/Page	10,000 cycle
09	28C513	64K x 8 EEPROM	250 ns	10 ms	Byte/Page	10,000 cycle
10	"	64K x 8 EEPROM	250 ns	5 ms	Byte/Page	10,000 cycle
11	"	64K x 8 EEPROM	200 ns	10 ms	Byte/Page	10,000 cycle
12	"	64K x 8 EEPROM	200 ns	5 ms	Byte/Page	10,000 cycle
13	"	64K x 8 EEPROM	150 ns	10 ms	Byte/Page	10,000 cycle
14	"	64K x 8 EEPROM	150 ns	5 ms	Byte/Page	10,000 cycle
15	"	64K x 8 EEPROM	120 ns	10 ms	Byte/Page	10,000 cycle
16	"	64K x 8 EEPROM	120 ns	5 ms	Byte/Page	10,000 cycle

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Case outline
X	See figure 1(32-lead, 1.685" x .600" x .225", dual in-line package
Y	C-12 (32-terminal, .560" x .458" x .120"), rectangular chip carrier package
Z	See figure 1(32-lead, .830" x .416" x .120"), flat package
U	See figure 1 (36-lead, .760" x .760" x .120"), pin grid array

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V dc to +6.0 V dc 3/
Operating case temperature range	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	28°C/W 4/
Case Y	See MIL-M-38510, appendix C
Case Z	22°C/W 4/
Case U	20°C/W 4/
Maximum power dissipation (P_D)	1.0 watts
Junction temperature (T_J)	+175°C 5/
Endurance	10,000 cycles/byte (minimum)
Data retention	10 years minimum

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Supply voltage (V_{SS})	0.0 V dc
High level input voltage range (V_{IH})	2.0 V dc to V_{CC} + 1.0 V dc
Low level input voltage range (V_{IL})	-0.1 V dc to 0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	6/ percent

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltages referenced to V_{SS} (V_{SS} = ground), unless otherwise specified.
3/ Negative undershoots to a minimum of -1.0 V are allowed with a maximum of 20 ns pulse width.
4/ When the thermal resistance for this case is specified in MIL-STD-1835, that value shall supersede the value indicated herein.
5/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
6/ When a QML source exists, a value shall be provided.

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. This is a fully characterized military detail specification and is suitable for qualification of device classes B and S to the requirements of MIL-M-38510. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified in 4.4.5e.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECS of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 42 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

3.12 Processing of EEPROMs: All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.12.1 Conditions of the supplied devices: Devices will be supplied in cleared state (logic "1's"). No provision will be made for supplying written devices.

3.12.2 Clearing of EEPROMs: When specified, devices shall be cleared in accordance with the procedures and characteristics specified in 4.6.4.

3.12.3 Writing of EEPROMs: When specified, devices shall be written in accordance with the procedures and characteristics specified in 4.6.3.

3.12.4 Verification of state of EEPROMs: When specified, devices shall be verified as either written to the specified pattern or cleared. As a minimum, verification shall consist of performing a read of the entire array to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and the device shall be removed from the lot or sample.

3.12.5 Power supply sequence of EEPROMs: In order to reduce the probability of inadvertent writes, the following power supply sequences shall be observed:

a. A logic high state shall be applied to $\overline{WE}$ and/or $\overline{CE}$ at the same time or before the application of V_{CC}.

b. A logic high state shall be applied to $\overline{WE}$ and/or $\overline{CE}$ at the same time or before the removal of V_{CC}.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. Prior to burn in, the devices shall be programmed (see 4.6.3 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). (See figure 4.) The pattern shall be read before and after burn in. Devices having bits not in the proper state after burn in shall constitute a device failure and shall be included in the percent defective allowable (PDA) calculation and shall be removed from the lot (see 4.2.3 herein).

c. For device class M, the burn-in test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S, the burn-in test circuit shall be submitted to the qualifying activity.

(1) Static burn-in for device classes S (method 1015 of MIL-STD-883, test condition A).

(a) All inputs shall be connected to GND. Outputs may be open or connected to 4.5 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to V_{CC} ±0.5 V. R1 = 220Ω to 47 kΩ. For static II burn-in, reverse all input connections (i.e., V_{SS} to V_{CC}).

(b) V_{CC} = 4.5 V minimum.

(c) Ambient temperature (T_A) shall be +125°C minimum.

(d) Test duration for the static test shall be 48 hours minimum. The 48-hour burn-in shall be broken into two sequences of 24 hours each (static I and static II) followed by interim electrical measurements.

(2) Dynamic burn-in for device classes M, B, and S (method 1015 of MIL-STD-883, test condition D or F) using the circuit submitted (see 4.2.1c herein).

d. Interim and final electrical parameters shall be as specified in table IIA herein.

e. For classes S and B devices, post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

f. An endurance test including a data retention bake, as specified in method 1033 of MIL-STD-883, prior to burn-in (e.g., may be performed at wafer sort) shall be included as part of the screening procedure, with the following conditions:

(1) Cycling may be chip, block, byte or page at equipment room ambient and shall cycle all bytes a minimum of 10,000 cycles.

(2) After cycling, perform a high temperature unbiased storage 48 hours at +150°C minimum. The storage time may be accelerated by a higher temperature in accordance with the Arrhenius relationship and with the apparent activation energy of 0.6 eV. The maximum storage temperature shall not exceed +200°C for assembled devices and +300°C for unassembled devices. All devices shall be programmed with a charge opposite the state that the cell would read in its equilibrium state (e.g. worst case pattern, see 3.12.3 herein).

(3) Read the data retention pattern and test using subgroups 1, 7, and 9 (at the manufacturer's option high temperature equivalent subgroups 2, 8A, and 10 or low temperature equivalent subgroups 3, 8B, and 11 may be used in lieu of subgroups 1, 7, and 9) after cycling and bake, but prior to burn-in. Devices having bits not in the proper state after storage shall constitute a device failure.

g. After the completion of all screening, the devices shall be erased and verified prior to delivery.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition, and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V; $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
High level input current	I_{IH}	$V_{CC} = 5.5$ V, $V_{IN} = 5.5$ V	1, 2, 3 (3010)	All	-5	5	µA
Low level input current	I_{IL}	$V_{CC} = 5.5$ V, $V_{IN} = 0.1$ V	1, 2, 3 (3009)	All	-5	5	µA
High impedance output leakage current 1/	I_{OZH}	$V_{CC} = 5.5$ V, $V_O = 5.5$ V $V_{IH} \le \overline{OE} \le V_{CC}$	1, 2, 3 (3021)	All	-10	10	µA
	I_{OZL}	$V_{CC} = 5.5$ V, $V_O = 0.0$ V $V_{IH} \le \overline{OE} \le V_{CC}$	1, 2, 3 (3020)		-10	10	
Output high voltage	V_{OH}	$I_{OH} = -400$ µA, $V_{CC} = 4.5$ V $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V	1, 2, 3 (3006)	All	2.4		V
Output low voltage	V_{OL}	$I_{OL} = 2.1$ mA, $V_{CC} = 4.5$ V $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V	1, 2, 3 (3007)	All		0.4	V
Input high voltage 2/	V_{IH}	$V_{CC} = 5.5$ V	1, 2, 3 (3008)	All	2.0	6.0	V
Input low voltage 2/	V_{IL}	$V_{CC} = 4.5$ V	1, 2, 3 (3008)	All	-0.5	0.8	V
$\overline{OE}$ high voltage	V_H		1, 2, 3	All	12	13	V
Operating supply current	I_{CC1}	$V_{CC} = 5.5$ V, $\overline{WE} = V_{IH}$, $\overline{CE} = \overline{OE} = V_{IL}$ $f = 1/t_{AVAV}$ min	1, 2, 3 (3005)	All		50	mA
Standby supply current TTL	I_{CC2}	$V_{CC} = 5.5$ V, $\overline{CE} = V_{IH}$, all I/O's = open, $\overline{OE} = V_{IL}$, f = 0 Hz	1, 2, 3 (3005)	All		3	mA
Standby supply current CMOS	I_{CC3}	$V_{CC} = 5.5$ V, $\overline{CE} = V_{CC} - 0.3$ V Inputs = V_{IH}, I/O's = open, $\overline{OE} = V_{IL}$, f = 0 Hz	1, 2, 3 (3005)			500	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V; $4.5 \text{ V} \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input capacitance 3/ 4/	C_{IN}	$V_{IN} = 0$ V, f = 1.0 MHz, $T_C = +25°C$, see 4.4.1d	4 (3012)	All		10.0	pF
Output capacitance 3/ 4/	C_{OUT}	$V_{OUT} = 0$ V, f = 1.0 MHz $T_C = +25°C$, see 4.4.1d	4 (3012)	All		10.0	pF
Functional tests		See 4.4.1b	7, 8 (3014)	All			
Read cycle time	t_{AVAV}	See figures 5, 6, and 7 as applicable. 5/	9, 10, 11 (3003)	01-02 09-10	250		ns
				03,04, 11,12	200		
				05,06, 13,14	150		
				07,08, 15,16	120		
Address access time	t_{AVQV}		9, 10, 11 (3003)	01,02, 09,10		250	ns
				03,04, 11,12		200	
				05,06, 13,14		150	
				11,12, 15,16		120	
$\overline{CE}$ access time	t_{ELQV}		9, 10, 11 (3003)	01-02 09,10		250	ns
				03,04, 11,12		200	
				05,06, 13,14		150	
				07,08, 15,16		120	
$\overline{OE}$ access time	t_{OLQV}		9, 10, 11 (3003)	All		50	ns
CE to output in low Z 4/	t_{ELQX}	See figures 5, 6, and 7 as applicable.	9, 10, 11 (3003)	All	0		ns
Chip disable to output in high Z 4/	t_{EHQZ}		9, 10, 11 (3003)	All		50	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V; 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{OE}$ to output in low Z 4/	t_{OLQX}	See figures 5, 6, and 7 as applicable.	9, 10, 11 (3003)	All	0		ns
Output disable to output in high Z 4/	t_{OHQZ}		9, 10, 11 (3003)	All		50	ns
Output hold from address change	t_{AXQX}	See figures 5, 6, and 7 as applicable. 5/	9, 10, 11 (3003)	All	0		ns
Write cycle time	t_{WHWL1} t_{EHEL1}		9, 10, 11 (3003)	01,03 05,07, 09,11, 13,15		10	ns
				02,04, 06,08 10,12, 14,16		5	
Address setup time	t_{AVWL} t_{AVEL}		9, 10, 11 (3003)	All	0		ns
Address hold time	t_{WLAX} t_{ELAX}		9, 10, 11 (3003)	All	50		ns
Write setup time	t_{ELWL} t_{WLEL}		9, 10, 11 (3003)	All	0		ns
Write hold time	t_{WHEH} t_{EHWH}		9, 10, 11 (3003)	All	0		ns
$\overline{OE}$ setup time	t_{OHWL} t_{OHEL}		9, 10, 11 (3003)	All	10		ns
$\overline{OE}$ hold time	t_{WHOL} t_{EHOL}		9, 10, 11 (3003)	All	10		ns
Write pulse width (page or byte write)	t_{WLWH} t_{ELEH}		9, 10, 11 (3003)	All	.100		µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V; 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Data setup time	t_{DVWH} t_{DVEH}	See figures 5, 6, and 7 as applicable. 5/	9, 10, 11 (3003)	All	50		ns
Data hold time	t_{WHDX} t_{EHDX}		9, 10, 11 (3003)	All	10		ns
Byte load cycle	t_{WHWL2}		9, 10, 11 (3003)	All	.20	100	µs
Last byte loaded to data polling	t_{WHEL} t_{EHEL}		9, 10, 11 (3003)	01,02 09,10		250	ns
				03,04, 11,12		200	
				05,06, 13,14		150	
				07,08, 15,16		120	
$\overline{CE}$ setup time	t_{ELWL}		9, 10, 11 (3003)	All	5		µs
$\overline{OE}$ setup time (chip erase)	t_{OVHWL}		9, 10, 11 (3003)	All	5		µs
$\overline{WE}$ pulse width (chip clear)	t_{WLWH2}		9, 10, 11 (3003)	All	10		ms
$\overline{CE}$ hold time (chip erase)	t_{WHEH}		9, 10, 11 (3003)	All	5		µs
$\overline{OE}$ hold time	t_{WHOH}		9, 10, 11 (3003)	All	5		µs
High voltage (chip erase)	V_H		9, 10, 11 (3003)	All	12	13	V
Clear recovery	t_{OLEL}	See figures 5, 6, and 7 as applicable.	9, 10, 11 (3003)	All		50	ms
Data setup time 6/	t_{DHWL}		9, 10, 11 (3003	All	1		µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V; 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Data hold time during chip erase cycle 6/	t_{WHDX}	See figures 5, 6, and 7 as applicable.	9, 10, 11 (3003)	All	1		µs

1/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{OZL} and I_{OZH} with the output under test connected to V_{OUT}. Terminal conditions for the output leakage current test shall be as follows:

a. $V_{IH} = 2.0$ V: $V_{IL} = 0.8$ V.

b. For I_{OZL}: Select an appropriate address to acquire a logic "1" on the designated output. Apply V_{IH} to $\overline{CE}$. Measure the leakage current while applying the specified voltage.

c. For I_{OZH}: Select an appropriate address to acquire a logic "0" on the designated output. Apply V_{IH} to $\overline{CE}$. Measure the leakage current while applying the specified voltage.

2/ A functional test shall verify the dc input and output levels and applicable patterns as appropriate, all input and I/O pins shall be tested. Terminal conditions are as follows:

a. Inputs: H = 2.0 V: L = 0.8 V.

b. Outputs: H = 2.4 V minimum and L = 0.4 V maximum.

c. The functional tests shall be performed with $V_{CC} = 4.5$ and $V_{CC} = 5.5$ V.

3/ All pins not being tested are to be open.

4/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table IA.

5/ Tested by application of specified timing signals and conditions.
Equivalent a.c. test conditions:
Output load: See figure 8.
Input rise and fall times ≤ 10 ns.
Input pulse levels: 0.4 V and 2.4 V.
Timing measurement reference levels:
Inputs: 1 V and 2 V.
Outputs: 0.8 V and 2 V.

6/ This parameter not applicable for internal timer controlled devices.

TABLE IB. Single event phenomena (SEP) test limits. 1/ 2/

Device type	Temperature +125°C (±10°C)	Memory pattern	$V_{CC} = 4.5$ V		Bias for latch-up test $V_{CC} = 5.5$ V (minimum) no latch-up LET = 3/ 4/
			Effective threshhold LET no upsets (Mev/(mg/cm^2)	Maximum device cross section (cm^2)	

1/ This blank table will be filled in when a qualified vendor exists.
2/ For SEP test conditions, see 4.4.5 herein.
3/ Value to be determined.
4/ Worst case temperature T_A = +125°C

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.

c. Static burn-in I and II failures shall be cumulative for determining PDA.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table IA, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

e. The PDA for device classes Q and V shall be in accordance with MIL-I-38535 for dynamic burn-in.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

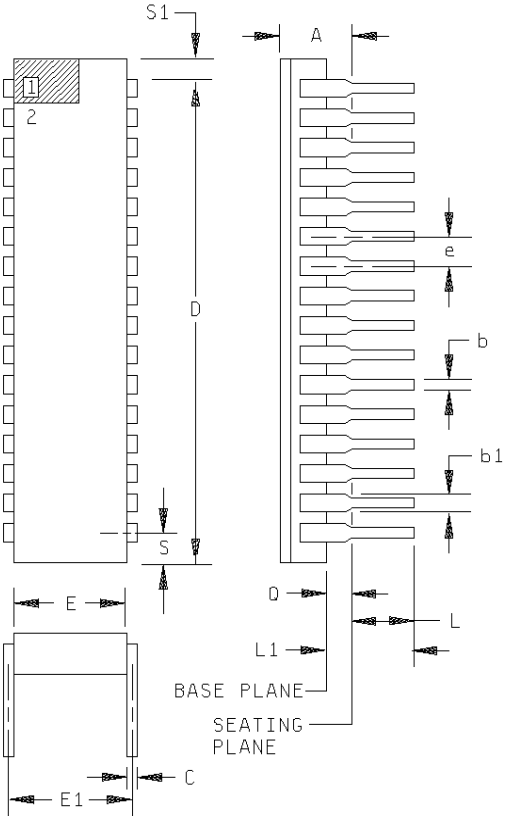
4.3.1.1 Qualification extension for device classes B and S. When authorized by the qualifying activity, if a manufacturer qualifies one device type which is identical (i.e., same die) to other device types on this specification, the slower device types may be part I qualified, upon the request of the manufacturer, without any further testing. The faster device types may be part I qualified by performing only group A qualification testing.

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.3 Electrostatic discharge sensitivity inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

Case X



Dimensions		
Letter	Inches	Millimeters
A	.232 max	5.89
b	.014/.023	0.36/0.58
b1	.033/.065	0.84/1.66
c	.008/.015	0.20/0.38
D	1.690 max	42.93
E	.570/.610	14.48/15.49
E1	.590/.620	14.99/15.76
e	.100 BSC	2.54
L	.125/.200	3.18/5.08
L1	.150 min	3.81
Q	.015/.060	0.38/1.51
S	.100 max	2.54
S1	.005 min	0.13

NOTE: Configurations 1 and e of MIL-M-38510 appendix C may be used.

FIGURE 1. Case outline.

Case Z

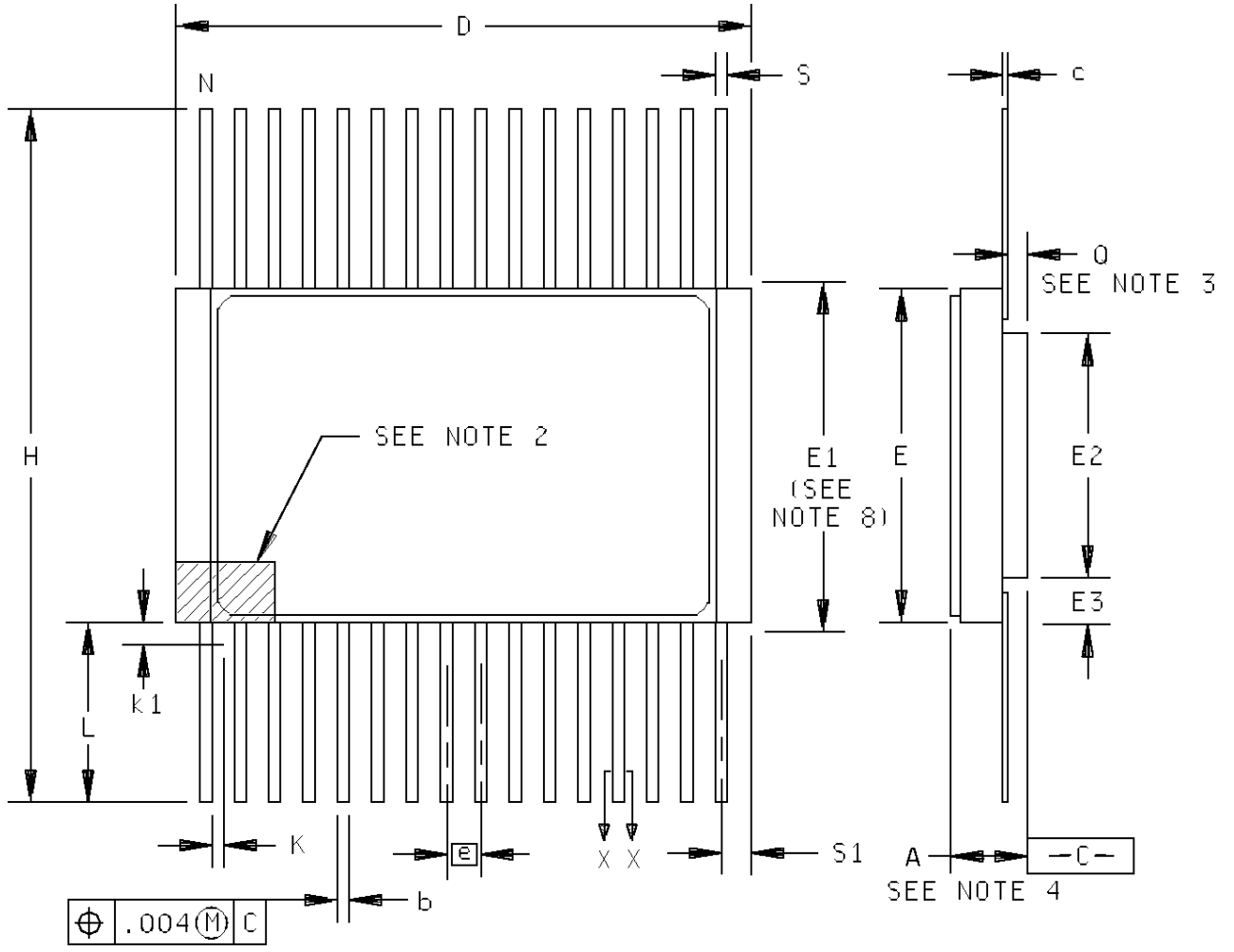


FIGURE 1. Case outline - Continued.

Variations (all dimensions shown in inches)			
Symbol			
	Min	Max	Notes
A	.090	.120	4
b	.015	.020	
b1	.015	.019	
C	.004	.007	
C1	.004	.006	
D		.830	
E	.430	.488	
E1		.498	
E2	.330	.498	8
E3	.030		
e	.050 BSC		
H		1.228	
k	.008	.015	2, 5
k1	.025 ref		2, 5
L	.270	.370	
Q	.026	.045	3
S	.005		
S1		.045	
N	32		6

Inches	mm	Inches	mm	Inches	mm
.004	0.10	.020	0.51	.270	6.86
.005	0.13	.025	0.64	.350	8.89
.006	0.15	.026	0.66	.370	9.40
.007	0.18	.030	0.76	.472	11.99
.008	0.20	.045	1.14	.488	12.40
.015	0.38	.050	1.27	.498	12.65
.019	0.48	.120	3.05	1.228	31.19

NOTES:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Index area: An identification mark shall be located adjacent to pin 1 within the shaded area shown. Alternatively, a tab (dim k) may be used as shown.
3. Dimension Q shall be measured from the point on the lead located opposite the braze pad.
4. This dimension includes lid thickness.
5. Optional, see note 2. If pin 1 identification is used instead of this tab, the minimum dimension does not apply.
6. (N) indicates number of leads.
7. Uses a metal lid.
8. Includes braze fillet.
9. Metric equivalents are given for general information only.

FIGURE 1. Case outline - Continued.

Case U

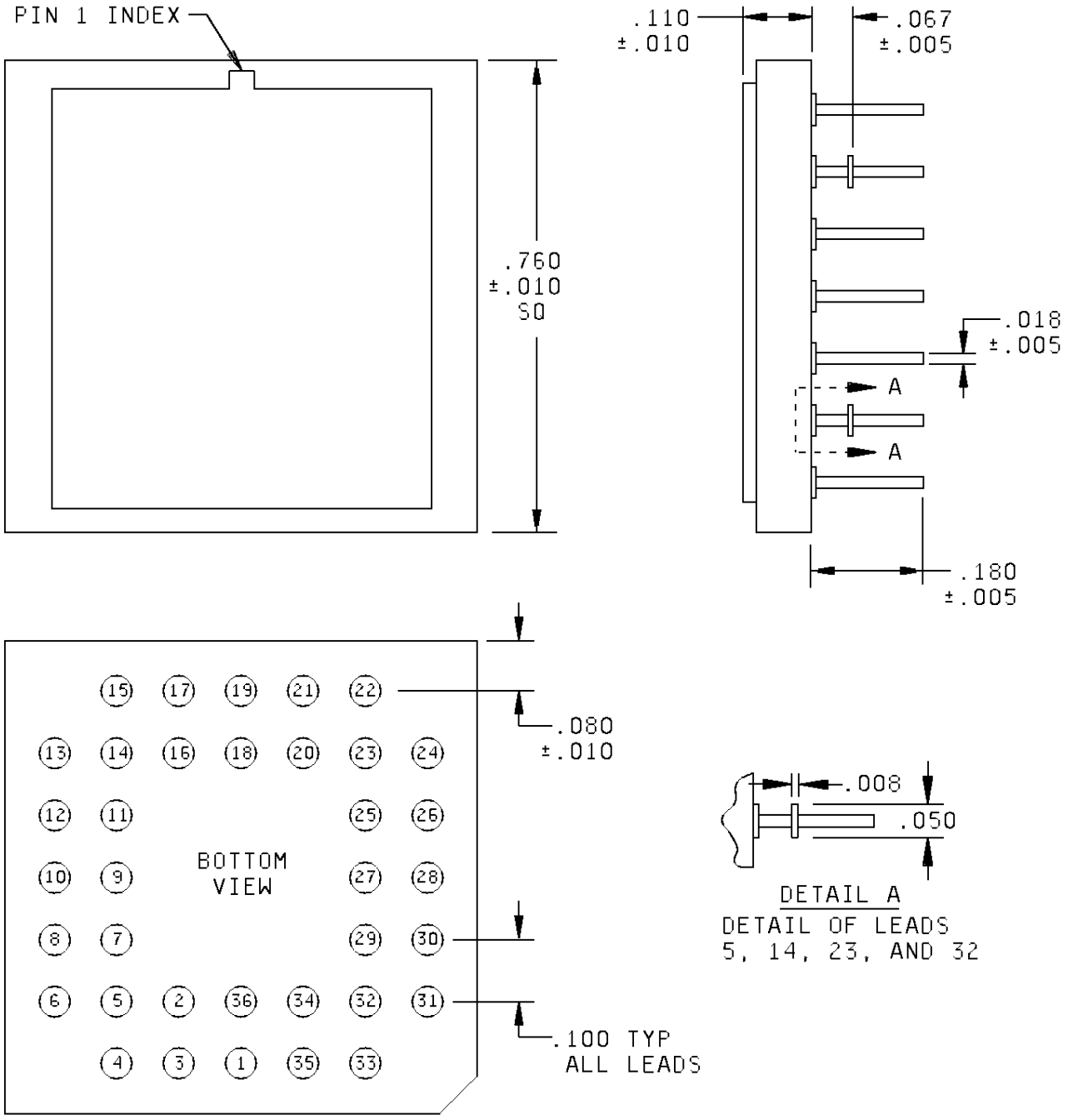


FIGURE 1. Case outline - Continued.

Device types	01-08		09-16
Case outlines	X, Y, and Z	U	Y
Terminal number	Terminal symbol		
1	NC	NC	A_{15}
2	NC	NC	A_{14}
3	A_{15}	NC	A_{12}
4	A_{12}	NC	A_7
5	A_7	A_{15}	A_6
6	A_6	A_{12}	A_5
7	A_5	A_7	A_4
8	A_4	A_6	A_3
9	A_3	A_5	A_2
10	A_2	A_4	A_1
11	A_1	A_3	A_0
12	A_0	A_2	NC
13	I/O_0	A_1	I/O_0
14	I/O_1	A_0	I/O_1
15	I/O_2	I/O_0	I/O_2
16	V_{SS}	I/O_1	V_{SS}
17	I/O_3	I/O_2	NC
18	I/O_4	V_{SS}	I/O_3
19	I/O_5	I/O_3	I/O_4
20	I/O_6	I/O_4	I/O_5
21	I/O_7	I/O_5	I/O_6
22	$\overline{CE}$	I/O_6	I/O_7
23	A_{10}	I/O_7	$\overline{CE}$
24	$\overline{OE}$	$\overline{CE}$	A_{10}
25	A_{11}	A_{10}	$\overline{OE}$
26	A_9	$\overline{OE}$	NC
27	A_8	A_{11}	A_{11}
28	A_{13}	A_9	A_9
29	A_{14}	A_8	A_8
30	NC	A_{13}	A_{13}
31	$\overline{WE}$	A_{14}	$\overline{WE}$
32	V_{CC}	NC	V_{CC}
33	--	NC	--
34	--	NC	--
35	--	$\overline{WE}$	--
36	--	V_{CC}	--

NC = no connection

FIGURE 2. Terminal connections.

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby	V_{IH}	X	X	High Z
Write inhibit	X	X	V_{IH}	D_{OUT} or high Z
Write inhibit	V_{IH}	X	X	High Z
Write inhibit	X	V_{IL}	X	D_{OUT} or high Z
Write inhibit	V_{IL}	V_{IL}	V_{IL}	No operation
Software chip clear	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Software write protect	V_{IL}	V_{IH}	V_{IL}	D_{IN}
High voltage chip clear	V_{IL}	V_H	V_{IL}	V_{IH}

V_{IH} = High logic, "1" state, V_{IL} = Low logic, "0" state.
X = logic "don't care" state, High Z = high impedance state.
V_H = Chip clear voltage, D_{OUT} = Data out, and
D_{IN} = Data in.

FIGURE 3. Truth table.

		0	1	2	3	4	5	6 225	226			509	510	511
R	0	AA	AA	AA	AA	AA	AA	AA AA	AA	AA	AA	AA	AA	AA
0	1	55	55	55	55	55	55	55 55	55	55	55	55	55	55
W	2	AA	AA	AA	AA	AA	AA	AA AA	AA	AA	AA	AA	AA	AA
	3	55	55	55	55	55	55	55 55	55	55	55	55	55	55
A														
D														
D														
R	125	AA	AA	AA	AA	AA	AA	AA AA	AA	AA	AA	AA	AA	AA
E	126	55	55	55	55	55	55	55 55	55	55	55	55	55	55
S	127	AA	AA	AA	AA	AA	AA	AA AA	AA	AA	AA	AA	AA	AA
S	128	55	55	55	55	55	55	55 55	55	55	55	55	55	55

NOTES:
1. All address numbers shown in decimal.
2. Each column/row address location corresponds to 1 byte.
3. All data numbers shown in hexadecimal.
   AA = 10101010 55 = 01010101
4. Manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern.

FIGURE 4. Data pattern.

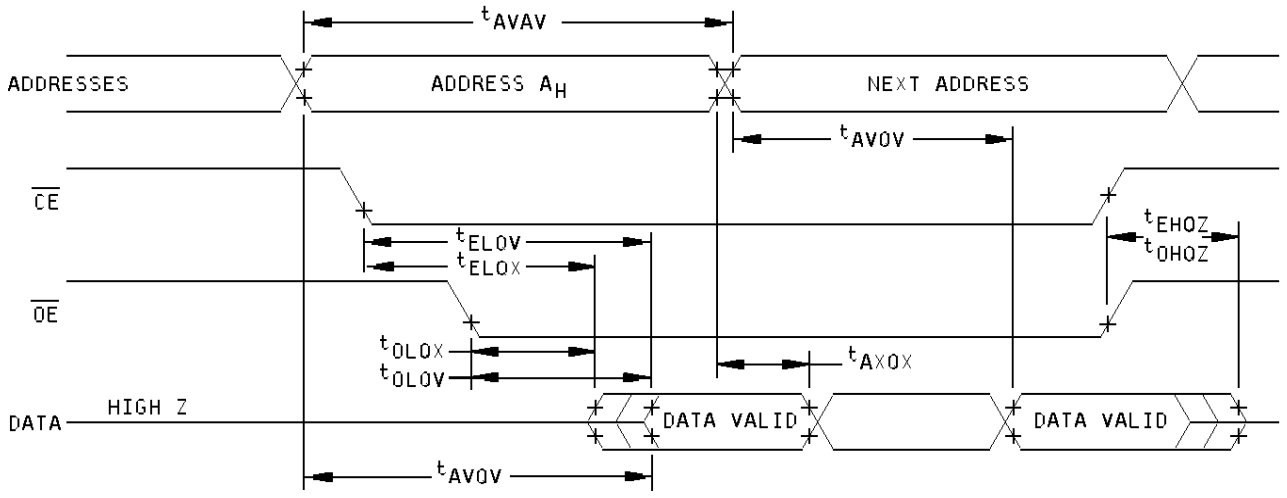


FIGURE 5. Read mode waveforms.

$\overline{WE}$ CONTROLLED BYTE WRITE WAVEFORMS
(ALL DEVICE TYPES)

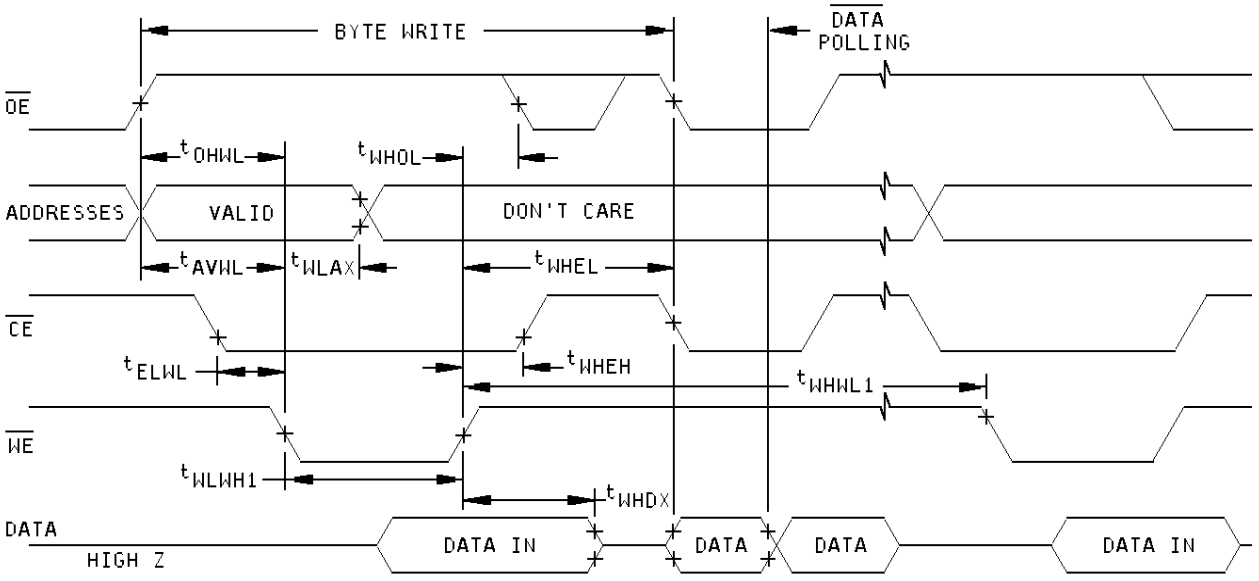


FIGURE 6. Waveforms.

$\overline{CE}$ CONTROLLED BYTE WRITE WAVEFORMS
(ALL DEVICE TYPES)

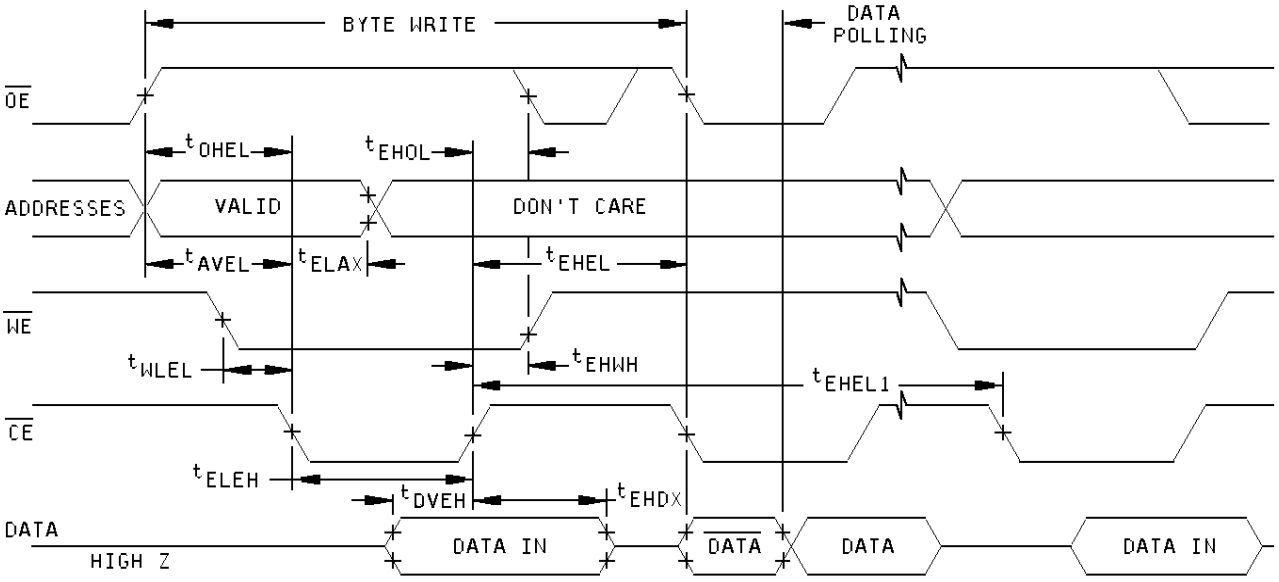


FIGURE 6. Waveforms - Continued.

PAGE MODE WRITE CYCLE WAVEFORMS
(ALL DEVICE TYPES)

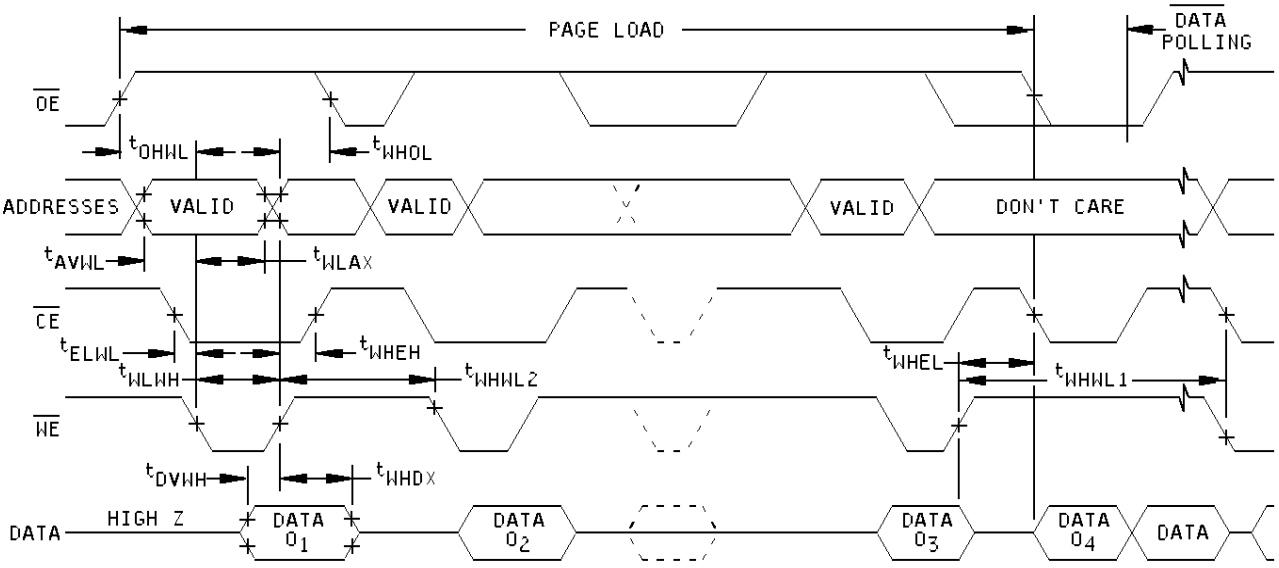


FIGURE 6. Waveforms - Continued.

(ALL DEVICE TYPES)

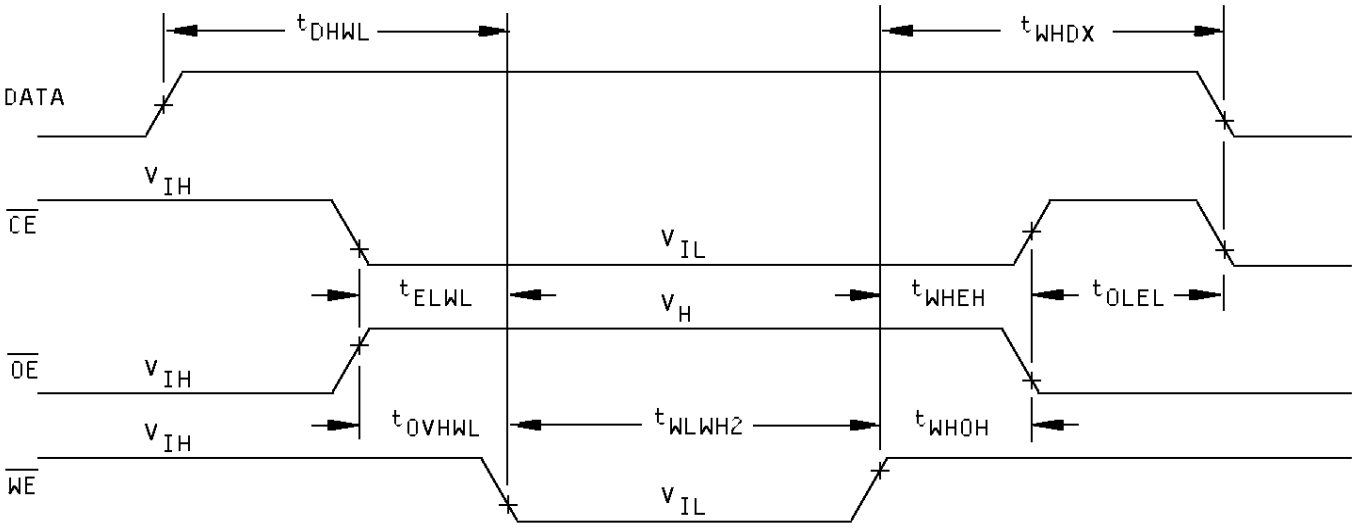
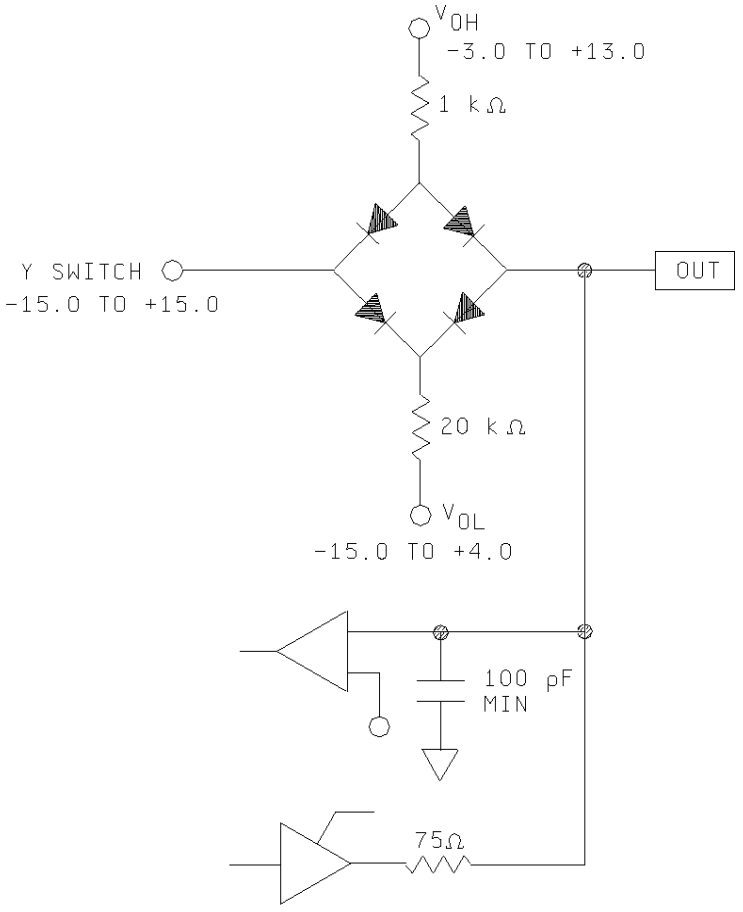


FIGURE 7. Chip erase mode waveforms.

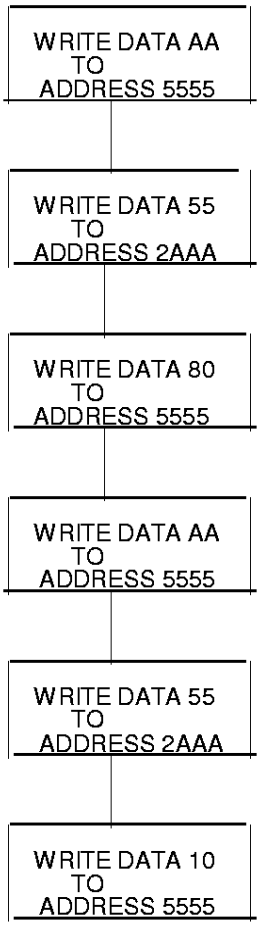


NOTES:
1. V_{OH} and V_{OL} will be adjusted to meet load conditions of table I.
2. Use this circuit or equivalent circuit.

FIGURE 8. Switching load circuit.

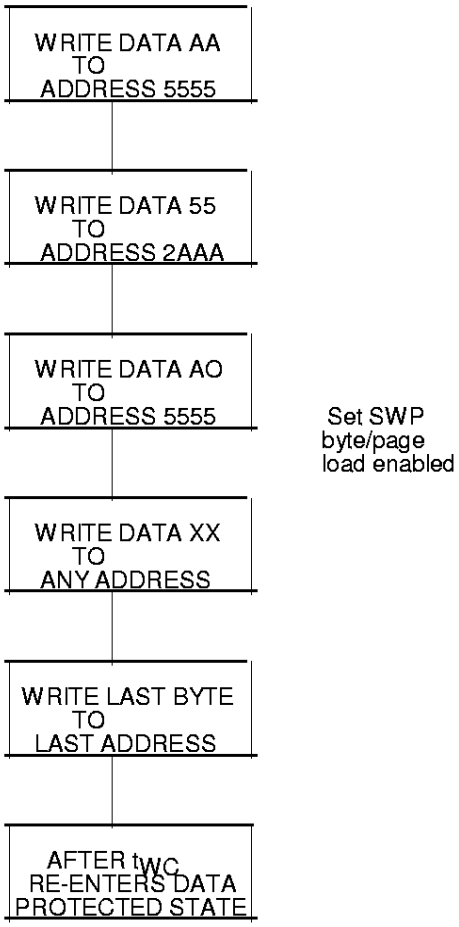
NOTE: When a qualified source exists, a circuit shall be provided and placed on this page.

Figure 9. Radiation hardness bias circuit.



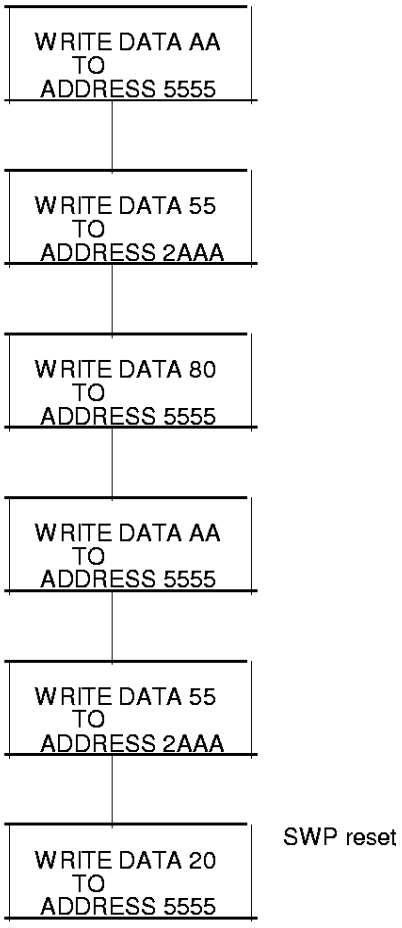
NOTES:
1. Software chip clear timings are referenced to $\overline{WE}$ and $\overline{CE}$ inputs, whichever is last to go low, and the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is first to go high.
2. The command sequence must conform to the page write timing.

FIGURE 10. Software chip clear and software write protect algorithm (all device types).



NOTES:
1. Reset software data protection timings are referenced to the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is last to go low, and the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is first to go high.
2. A minimum of one valid byte write must follow the first three bytes of the command sequence.
3. The command sequence and subsequent data must conform to page write timing.

FIGURE 11a. Set software write protect and software protected write algorithm.



NOTES:
1. Reset software data protection timings are referenced to the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is last to go low, and the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is first to go high.
2. The command sequence must conform to the page write timing.

FIGURE 11b. Reset software write protect algorithm.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/

Line no.	Test requirements	Subgroups (in accordance with method 5005 table I)			Subgroups (in (accordance with MIL-I-38535, table III)	
		Device class M	Device class B	Device class S	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9 or 2,8A,10	1,7,9 or 1,2,8A,10	1,7,9 or 2,8A,10	1,7,9 or 1,2,8A,10
2	Static burn-in I & II method 1015	Not required	Not required	Required	Not required	Required
3	Same as line 1			1*,7* Δ		1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required	Required	Required
5	Same as line 1			1*,7* Δ		1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements 7/	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11
8	Group B end-point electrical parameters			1,2,3,7, 8A,8B,9, 10,11 Δ		1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B,9, 10,11 8/ Δ		1,2,3,7, 8A,8B,9, 10,11 8/ Δ	
10	Group D end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B
11	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

See footnotes on top of next page.

TABLE IIA. Electrical test requirements - Continued.

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIC) shall be required where specified, and the delta values shall be computed with reference to the previous electrical parameters (see table IIC).
7/ See table III.
8/ Delta limits required for initial qualification and after any design or process change.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hrs. at +125°C	100%
Radiographic	2012	100%

TABLE IIC. Delta limits at +25°C.

Test 1/	Device types
	All
I_{CC3} standby	±10% of specified value in table I
I_{IH}, I_{IL}	±10% of specified value in table I
I_{OHZ}, I_{OLZ}	±10% of specified value in table I

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

TABLE III. Input/output pulse levels for table I, subgroups 7, 8, 9, 10, and 11.

Symbol	Terminals	A	B	Device type	Units
V_{CC}	V_{CC}	4.5	5.5	All	V
V_{IH}	Logic inputs address and control pins	2.4	2.4	All	V
V_{IL}	Logic inputs address and control pins	0.4	0.4	All	V
V_{OH}	Logic output compare level	2.0	2.0	All	V
V_{OL}	Logic output compare level	0.8	0.8	All	V
t_{AVQV}	Address	250	250	01,02,09,10	ns
		200	200	03,04,11,12	ns
		150	150	05,06,13,14	ns
		120	120	07,08,15,16	ns
t_{ELQV}	Chip enable	250	250	01,02,09,10	ns
		200	200	03,04,11,12	ns
		150	150	05,06,13,14	ns
		120	120	07,08,15,16	ns
t_{OLQV}	Output enable	50.0	50.0	All	ns
t_{AXQX}	I/O_0-I/O_7	0.0	0.0	All	ns

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity.I For device classes Q and V subgroups 7 and 8 shall include verifying the functionality of the device, these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. Procedures and circuitsshall besubmitted to DESC-ECS for class M devices. For classes B and S, the procedures and circuitsshall be submitted to the qualifying activity. For classes Q and V, the procedures and circuits shall be submitted to DESC-ECS and shall be as indicated in the QM plan and will be under the control of the device manufacturer's technical review board (TRB). Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive.

d. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 Mhz. Sample size is fifteen devices with no failures, and all input and output terminals tested.

e. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be cleardd and verified, (except device submitted for groups B, C, and D testing).

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

a. For device class S only, steady-state life tests shall be conducted using test condition D and the circuit described in 4.2.1c herein, or equivalent as approved by the qualifying activity.

b. For device class S only, end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table IIC herein.

c. All devices selected for class S electrical testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified, (except devices submitted to group C and D).

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIC herein.

4.4.3.1 Additional criteria for device classes M, B, and S.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) The devices selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be cleared and verified (except devices submitted for group D testing).

(2) Test condition D or E. For device class M, the test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device class B and S, the test circuit shall be submitted to the qualifying activity.

(3) T_A = +125°C, minimum.

(4) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

b. An endurance test, as specified in method 1033 of MIL-STD-883, shall be added to group C, subgroup 1 inspection prior to performing the steady-state life test (see 4.4.3.1a) and extended data retention (see 4.4.3.1c). Cycling may be block, byte, or page from devices passing group A after the completion of the requirements of 4.2 herein. Initially two groups of devices shall be formed, cell 1 and cell 2. The following conditions shall be met:

(1) Cell 1 shall be cycled at -55°C and cell 2 shall be cycled at +125°C for a minimum of 10,000 cycles for device types.

(2) Perform group A, subgroups 1, 7, and 9 after cycling. Form new cells (cell 3 and cell 4) for steady-state life and extended data retention. Cell 3 for steady-state life test consists of one-half of the devices from cell 1 and one-half of the devices from cell 2. Cell 4 for extended data retention consists of the remaining devices from cell 1 and cell 2.

(3) Extended data retention test shall consist of the following:

a. All devices shall be programmed with a charge on all memory cells in each device, such that loss of charge (e.g., leakage in the cell) can be detected (e.g., worst case pattern).

b. Unbiased bake for 1,000 hours (minimum) at +150°C (minimum). The unbiased bake time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship and with the apparent activation of 0.6 eV. The maximum bake temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

c. Read the pattern after bake and perform end-point electrical tests in accordance with table IIA herein for group C.

(4) The sample plans for cell 1, cell 2, cell 3, and cell 4 shall individually be the same as for group C, subgroup 1, as specified in method 5005 of MIL-STD-883, and shall individually pass the specified sample plan.

c. After the completion of all testing, the devices shall be cleared and verified prior to delivery.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-3853. After the completion of all testing, the devices shall be erased and verified prior to delivery.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein. The devices selected for testing shall be programmed with a checkerboard pattern (see figure 10). After completion of all testing, the devices shall be erased and verified.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document or to a higher qualified level. RHA tests for device classes Q and V shall be performed in accordance with MIL-I-38535 and 1.2.1 herein.

a. RHA tests for device classes B, S, Q, and V for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IA herein. RHA samples need not be tested at -55°C or +125°C prior to total dose irradiation.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. The samples shall pass the specified group A electrical parameters for subgroups specified in table IIA herein. Additionally, classes Q and V for quality conformance inspection may be at wafer level.

d. The devices shall be subjected to radiation hardness assurance tests as specified in MIL-M-38510 for device classes M, B, and S, and MIL-I-38535 for device classes Q and V, for the RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure.

e. Prior to and during total dose irradiation, the devices shall be biased to the worst case conditions established during characterization (see figure 9 herein).

f. Single Event Phenomena (SEP) testing shall be performed on all class S and V devices. SEP testing shall be performed at initial qualification and after any design or process changes which may affect the upset or latchup characteristics of the device. Test four devices with zero failures. ASTM standard F1192-88 may be used as a guideline when performing SEP testing. For device class V, the device parametrics that influence single event upset immunity shall be monitored at the wafer level as part of a TRB approved wafer level hardness plan. The test conditions for SEP are as follows:

(1) The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

(2) The fluence shall be greater than 100 errors or ≥ 10^7 ions/cm^2.

(3) The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

(4) The particle range shall be ≥ 20 microns in silicon.

(5) The test temperatures shall be +25°C and the maximum rated operating temperature ±10°C.

(6) Bias conditions shall be V_{CC} = 4.5 V dc for the upset measurements and V_{CC} = 5.5 V dc for latch-up measurements.

(7) For SEP test limits, see table IB herein.

g. For device classes M, B, and S, subgroups 1 and 2 of table V method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

h. Transient dose rate upset testing for class Q and V devices ahall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-I-38535.

i. Transient dose rate survivability testing for class Q and V devices shall be performed as specifed by a TRB approved radiation hardness assurance plan and MIL-I-38535. Device parametric parameters that influence latch-up and device burn-out shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-I-38535.

j. When specified in the purchase order or contract a copy of the following additional data shall be supplied.

(1) RHA delta limits.

(2) RHA upset levels

(3) Test conditions (SEP).

(4) Number of upsets (SEP).

(5) Number of transients.

(6) Occurrence of latch-up.

4.5 Delta measurements for device classes B, S, Q, and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIC.

4.6 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.6.1 Voltages and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6.2 Life test, burn-in, cool down and electrical test procedure. When devices are measured at +25°C following application of the steady state life or burn-in test condition, all devices shall be cooled to +35°C or within +10°C of the power stable condition prior to removal of bias voltages/signals. Any electrical tests required shall first be performed at -55°C or +25°C prior to any required tests at +125°C.

4.6.3 Writing procedure. The waveforms and timing relationships shown on figure 6 and the conditions specified in table IA shall be adhered to. Initially and after each chip clear (see 4.6.4), all bits are in the high state (output at V_{OH}).

4.6.3.1 Byte write operation. Information is introduced by selectively writing "L" (logic "0" level) or "H" (logic "1" level) into the desired bit. A written "L" can be changed to an "H" by writing an "H". No clearing is necessary (see 4.6.4).

4.6.3.2 Page write operation. The page write operation can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to 127 bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ ($\overline{CE}$) HIGH to LOW transition, must begin within 150 µs of the falling edge of the preceding $\overline{WE}$ ($\overline{CE}$) high to low transition, [twlwh1+twhwl2] or [teleh1+tehel2]. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 150 µs, the internal automatic write cycle will commence. The successive writes need not be sequential; however, the page address (A7 through A16) for each write during a page write operation shall be the same.

4.6.3.3 Data polling operation. During the internal writing cycle after a byte or page write operation, an attempt to read the last byte written will produce the complement of that data on all I/O or I/07 (i.e., write data - 0xxx xxxx and read data - 1xxx xxx). Once the writing cycle has completed, all I/0 or I/O7 will reflect true data (i.e. write data - 0xxx xxx, read data - 0xxx xxx).

4.6.3.4 Toggle bit. Toggle bit determines the end of the internal write cycle. While the internal write cycle is in progress $I/0_6$ toggles from 1 to 0 and 0 to 1 on sequential polling reads. When the internal write cycle is complete, the toggling stops and the device is ready for additional read/write operations.

4.6.4 Clearing procedure. The waveforms and timing relationship shown on figures 5, 6, 7, and 8 and the conditions specified in table IA shall be adhered to. Initially and after each chip clear, all bits are in the high state (output at V_{OH}).

4.6.4.1 Byte clearing. A byte is cleared by simultaneously writing an "H" state into each bit at the selected address (see 4.6.3). This can be done by a byte write cycle or a page mode write cycle (see figure 6).

4.6.4.2 Software chip clear. Software chip clear is performed by executing a series of instructions to the device (see figure 10). At the end of the step sequence, the device begins and completes chip clear internally. The waveforms and timing relationships shown on figures 6 and 7, and the test conditions and limits specified in table IA apply.

4.6.4.3 High voltage chip clear. The device is cleared by setting the $\overline{OE}$ (output enable) pin to V_H (see figure 7) while all other inputs are set in the normal byte erase mode (see 4.6.4.2). After chip clear, all bits are in the "H" state. (Applies to all device types.)

4.6.5 Read mode operation. The device is in the read mode whenever the CE and $\overline{OE}$ pins are at V_{IL}. The waveforms and timing relationships shown on figure 5 and the test conditions and limits specified in table I shall be applied.

4.6.6 Extended page load. The write cycle must be "stretched" by maintaining $\overline{WE}$ low, assuming a write enable-controlled cycle, and leaving all other control inputs ($\overline{CE}$, $\overline{OE}$) in the proper page load cycle state. Since the page load timer is reset on the falling edge of $\overline{WE}$, keeping this signal low will inhibit the page timer. When $\overline{WE}$ returns high, the input data is latched and the page load cycle timer begins in $\overline{CE}$ controlled write. The same is true, with $\overline{CE}$ holding the timer reset instead of $\overline{WE}$.

4.6.7 Software data protection. Device types 01 through 15 software data protection offers a method of preventing inadvertent writes. The instruction, waveforms, and timing relationships shown on figures 5, 6, 11a, and figure 11b, and the conditions specified in table IA shall apply.

4.6.7.1 Set software protection. Device types 01 through 15 are placed in protected state by writing a series of instructions (see figure 11A) to the device. Once protected, writing to the device may only be preformed by executing the same sequence of instructions appended with either a byte write operation or page write operation. The waveforms and timing relationship shown on figure 6 and the test conditions and limits specified in table IA apply.

4.6.7.2 Reset software data protection. Device types 01 through 15 protection feature is reset by writing a series of instructions (see figure 11b) to the device. The waveforms and timing relationships shown on figure 6 and the test conditions and limits specified in table IA apply.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

C_{IN} C_{OUT}	Input and bidirectional output, terminal-to-GND capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
I_{IL}	Input current low.
I_{IH}	Input current high.
T_C	Case temperature.
T_A	Ambient temperature.
V_{CC}	Positive supply voltage.
V_H	Output enable and write enable voltage during chip erase.
O/V	Latch-up over-voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. Thus the format is:

t X X X X

Signal name from which interval is defined _____

Transition direction for first signal _____

Signal name to which interval is defined _____

Transition direction for second signal _____

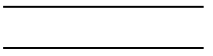
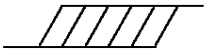
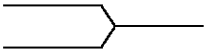
a. Signal definitions:

A = Address
D = Data in
Q = Data out
W = Write enable
E = Chip enable
O = Output enable

b. Transition definitions:

H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid or don't care
Z = Transition to off (high impedance)

6.5.3 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECS and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 91-10-18

Approved sources of supply for SMD 5962-90869 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9086901MXX	60395	X28C512DMB-25
5962-9086901MYX	60395	X28C512EMB-25
5962-9086901MZX	60395	X28C512FMB-25
5962-9086901MUX	60395	X28C512KMB-25
5962-9086902MXX	60395	X28C512DMB-25
5962-9086902MYX	60395	X28C512EMB-25
5962-9086902MZX	60395	X28C512FMB-25
5962-9086902MUX	60395	X28C512KMB-25
5962-9086903MXX	60395	X28C512DMB-20
5962-9086903MYX	60395	X28C512EMB-20
5962-9086903MZX	60395	X28C512FMB-20
5962-9086903MUX	60395	X28C512KMB-20
5962-9086904MXX	60395	X28C512DMB-20
5962-9086904MYX	60395	X28C512EMB-20
5962-9086904MZX	60395	X28C512FMB-20

See footnote at end of list.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9086904MUX	60395	X28C512KMB-20
5962-9086905MXX	60395	X28C512DMB-15
5962-9086905MYX	60395	X28C512EMB-15
5962-9086905MZX	60395	X28C512FMB-15
5962-9086905MUX	60395	X28C512KMB-15
5962-9086906MXX	60395	X28C512DMB-15
5962-9086906MYX	60395	X28C512EMB-15
5962-9086906MZX	60395	X28C512FMB-15
5962-9086906MUX	60395	X28C512KMB-15
5962-9086907MXX	60395	X28C512DMB-12
5962-9086907MYX	60395	X28C512EMB-12
5962-9086907MZX	60395	X28C512FMB-12
5962-9086907MUX	60395	X28C512KMB-12
5962-9086908MXX	60395	X28C512DMB-12
5962-9086908MYX	60395	X28C512EMB-12
5962-9086908MZX	60395	X28C512FMB-12
5962-9086908MUX	60395	X28C512KMB-12
5962-9086909MYX	60395	X28C513EMB-25
5962-9086910MYX	60395	X28C513EMB-25
5962-9086911MYX	60395	X28C513EMB-20

See footnote at end of list.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9086912MYX	60395	X28C513EMB-20
5962-9086913MYX	60395	X28C513EMB-15
5962-9086914MYX	60395	X28C513EMB-15
5962-9086915MYX	60395	X28C513EMB-12
5962-9086916MYX	60395	X28C513EMB-12

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
60395	Xicor, Incorporated 851 Buckeye Court Milpitas, CA 95035