CY27C512

64K x 8 CMOS EPROM

Features

- **Very Fast Read Access Time: (45 - 200 ns)**
- **5V ± 10% Power Supply**
- **Capable of withstanding >2001V ESD**
- **Latch-up Protection up to 200mA**
- **Two line control functions to prevent bus contention**
- **Standard JEDEC Packages**
  - **— 32-pin PLCC**
  - **— 28-pin TSOP**
  - **— 28-pin, 600-mil plastic DIP**
  - **— 32-pin, hermetic LCC**
  - **— 28-pin, 600-mil hermetic DIP**
- **Available in Commercial, Industrial, and Military Temperature Ranges**

Functional Description

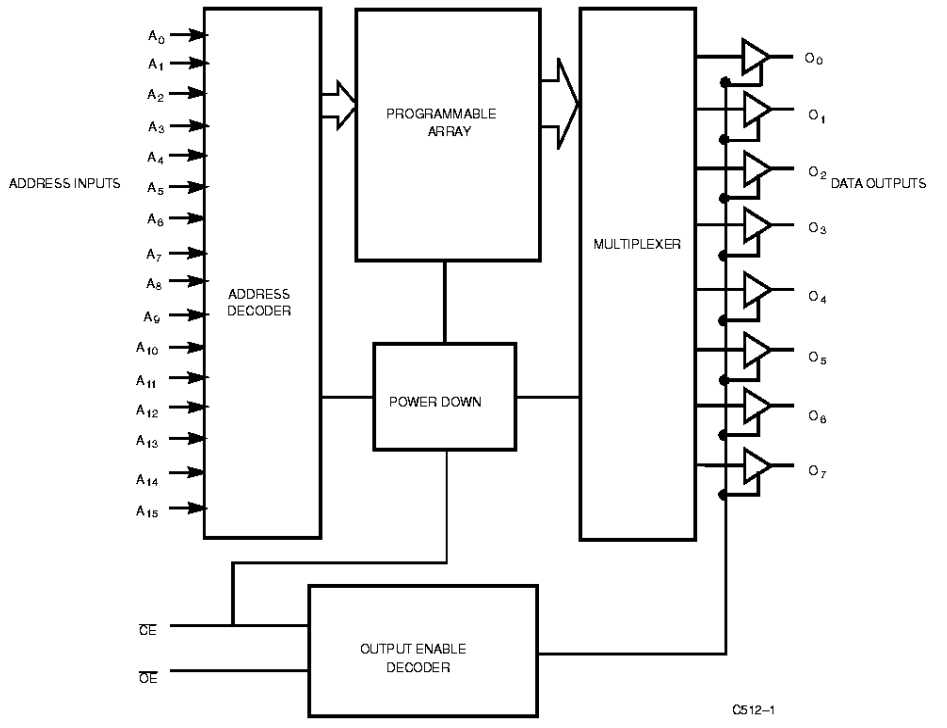
The CY27C512 is a high-performance, 512-Kbit ultraviolet erasable programmable read-only memory (EPROM) organized as 64 Kbytes by 8 bits. It is available in JEDEC-standard, one-time programmable (OTP), 32-pin PLCC and 28-pin PDIP and TSOP packages. The CY27C512 is also available in windowed packages (28-pin hermetic DIP and and 32-pin LCC) which allow the device to be erased with UV light for 100% reprogrammability.

The CY27C512 is equipped with a power-down chip enable ($\overline{CE}$) input and output enable ($\overline{OE}$) to prevent bus contention. When $\overline{CE}$ is deasserted, the device powers down to a low-power stand-by mode. The $\overline{OE}$ pin three-states the outputs without putting the device into stand-by mode. While $\overline{CE}$ offers lower power, $\overline{OE}$ provides a more rapid transition to and from three-stated outputs.

The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

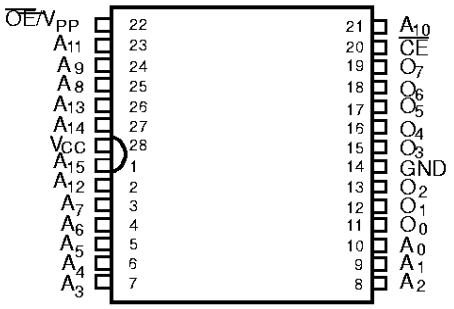
The CY27C512 is read by asserting both the $\overline{CE}$ and the $\overline{OE}$ inputs. The contents of the memory location selected by the address on inputs A_{15}–A_0 will appear at the outputs O_7–O_0.

Logic Block Diagram



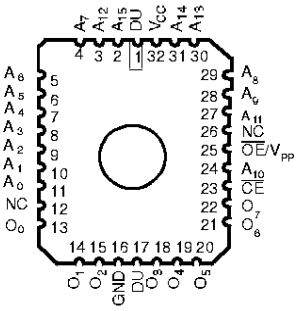
Pin Configurations

TSOP (Z)
Top View



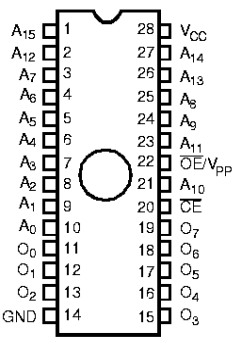
C512–2

PLCC/LCC (J and Q)[1]
Top View



C512–3

DIP/WDIP (P and W)
Top View



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Selection Guide

		–45	–55	–70	–90	–120	–150	–200
Maximum Access Time (ns)		45	55	70	90	120	150	200
$\overline{CE}$ Access Time (ns)		45	55	70	90	120	150	200
$\overline{OE}$ Access Time (ns)		20	20	25	30	40	50	60
I_{CC}[2] (mA) Power Supply Current	Com'l(Max)	50	50	50	50	50	50	50
	Mil	60	60	60	60	60	60	60
I_{SB}[3] (mA) Stand-by Current	Com'l(Max)	15	15	15	15	15	15	15
	Mil	25	25	25	25	25	25	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +5.5V

DC Input Voltage..... –3.0V to +7.0V

Transient Input Voltage .....–3.0V for <20 ns

DC Program Voltage.....13.0 V

UV Erasure..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[4]	–40°C to +85°C	5V ± 10%
Military[5]	–55°C to +125°C	5V ± 10%

Notes:

1. For LCC/PLCC only: Pins 1 and 17 are designated as DU (DON'T USE) and should not be used.
2. V_{CC} = Max., I_{OUT} = 0 mA, f=5 MHz.
3. V_{CC} = Max., $\overline{CE}$ = V_{IH}.
4. Contact a Cypress representative for industrial temperature range specification.
5. T_A is the "instant on" case temperature.

DC Electrical Characteristics Over the Operating Range[6, 7]

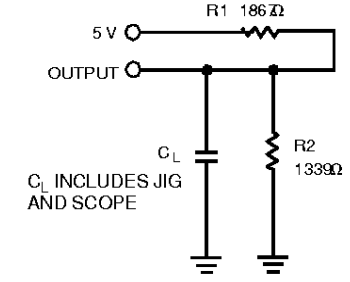
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –400µA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2 mA			0.45	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}+0.5	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		–10	+10	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disable		–10	+10	µA
I_{CC}	Power Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=5 MHz	Com'l		50	mA
			Mil		60	mA
I_{SB}	Stand-By Current	V_{CC}=Max., $\overline{CE}$ = V_{IH}	Com'l		15	mA
			Mil		25	mA

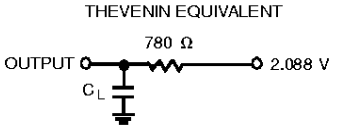
Capacitance[8]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
6. See the last page of this specification for Group A subgroup testing information.
7. See Introduction to CMOS NVMs in this Data Book for general information on testing.
8. This parameter is sampled only and is not 100% tested.

AC Test Loads and Waveforms





Notes: C_L = 30pF for –45 and –55 devices
C_L = 100pF for –70, –90, –120, –150, and –200 devices
C_L = 5pF for t_{DF}

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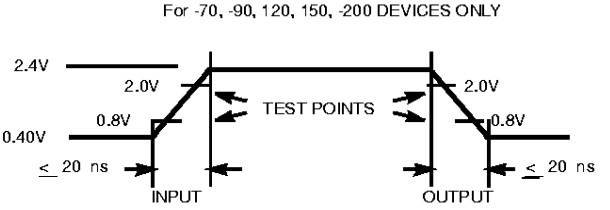
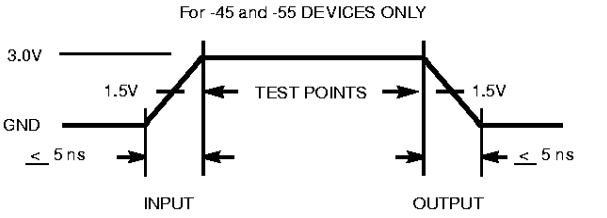


INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC 1 AND 0.40V FOR A LOGIC 0.



INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC 1 AND 0.0V FOR A LOGIC 0.

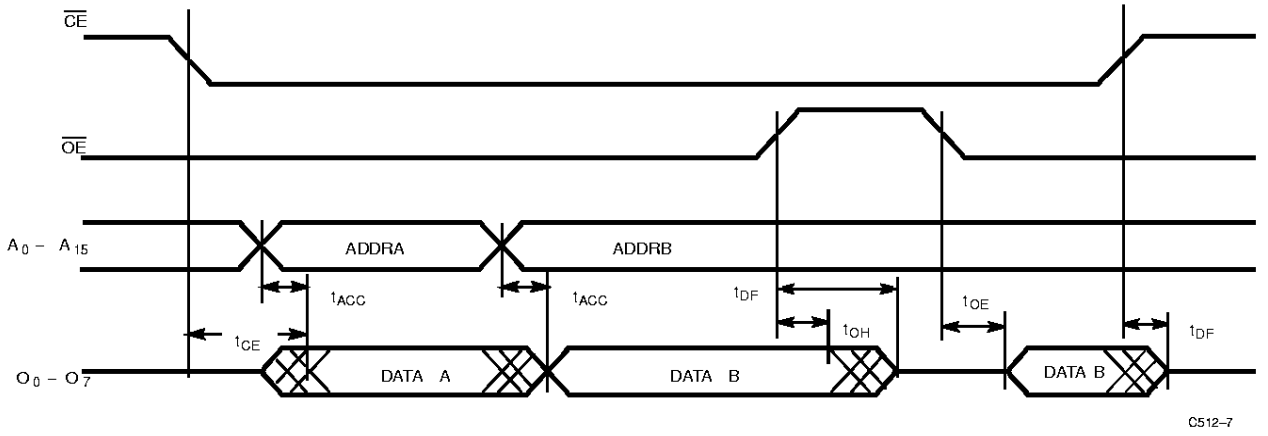
C512–6

Switching Characteristics Over the Operating Range

Parameter	Description	-45		-55		-70		-90		-120		-150		-200		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Valid		45		55		70		90		120		150		200	ns
t_{OE}	$\overline{OE}$ Active to Output Valid		20		20		25		30		35		40		60	ns
t_{DF}[9]	$\overline{OE}$ or $\overline{CE}$ Inactive to High Z, whichever occurs first		20		20		25		30		30		30		30	ns
t_{CE}	$\overline{CE}$ Active to Output Valid		45		55		70		90		120		150		200	ns
t_{OH}	Output Data Hold	0		0		0		0		0		0		0		ns

Note:
9. This parameter is sampled only and is not 100% tested.

Switching Waveform



Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the CY27C512 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 15 Wsec/cm2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 15 minutes. The CY27C512 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V_{PP}	Programming Power Supply	12.5	13	V
I_{PP}	Programming Supply Current		50	mA
V_{IHP}	Programming Input Voltage HIGH	3.0	V_{CC}	V
V_{ILP}	Programming Input Voltage LOW	–0.5	0.4	V
V_{CCP}	Programming V_{CC}	6.0	6.5	V

Table 2. Mode Selection

Mode	Pin Function[10]				
	$\overline{CE}$	$\overline{OE}/V_{PP}$	A_0	A_9	Outputs
Read	V_{IL}	V_{IL}	A_0	A_9	Dout
Output Disable	X	V_{IH}	X	X	High Z
Stand-by(TTL)	V_{IH}	X	X	X	High Z
Program	V_{ILP}	V_{PP}	A_0	A_9	Din
Program Verify	V_{ILP}	V_{ILP}	A_0	A_9	Dout
Program Inhibit	V_{IHP}	V_{PP}	X	X	High Z
Signature Read (MFG)[12]	V_{IL}	V_{IL}	V_{IL}	V_{HV}[11]	34H
Signature Read (DEV)[12]	V_{IL}	V_{IL}	V_{IH}	V_{HV}[11]	1FH

Note:

10. X can be V_{IL} or V_{IH}
11. V_{HV}=12V±0.5V
12. A_1 - A_8 and A_{10} - A_{15} = V_{IL}

Ordering Information [10]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY27C512-45JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512-45PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512-45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512-45ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512-45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	Military
	CY27C512-45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
55	CY27C512-55JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512-55PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512-55WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512-55ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512-55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	Military
	CY27C512-55WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
70	CY27C512-70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512-70PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512-70WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512-70ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512-70QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	Military
	CY27C512-70WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
90	CY27C512-90JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512-90PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512-90WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512-90ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512-90QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	Military
	CY27C512-90WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
120	CY27C512-120JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512-120PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512-120WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512-120ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512-120QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	Military
	CY27C512-120WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Ordering Information[10] (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
150	CY27C512-150JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512-150PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512-150WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512-150ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512-150QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	Military
	CY27C512-150WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
200	CY27C512-200JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C512-200PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C512-200WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27C512-200ZC	Z28	28-Lead Thin Small Outline Package	
	CY27C512-200QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	Military
	CY27C512-200WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Notes:
13. Contact a Cypress sales representative for industrial temperature offerings.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

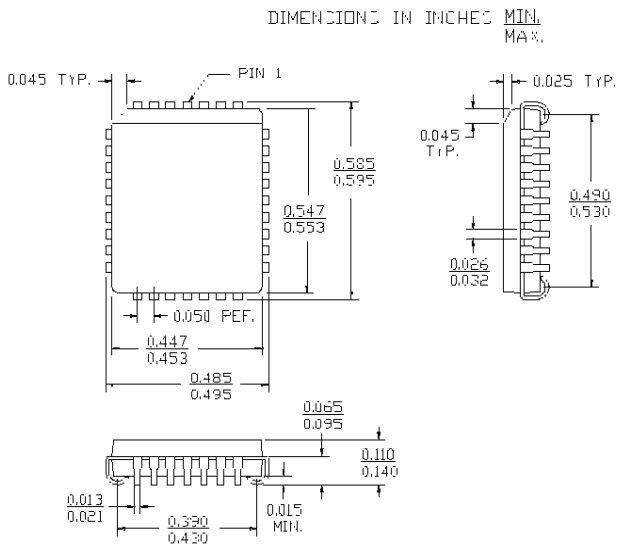
Switching Characteristics

Parameter	Subgroups
t_{ACC}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{CE}	7, 8, 9, 10, 11

Document #: 38-00428-A

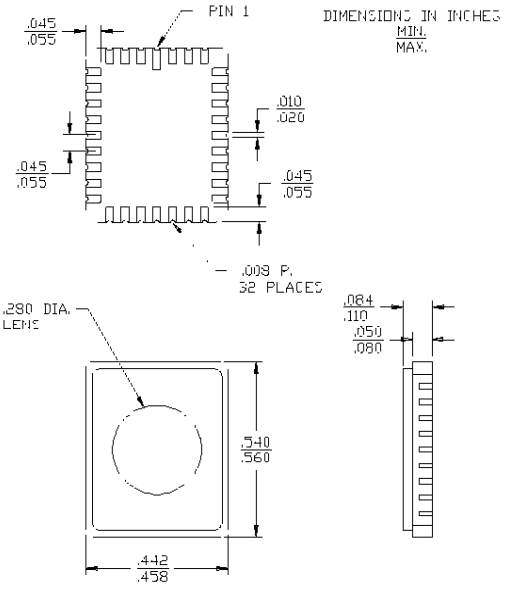
Package Diagrams

32-Lead Plastic Leaded Chip Carrier J65

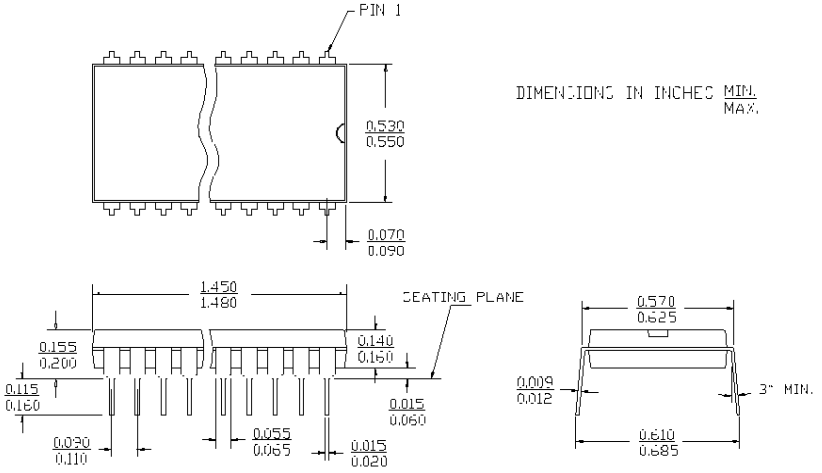


32-Pin Windowed Rectangular Leadless Chip Carrier Q55

MIL-STD-1835 C-12



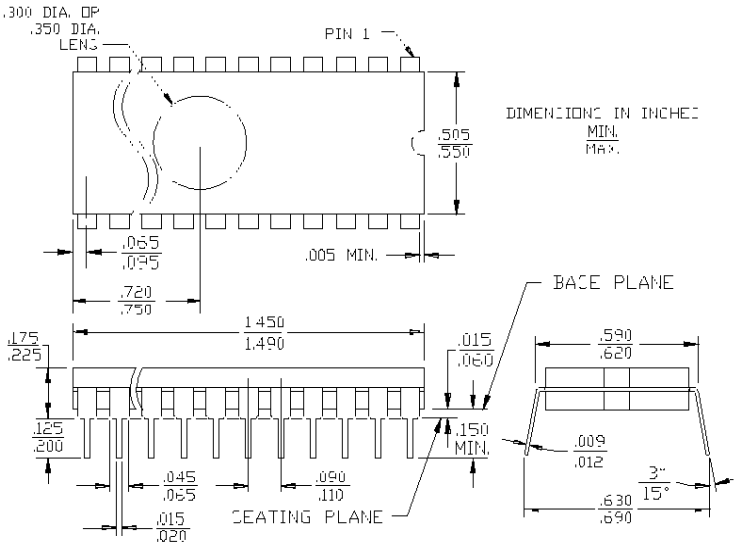
28-Lead (600-Mil) Molded DIP P15



Package Diagrams (continued)

28-Lead (600-Mil) Windowed CerDIP W16

MIL-STD-1835 D- 10Config.A



28-Lead Thin Small Outline Package Z28