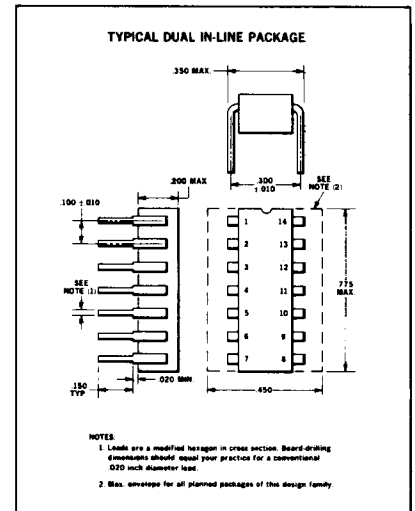
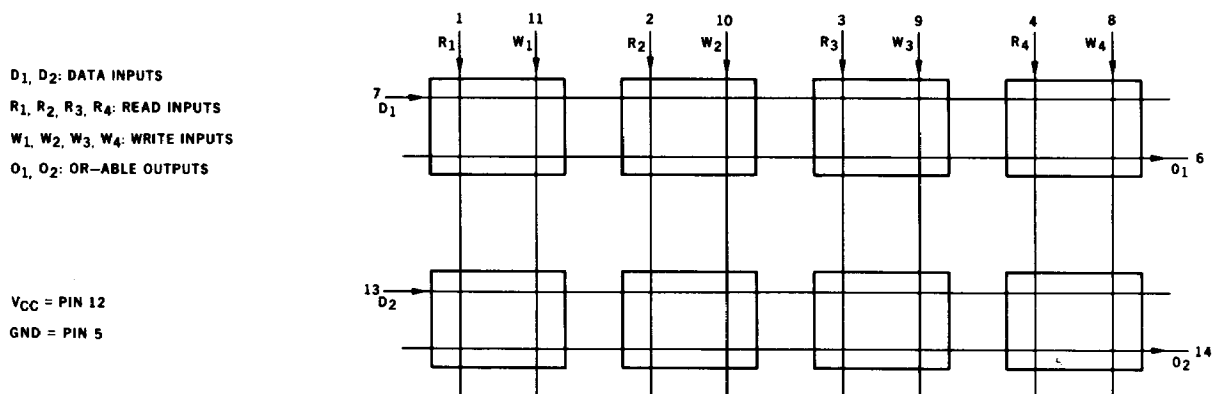


MEMORY MICROLOGIC® INTEGRATED CIRCUITS

***Planar is a Patented Fairchild Process.**



LOGIC DIAGRAM AND PIN ARRANGEMENTS



FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

FAIRCHILD MEMORY MICROLOGIC® INTEGRATED CIRCUITS M μ L9030

D.C. TESTS ($V_{CC} = 4.5V$, $T = 25^{\circ}C$)

DESCRIPTION	TEST	CONDITIONS	LIMITS		UNITS	EQUIV CT μ L LOAD
			MIN	MAX		
Read Input Current	I_1, I_2, I_3, I_4	$V_1, V_2, V_3, V_4 = 2.5V$		4.4	mA ea.	1.5
Data Input Current	I_7, I_{13}	$V_7, V_{13} = 2.5V$		4.4	mA ea.	1.5
Write Input Current	I_8, I_9, I_{10}, I_{11}	$V_8, V_9, V_{10}, V_{11} = 2.5V$		8.8	mA ea.	3
Output Voltage (High State)	V_6, V_{14}	$I_6, I_{14} = -10\text{ mA}$	2.35		V	
Output Voltage (Low State)	V_6, V_{14}	$I_6, I_{14} = -1\text{ mA}$		-0.36	V	
Output Leakage	I_6, I_{14}	$V_6, V_{14} = 4V$		5	μ A	
Output Capacitance	C_6, C_{14}	$V_6, V_{14} = 0$ Boonton Bridge		8	pF	

INPUT LEVEL: Maximum permissible "low" level = 0.8 V. Maximum required "high" level: 1.25 V.

RECOMMENDED OPERATING CONDITIONS:

The above test specifications characterize the terminal properties of the circuit under one set of conditions. They in no way limit the circuit to be used under different conditions where certain advantages may be achieved. In general, excessive heat generated in the circuit presents the largest factor in degrading the performance of the circuit. For noise immunity greater than 0.5 V and operating speed within 20% of $25^{\circ}C$ speed, junction temperature must be kept within $0-125^{\circ}C$. The circuit dissipates 350 mW with $V_{CC} = 4.5V \pm 10\%$ and full load. (F/O = 3 CT μ L Gates.)

Maximum thermal resistances of the package from junction to air are:

100°C/W in still air

65°C/W with 200 feet/min air flow

50°C/W with 400 feet/min air flow

For example, the circuit may be operated in still air at $T_A = 90^{\circ}C$ with $V_{CC} = 4.5V \pm 10\%$. Higher ambient temperatures are possible in moving air, as can be calculated from the data above.

The outputs of the M μ L 9030 may be "OR-ed" with the outputs of different words. Each output terminal represents 8 pF capacitance and 5 μ A leakage current. The limit on OR-tying outputs is the degradation of switching speed that the user can tolerate due to added capacitance.

Fan-out of the M μ L 9030 can be increased to 15 with only a slight increase in delay by buffering with the CT μ L 965.

SWITCHING TIME:

Load Resistance: 1 k to $-2V$ — Load Capacitance: 10 pF probe and jig capacitance — Input waveform rise and fall time: 6 ns

These tests are for correlations only. While t_1 through t_4 do not change with varied loads, t_5 , t_6 , and t_7 may differ under different output loading conditions.

SWITCHING TIME:

- t_1 : 25 ns MIN.
- t_2 : 10 ns MIN.
- t_3 : 10 ns MIN.
- t_4 : 10 ns MIN.
- t_5 : 25 ns MAX.
- t_6 : 25 ns MAX.
- t_7 : 25 ns MIN.

NOTE:

- 1) DOTTED LINES REPRESENT CELL STORING "LOW" LEVEL.
- 2) t_7 REPRESENTS TIME INTERVAL BETWEEN READ PULSES FOR ERROR-FREE READOUT.

