National Semiconductor

August 1998

100325
Low Power Hex ECL-to-TTL Translator

General Description

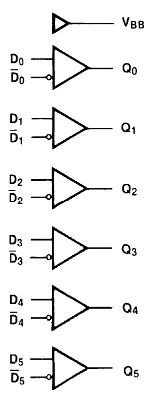
The 100325 is a hex translator for converting F100K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference voltage generator provides V_{BB} for single-ended operation, or for use in Schmitt trigger applications. All inputs have 50 kΩ pull-down resistors. When the inputs are either unconnected or at the same potential the outputs will go low.

When used in single-ended operation the apparent input threshold of the true inputs is 20 mV to 40 mV higher (positive) than the threshold of the complementary inputs. The V_{EE} and V_{TTL} power may be applied in either order.

Features

- Pin/function compatible with 100125
- Meets 100125 AC specifications
- 50% power reduction of the 100125
- Differential inputs with built in offset
- Standard FAST® outputs
- 2000V ESD protection
- −4.2V to −5.7V operating range
- Available to Microcircuit Drawing (SMD) 5962-9153101

Logic Diagram



DS100314-4

Pin Names	Description
D_0–D_5	Data Inputs
$\overline{D}_0$–$\overline{D}_5$	Inverting Data Inputs
Q_0–Q_5	Data Outputs

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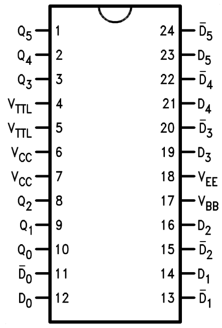
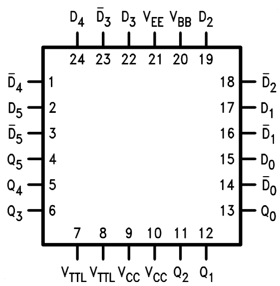
Connection Diagrams

24-Pin DIP



DS100314-1

24-Pin Quad Cerpak



DS100314-2

Truth Table

Inputs		Outputs
D_n	$\overline{D}_n$	Q_n
L	H	L
H	L	H
L	L	L
H	H	L
Open	Open	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Above which the useful life may be impaired.

Storage Temperature (T_{STG})	−65˚C to +150˚C
Maximum Junction Temperature (T_J)	
Ceramic	+175˚C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	−0.5V to +6.0V
Input Voltage (DC)	V_{EE} to +0.5V
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	−55˚C to +125˚C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55˚C to +125˚C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{BB}	Output Reference Voltage	−1380	−1260	mV	0˚C to +125˚C	I_{VBB} = −3 µA, V_{EE} = −4.2V		(Notes 3, 4, 5)
						I_{VBB} = −2.1 mA	V_{EE} = −5.7V	
		−1396	−1260		−55˚C	I_{VBB} = −3 mA		
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55˚C to +125˚C	Guaranteed HIGH Signal for All Inputs (with One Input Tied to V_{BB})		(Notes 3, 4, 5, 6)
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55˚C to +125˚C	Guaranteed LOW Signal for All Inputs (with One Input Tied to V_{BB})		(Notes 3, 4, 5, 6)
V_{OH}	Output HIGH Voltage	2.5		mV	0˚C to +125˚C	I_{OH} = −2.0 mA	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	(Notes 3, 4, 5)
		2.4			−55˚C			
V_{OL}	Output LOW Voltage		0.5	mV	−55˚C to +125˚C	I_{OL} = 20 mA		
V_{DIFF}	Input Voltage Differential	150		mV	−55˚C to +125˚C	Required for Full Output Swing		(Notes 3, 4, 5)
V_{CM}	Common Mode Voltage	−2000	−500	mV	−55˚C to +125˚C			(Notes 3, 4, 5, 6)
I_{IH}	Input HIGH Current		350	µA	0˚C to +125˚C	V_{IN} = $V_{IH\ (Max)}$, D_0–D_5 = V_{BB}, $\overline{D}_0$–$\overline{D}_5$ = $V_{IL\ (Min)}$		(Notes 3, 4, 5)
			500		−55˚C			
I_{IL}	Input LOW Current	0.50		µA	−55˚C to +125˚C	V_{IN} = $V_{IL\ (Min)}$, D_0–D_5 = V_{BB}		(Notes 3, 4, 5)
I_{OS}	Output Short Circuit Current	−150	−60	mA	−55˚C to +125˚C	V_{OUT} = GND Test One Output at a Time		(Notes 3, 4, 5)
I_{CEX}	Output HIGH Leakage Current		250	µA	−55˚C to +125˚C	V_{OUT} = 5.5V		(Notes 3, 4, 5)
I_{EE}	V_{EE} Power Supply Current	−35	−12	mA	−55˚C to +125˚C	D_0–D_5 = V_{BB}		(Notes 3, 4, 5)
I_{TTL}	V_{TTL} Power Supply Current		65	mA	−55˚C to +125˚C	D_0–D_5 = V_{BB}		(Notes 3, 4, 5)

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at −55˚C, +25˚C, and +125˚C, Subgroups 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table I) on each manufactured lot at −55˚C, + 25˚C, and +125˚C, Subgroups A1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = −55˚C		T_C = +25˚C		T_C = +125˚C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.50	5.00	1.60	4.70	1.70	5.70	ns	C_L = 50 pF *Figures 1, 3*	(Notes 7, 8, 9)

Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at +25˚C, temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each manufactured lot at +25˚C, Subgroup A9, and at +125˚C and −55˚C temperatures, Subgroups A10 and A11.

Note 10: Not tested at +25˚C, +125˚C, and −55˚C temperature (design characterization data).

Switching Waveform

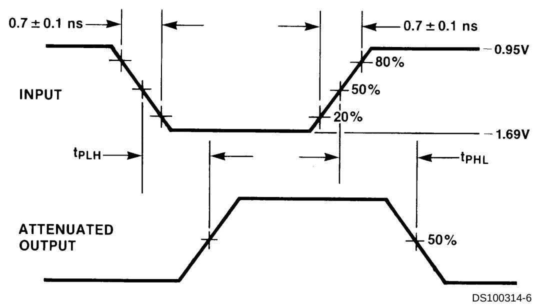
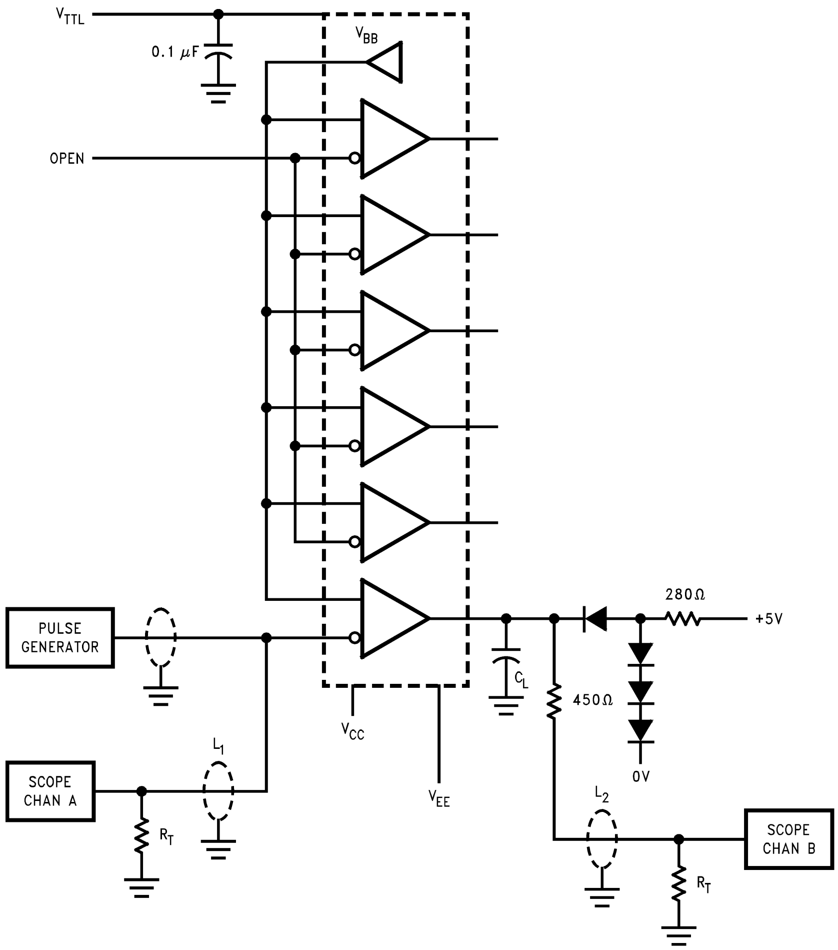


FIGURE 1. Propagation Delay

Test Circuits

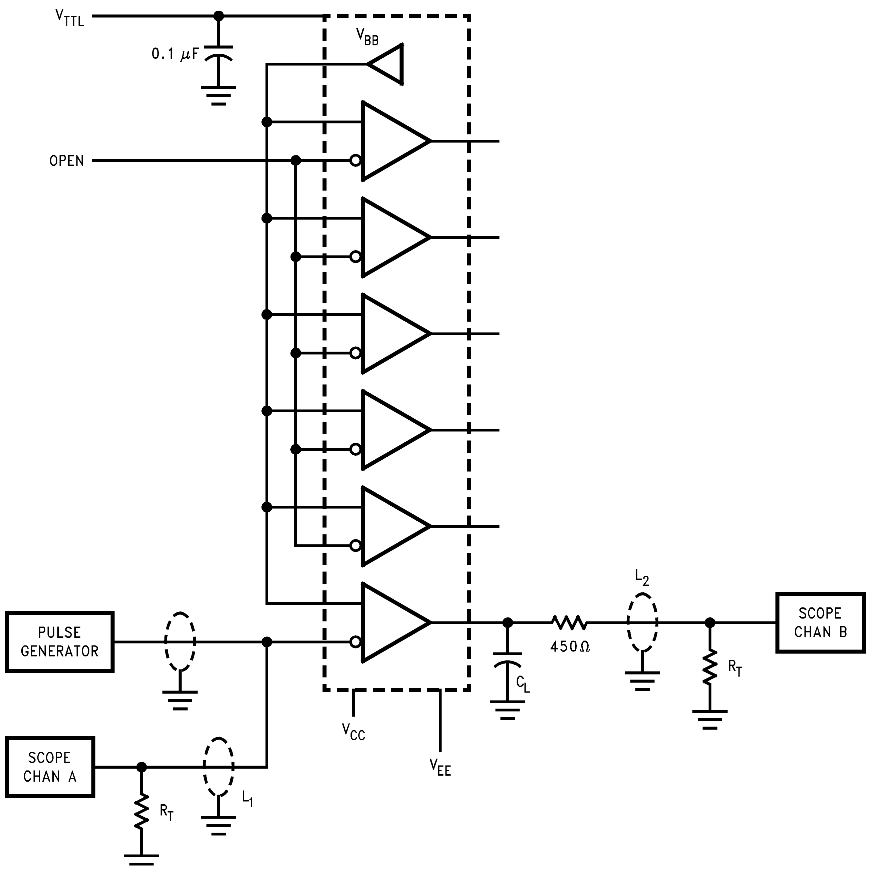


Notes:

V_{CC} = 0V, V_{EE} = −4.5V, V_{TTL} = +5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC}, V_{EE} and V_{TTL}
All unused outputs are loaded with 500Ω to GND
C_L = Fixture and stray capacitance = 15 pF

FIGURE 2. AC Test Circuit for 15 pF Loading

Test Circuits (Continued)



Notes:

V_{CC} = 0V, V_{EE} = −4.5V, V_{TTL} = +5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

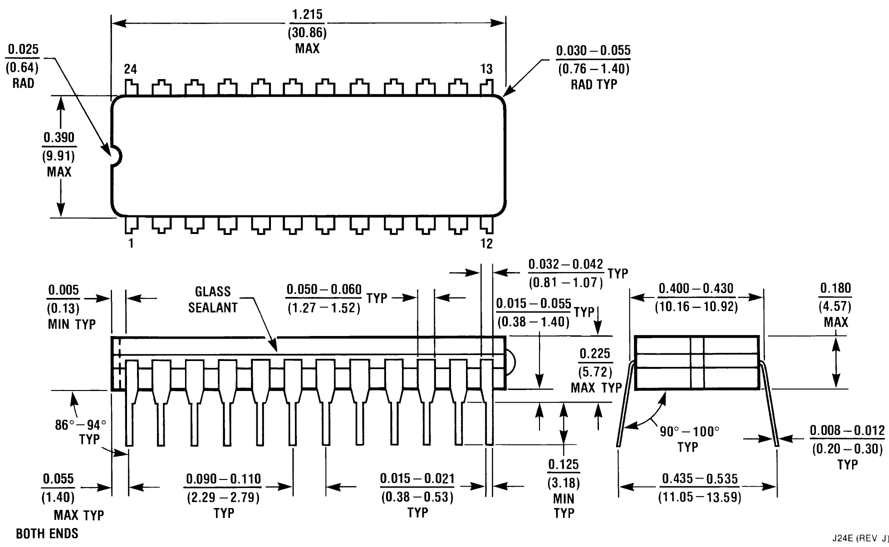
Decoupling 0.1 µF from GND to V_{CC}, V_{EE} and V_{TTL}

All unused outputs are loaded with 500Ω to GND

C_L = Fixture and stray capacitance = 50 pF

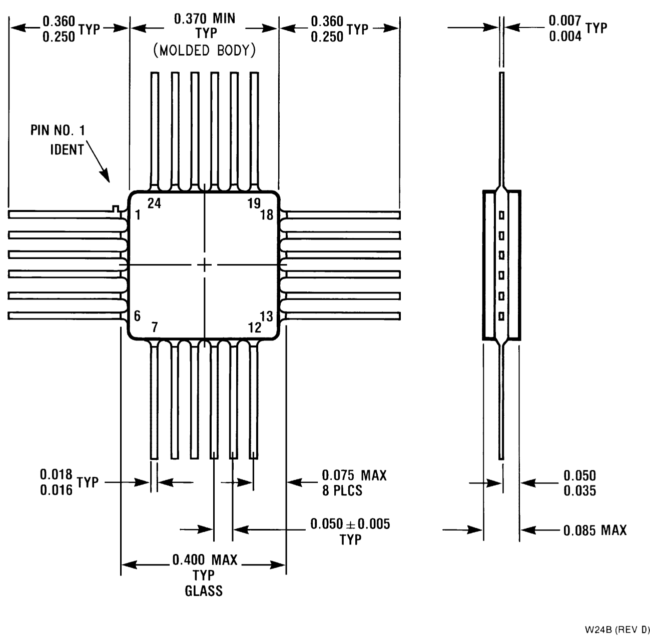
FIGURE 3. AC Test Circuit for 50 pF Loading

Physical Dimensions inches (millimeters) unless otherwise noted



J24E (REV J)

24 Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E



W24B (REV D)

24 Lead Quad Cerpak (F)
NS Package Number W24B

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