19-2127; Rev 0; 8/01

MAXIM

±15kV ESD-Protected USB Level Translator in UCSP

General Description

The MAX3340E bidirectional level translator converts logic-level signals to USB signals, and USB signals to logic-level signals. It includes the 1.5kΩ USB termination resistor internally, and supports both full-speed (12Mbps) and low-speed (1.5Mbps) USB operation. It has built-in ±15kV ESD protection circuitry to guard the USB I/O pins, D+ and D-.

The MAX3340E operates with V_L at voltages as low as 1.8V, ensuring compatibility with low-voltage ASICs. The MAX3340E features a logic selectable suspend mode that lowers current draw to less than 200µA. The MAX3340E has a unique re-enumerate feature that allows changes in USB communication protocol while the power is on. The MAX3340E is fully compliant with USB specification 1.1, and the full-speed and low-speed operation under USB specification 2.0.

The MAX3340E is available in the miniature 4 x 4 chip-scale package, as well as the small 14-pin TSSOP, and is rated for the -40°C to +85°C extended temperature range.

Applications

Cell Phones

PC Peripherals

Data Cradles

PDAs

MP3 Players

Features

- ♦ **±15kV ESD Protection on D+ and D-**
- ♦ **Allows Single-Ended or Differential Logic I/O**
- ♦ **Internal Linear Regulator Allows Direct Powering from the USB**
- ♦ **Internal 1.5kΩ Termination Resistor for Low/Full-Speed**
- ♦ **Supports Low-Speed and Full-Speed USB Communications**
- ♦ **Complies with USB Standard 1.1**
- ♦ **Three-State Outputs**
- ♦ **Re-Enumerate with Power Applied**
- ♦ **Up to 15mA Available from the +3.3V Linear Regulator to Power External Circuitry**
- ♦ **No Power-Supply Sequencing Required**
- ♦ **Dual Function Logic Minimizes System Connections**
- ♦ **Operates with V_L of 1.8V to 3.6V, Ensuring Compatibility with Low-Voltage ASICs**
- ♦ **Available in Miniature Chip-Scale Package**

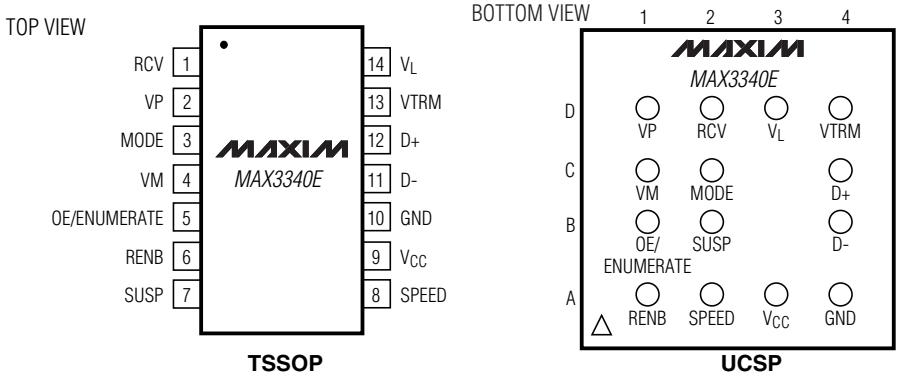
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3340EEUD	-40°C to +85°C	14 TSSOP
MAX3340EEBE*	-40°C to +85°C	16 UCSP**

**Future product—contact factory for availability.*

***UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and environment. Refer to the UCSP Reliability Notice in the UCSP Reliability section of this data sheet for more information.*

Pin Configurations



±15kV ESD-Protected USB Level Translator in UCSP

ABSOLUTE MAXIMUM RATINGS

(All voltages refer to GND unless otherwise noted)

V_{CC} .....-0.3V to +6V
V_L .....-0.3V to +5.5V
D+, D- .....-0.3V to (VTRM + 0.3V)
VP, VM, SUSP, OE/ENUMERATE, MODE, SPEED, RENB, RCV .....-0.3V to (V_L + 0.3V)
VTRM .....-0.3V to (V_{CC} + 0.3V)
Maximum Continuous Output Current .....±50mA
Short-Circuit Duration (D+, D- to V_{CC} or GND).....Continuous

Continuous Power Dissipation (T_A = +70°C)
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
16-Pin UCSP (derate 7.4mW/°C above +70°C) 589mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Solder Profile (MAX3340EEBE) .....(Note 1)
Lead Temperature (soldering 10s) .....+300°C

Note 1: For UCSP solder profile information visit www.maxim-ic.com/1st_pages/UCSP.htm

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4V to +5.5V, GND = 0, V_L = +1.8V to +3.6V, D+ to GND = 15kΩ, D- to GND = 15kΩ, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB Supply Voltage	V_{CC}		4		5.5	V
USB Supply Current	I_{CC}	Transmitter-enabled, OE/ENUMERATE low, output static		3	5	mA
USB Supply Current (Suspend Mode)	I_{CC}	SUSP high, OE/ENUMERATE floating, D+, D- static		90	200	µA
LINEAR REGULATOR						
VTRM Voltage		I_{VTRM} = 0 or 15mA, C_{OUT} = 1µF	3.0	3.3	3.6	V
PSRR		10kHz, I_{VTRM} = 15mA, C_{OUT} = 1µF		55		dB
External Capacitor			1			µF
Continuous Output Current	I_{VTRM}		15			mA
ESD PROTECTION (D+, D-)						
Human Body Model				±15		kV
IEC1000-4-2 Air-Gap Discharge				±9		kV
IEC1000-4-2 Contact Discharge				±5		kV
LOGIC-SIDE I/O						
V_L Input Range	V_L		1.8		3.6	V
V_L Supply Current	I_L	RCV, VP, VM open, output static		40		µA
Input High Voltage (Note 3)	V_{IH}		(2/3) x V_L			V
Input Low Voltage (Note 3)	V_{IL}				0.4	V
Output High Voltage (Note 3)	V_{OH}	I_{SOURCE} = +1mA	(2/3) x V_L			V
Output Low Voltage (Note 3)	V_{OL}	I_{SINK} = -1mA			0.4	V
OE/ENUMERATE Input High Voltage	V_{EH}		V_L - 0.4			V
OE/ENUMERATE Input Low Voltage	V_{EL}				0.4	V
OE/ENUMERATE Input Impedance				400		kΩ
USB-SIDE I/O						
Output Voltage Low	V_{OLD}	D+, D-; 1.5kΩ from D+ or D- to 3.6V, I_{SINK} = 1mA			0.3	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4V to +5.5V, GND = 0, V_L = +1.8V to +3.6V, D+ to GND = 15kΩ, D- to GND = 15kΩ, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage High	V_{OHD}	D+, D-; 15kΩ from D+ and D- to GND, I_{SOURCE} = 1mA	2.8			V
Input Impedance	Z_{INP}	D+, D-, OE/ENUMERATE floating	300			kΩ
Single-Ended Input Voltage High	V_{IHD}	D+, D- for VP/VM	2.0			V
Single-Ended Input Voltage Low	V_{ILD}	D+, D- for VP/VM			0.8	V
D+, D- Receiver Hysteresis				200		mV
Driver Output Impedance (Note 4)	R_{OUT}	D+, D- steady state drive I_{VTRM} = 15mA	6		18	Ω
Internal Resistor	R_{PULLUP}		1.425	1.5	1.575	kΩ
Termination Voltage		I_{VTRM} = 0	3		3.6	V
High-Z State Input Leakage		D+, D-; SUSP high	-10		10	µA
Input Common-Mode Voltage Range			0.8		2.5	V

TIMING CHARACTERISTICS

(V_{CC} = +4V to +5.5V, GND = 0, V_L = +1.8V to +3.6V, D+ to GND = 15kΩ, D- to GND = 15kΩ, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPEED INDEPENDENT TIMING CHARACTERISTICS						
RENB to Receive Three-State Delay Disable-Time	t_{PVZ}	(Figure 1a)			17	ns
RENB to Receiver Delay Enable-Time	t_{PZV}	(Figure 1a)	15			ns
D+/D- RCV Propagation Delay	t_{PLH}	C_{LOAD} = 25pF			25	ns
D+/D- RCV Propagation Delay	t_{PHL}	C_{LOAD} = 25pF			25	ns
D+/D- to VP Propagation Delay	t_{PLH}	C_{LOAD} = 25pF			12	ns
D+/D- to VP Propagation Delay	t_{PHL}	C_{LOAD} = 25pF			12	ns
RCV Rise-Time	t_R	C_{LOAD} = 25pF			10	ns
RCV Fall-Time	t_F	C_{LOAD} = 25pF			10	ns
FULL-SPEED TIMING CHARACTERISTICS						
OE/ENUMERATE to Transmit Delay Enable-Time	t_{PZD}	(Figure 1b)	15			ns
OE/ENUMERATE to Driver Three-State Delay Disable-Time	t_{PDZ}	(Figure 1b)			17	ns
VP/VM to D+/D- Propagation Delay (MODE 1)	t_{PLH}	(Figure 3)			25	ns

TIMING CHARACTERISTICS (continued)

(V_{CC} = +4V to +5.5V, GND = 0, V_L = +1.8V to +3.6V, D+ to GND = 15kΩ, D- to GND = 15kΩ, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VM/VP to D+/D- Propagation Delay (MODE 1)	t_{PHL}	(Figure 3)			25	ns
VP and VM Rise-Time	t_R	Single-ended receiver, C_{LOAD} = 25pF			10	ns
VP and VM Fall-Time	t_F	Single-ended receiver, C_{LOAD} = 25pF			10	ns
D+, D- Rise-Time MODE = 1 (Note 5)	t_R	C_{LOAD} = 50pF	4		20	ns
D+, D- Fall-Time (Note 5) MODE = 1	t_F	C_{LOAD} = 50pF	4		20	ns
Rise- and Fall-Time Matching MODE = 1 (Note 5)	t_R/t_F	C_{LOAD} = 50pF	90		110	%
Output Signal Crossover Voltage MODE = 1 (Note 5)	V_{CRS}	C_{LOAD} = 50pF	1.3		2	V
Time to Ignore SE0			14			ns
VP to D+/D- Propagation Delay MODE = 0 (Note 5)	t_P	C_{LOAD} = 50pF (Figure 2)			30	ns
D+/D- Rise-Time MODE = 0 (Note 5)	t_R	C_{LOAD} = 50pF	4		20	ns
D+, D- Fall-Time MODE = 0 (Note 5)	t_F	C_{LOAD} = 50pF	4		20	ns
Rise- and Fall-Time Matching MODE = 0 (Note 5)	t_R/t_F	C_{LOAD} = 50pF	90		110	%
Output Signal Crossover MODE = 0 (Note 5)	V_{CRS}	C_{LOAD} = 50pF	1.3		2	V
LOW-SPEED TIMING CHARACTERISTICS						
OE/ENUMERATE to Transmit Delay Enable-Time	t_{PZD}	(Figure 1b)	15			ns
OE/ENUMERATE to Driver Three-State Delay Disable-Time	t_{PDZ}	(Figure 1b)			17	ns
VP/VM to D+/D- Propagation Delay (MODE = 1)	t_{PLH}	(Figure 3) C_{LOAD} = 50pF to 600pF	30		200	ns
VM/VP to D+/D- Propagation Delay (MODE = 1)	t_{PHL}	(Figure 3) C_{LOAD} = 50pF to 600pF	30		200	ns

TIMING CHARACTERISTICS (continued)

(V_{CC} = +4V to +5.5V, GND = 0, V_L = +1.8V to +3.6V, D+ to GND = 15kΩ, D- to GND = 15kΩ, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Transition Rise-Time MODE = 1 (Note 5)	t_R	C_{LOAD} = 50pF to 600pF	75		300	ns
Transition Fall-Time MODE = 1 (Note 5)	t_F	C_{LOAD} = 50pF to 600pF	75		300	ns
Rise- and Fall-Time Matching MODE = 1 (Note 5)	t_R/t_F	C_{LOAD} = 50pF to 600pF	80		125	%
Time to Ignore SE0			210			ns
Output Signal Crossover Voltage MODE = 1 (Note 5)	V_{CRS}	C_{LOAD} = 50pF to 600pF	1.3		2	V
VP to D+/D- Propagation Delay MODE = 0	t_P	(Figure 2) C_{LOAD} = 50pF to 600pF	30		200	ns
Transition Rise-Time MODE = 0 (Note 5)	t_R	C_{LOAD} = 50pF to 600pF	75		300	ns
Transition Fall-Time MODE = 0 (Note 5)	t_F	C_{LOAD} = 50pF to 600pF	75		300	ns
Rise- and Fall-Time Matching MODE = 0 (Note 5)	t_R/t_F	C_{LOAD} = 50pF to 600pF	80		125	%
Output Signal Crossover Voltage MODE = 0 (Note 5)	V_{CRS}	C_{LOAD} = 50pF to 600pF	1.3		2	V

Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the entire operating temperature range are guaranteed by design and characterization but are not production tested.

Note 3: Logic side refers to RCV, VP, VM, SUSP, SPEED, MODE, and RENB.

Note 4: Excludes external resistors. In order to comply with USB specification 1.1, external 24Ω (±1%) series resistors are recommended at D+ and D-.

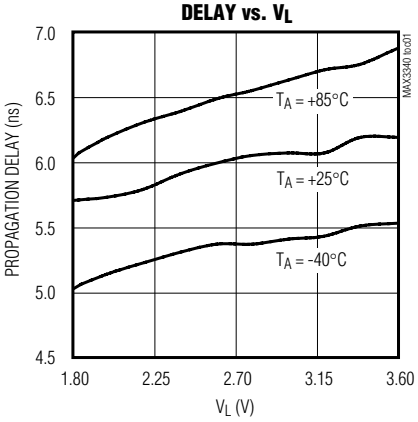
Note 5: Not guaranteed if VP = VM = high.

±15kV ESD-Protected USB Level Translator in UCSP

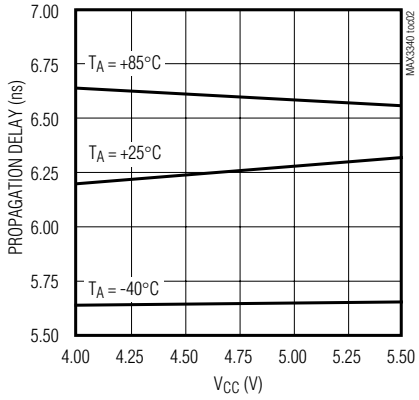
Typical Operating Characteristics

(V_{CC} = +5V, V_L =+3.3V T_A = +25°C, unless otherwise noted.)

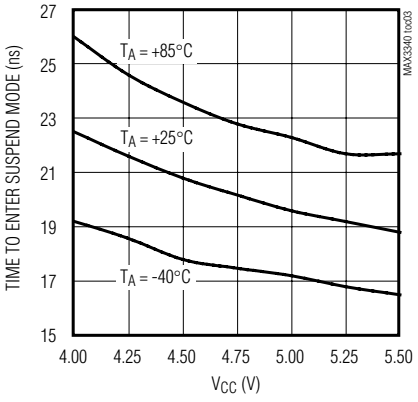
SINGLE-ENDED RECEIVER PROPAGATION DELAY vs. V_L



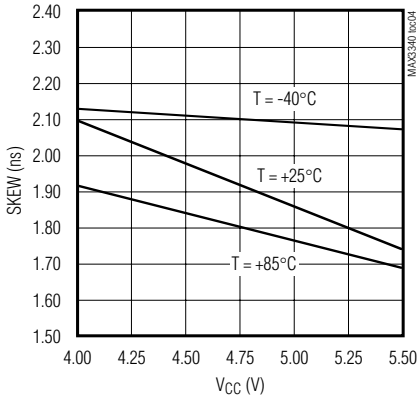
SINGLE-ENDED RECEIVER PROPAGATION DELAY vs. V_{CC}



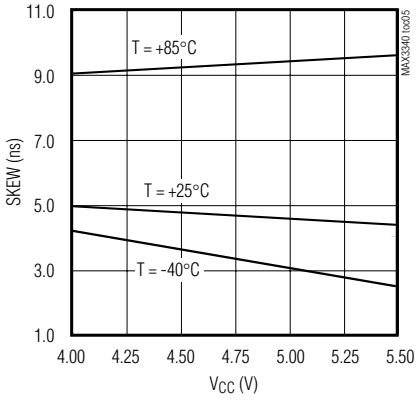
TIME TO ENTER SUSPEND MODE vs. V_{CC}



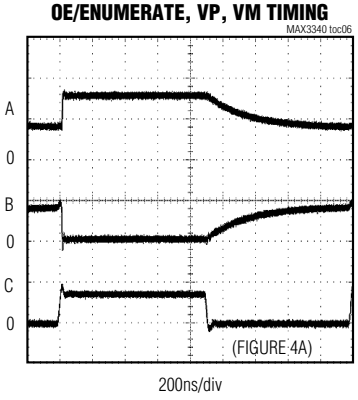
SKEW vs. V_{CC} (MODE 0) (HIGH SPEED)



SKEW vs. V_{CC} (MODE 0) (LOW SPEED)

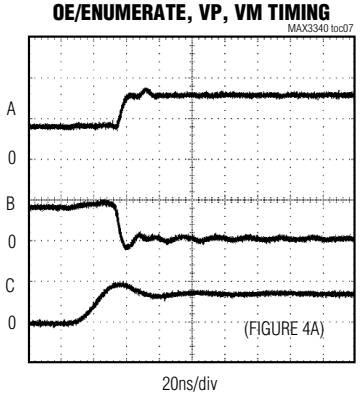


OE/ENUMERATE, VP, VM TIMING



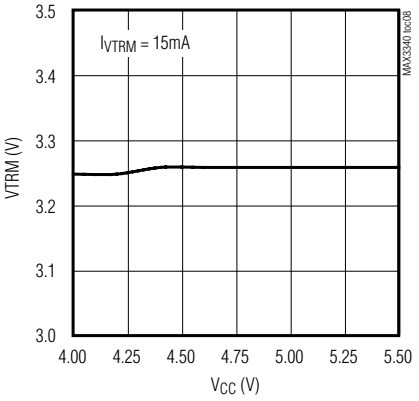
A: VP, 2V/div
B: VM, 2V/div
C: OE/ENUMERATE, 5V/div

OE/ENUMERATE, VP, VM TIMING

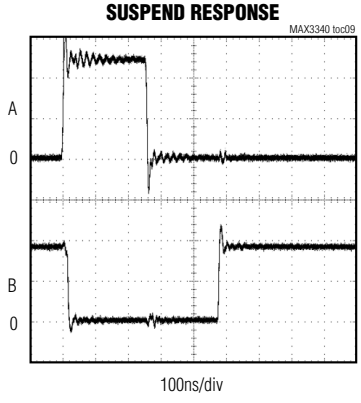


A: VP, 2V/div
B: VM, 2V/div
C: OE/ENUMERATE, 5V/div

VTRM vs. V_{CC}



SUSPEND RESPONSE

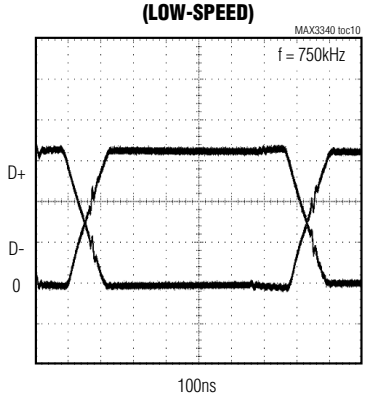


A: SUSP, 2V/div
B: RCV, 2V/div

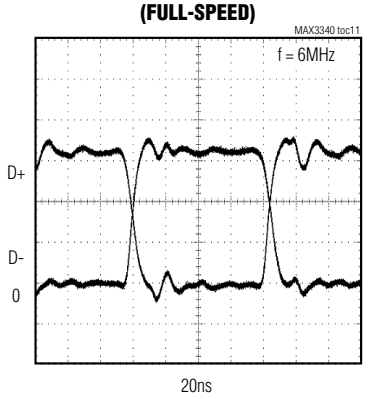
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_L = +3.3V T_A = +25°C, unless otherwise noted.)

RISE- AND FALL-TIME MATCHING (LOW-SPEED)



RISE- AND FALL-TIME MATCHING (FULL-SPEED)



Pin Description

PIN		NAME	FUNCTION
TSSOP	CSP		
1	D2	RCV	Receiver Output. Single-ended CMOS output. RCV responds to the differential input on D+ and D-. (See Table 1)
2	D1	VP	System-Side Data Input/Output. Drive OE/ENUMERATE high to make VP a receiver output. Drive OE/ENUMERATE low to make VP a driver input. VP and VM work together, see Table 1 for details.
3	C2	MODE	Mode Control Input. Selects single-ended (Mode Zero) or differential (Mode One) input for the system side when converting logic level signals to USB level signals. MODE is pulled to V_{CC} with an internal 10µA current. If MODE is forced high or left floating, Mode One is selected. If MODE is forced low, Mode Zero is selected. Refer to Table 1.
4	C1	VM	System-Side Data Input/Output. Drive OE/ENUMERATE high to make VM a receiver output. Drive OE/ENUMERATE low to make VM a driver input. VM and VP work together, see Table 1 for details.
5	B1	OE/ ENUMERATE	Output Enable. Drive OE/ENUMERATE high to enable VP/VM outputs. Float to disconnect R_{PULLUP}.
6	A1	RENB	Receive Enable Input. When RENB is forced high, RCV and VM/VP respond to signals at D+/D-. When RENB is forced low, only RCV responds to signals at D+/D-, VM/VP are high impedance. Normally connected to OE/ENUMERATE.
7	B2	SUSP	Suspend Input. Drive SUSP low for normal operation. Force SUSP high for low-power state. In low-power state RCV is low, D+/D- are high impedance if OE/ENUMERATE is floating, and VP/VM are active outputs.

±15kV ESD-Protected USB Level Translator in UCSP

Pin Description (continued)

PIN		NAME	FUNCTION
TSSOP	CSP		
8	A2	SPEED	USB Transmission Speed Select Input. If SPEED is forced high, full-speed (12Mbps) is selected and the internal 1.5kΩ pullup resistor is connected to D+. If SPEED is forced low, low-speed (1.5Mbps) is selected and the internal 1.5kΩ pullup resistor is connected to D-.
9	A3	V_{CC}	USB-Side Power-Supply Input. Connect V_{CC} to the incoming USB power supply. Bypass V_{CC} to GND with 0.1µF ceramic and 10µF electrolytic capacitors.
10	A4	GND	Ground
—	B3, C3	N.C.	No Connect. There are no solder bumps at these locations.
11	B4	D-	USB Differential Data Input/Output. Connect to the USB's D- signal through a 24.3Ω ±1% resistor.
12	C4	D+	USB Differential Data Input/Output. Connect to the USB's D+ signal through a 24.3Ω ±1% resistor.
13	D4	VTRM	Regulated Output Voltage. 3.3V output derived from the V_{CC} input. Bypass VTRM to GND with a 1µF (or more) low-ESR capacitor such as ceramic or plastic film types. Up to 15mA may be drawn from VTRM for powering external components.
14	D3	V_L	System-Side Power-Supply Input. Connect to the system's logic-level power supply, 1.8V to 3.6V.

Detailed Description

The MAX3340E is a bidirectional level translator that converts single-ended or differential logic level signals to differential USB signals, and converts differential USB signals to single-ended or differential logic level signals. It includes an internal 1.5kΩ pullup resistor that may be connected to either D+ to D- for full-speed or low-speed operation (Functional Diagram). The MAX3340E can be energized without concern about power-supply sequencing. Additionally, the USB I/O pins, D+ and D-, are ESD protected to ±15kV. The MAX3340E can get its USB-side power, V_{CC}, directly from the USB connection, and can operate with system-side power, V_L, down to 1.8V and still meet the USB physical layer specifications. MAX3340E supports both full-speed (12Mbps) and low-speed (1.5Mbps), USB specification 1.1 operation.

The MAX3340E has a unique re-enumerate feature which works when power is on. Floating OE/ENUMERATE will disconnect the internal 1.5kΩ termination resistor from both D+ and D-, re-enumerating the USB. This is useful if changes in communication protocol are required while power is applied, and while the USB cable is connected.

ESD protection

To protect the MAX3340E against ESD, D+ and D- have extra protection against static electricity to protect the device up to ±15kV. The ESD structures withstand high ESD in all states; normal operation, suspend, and powered down. In order for the 15kV ESD structures to work correctly a 1µF or greater capacitor must be connected from VTRM to GND.

ESD protection can be tested in various ways; the D+ and D- input/output pins are characterized for protection to the following limits:

1) ±15kV using the Human Body Model.

2) ±5kV using the Contact Discharge method specified in IEC 1000-4-2.

3) ±9kV using the IEC 1000-4-2 Air-Gap method.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 5a shows the Human Body Model, and Figure 5b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX3340E helps you design equipment that meets Level 2 of IEC 1000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 1000-4-2 is a higher peak current in IEC 1000-4-2, because series resistance is lower in the IEC 1000-4-2 model. Hence, the ESD withstand voltage measured to IEC 1000-4-2 is generally lower than that measured using the Human Body Model. Figure 6a shows the IEC 1000-4-2 model.

The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing, not just RS-232 inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

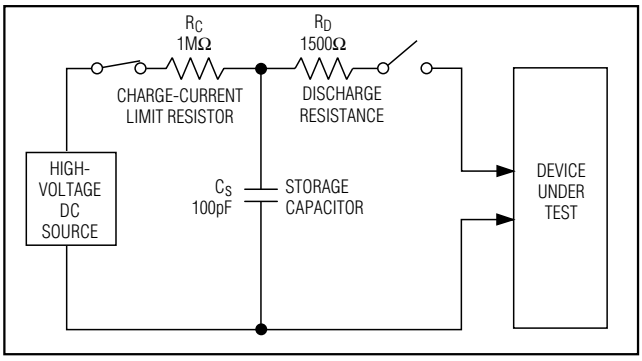


Figure 5a. Human Body ESD Test Models

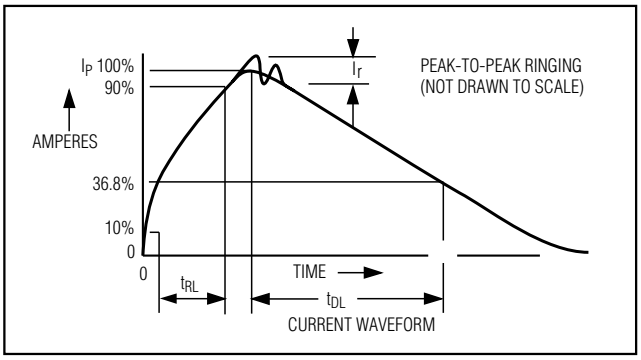


Figure 5b. Human Body Model Current Waveform

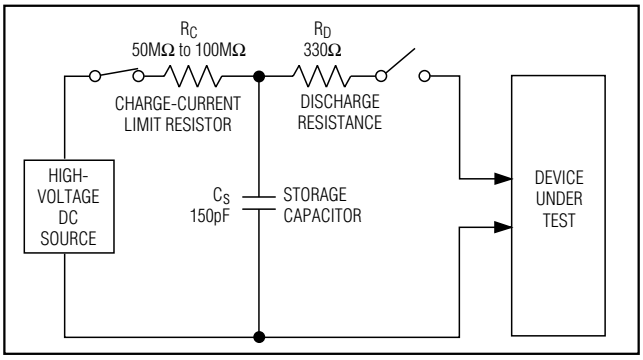


Figure 6a. IEC 1000-4-2 ESD Test Model

±15kV ESD-Protected USB Level Translator in UCSP

Applications Information

Device Control

OE/ENUMERATE

OE/ENUMERATE is a dual-function control input. It controls the direction of communication, and can also be used to re-establish a device on the USB. With OE/ENUMERATE low, the MAX3340E transfers data from the system side to the USB side. With OE/ENUMERATE high, the MAX3340E transfers data from the USB side to the system side. If OE/ENUMERATE is floating for more than 200ns (typ), the internal 1.5kΩ resistor is disconnected from both D+ and D-, signaling the USB to re-enumerate the device. This is useful if changes in the USB transmission protocol are required while operating.

MODE

MODE is a control input that selects whether differential or single-ended logic signals are recognized by the system side of the MAX3340E (Table 1). MODE has an internal pullup to V_{CC}.

If MODE is left floating or forced high, differential input is selected. With differential input selected, outputs D+ and D- follow the differential inputs at VP and VM. If VP and VM are both forced low, an SE0 condition is forced on the USB.

Drive MODE and VM low for single-ended input mode. With single-ended input selected, the differential signal on D+ and D- is controlled by VP. If VM is high when MODE is low, D- and D+ are both low forcing an SEO condition.

RENB

Drive RENB (receive enable) high to enable VP and VM as receive outputs. When RENB is forced low VP and VM are high impedance. RCV is unaffected by RENB. Connect RENB to OE/ENUMERATE for normal operation.

SUSP

SUSP, or suspend, is a control input. When SUSP is forced high the MAX3340E enters low-power state. In this state the quiescent supply current into V_{CC} is less than 200µA if OE/ENUMERATE is floating and D+ and D- are static. In this mode RCV is forced low, and D+ and D- are high-impedance inputs (Table 1d).

In suspend mode, VP and VM remain active as receive outputs, VTRM stays on, and the MAX3340E continues to receive data from the USB.

SPEED

SPEED is a control input that selects between low-speed (1.5Mbps) and full-speed (12Mbps) USB transmission. Internally, it selects whether the 1.5kΩ pullup resistor is connected to D+ (full-speed) or D- (low-speed) (Functional Diagram). Force SPEED high to select full-speed, or force SPEED low to select low-speed.

VTRM

VTRM is the 3.3V output of the internal linear voltage regulator. The regulator is used to power the internal portions of the USB side of the MAX3340E. VTRM can be used to power external devices with the ability to source up to 15mA. The VTRM regulator's supply input is V_{CC}. Connect a 1.0µF (or greater) ceramic or plastic capacitor from VTRM to GND, as close to VTRM as possible.

D+ and D-

D+ and D- are the transmitter I/O connections, and are ESD protected to ±15kV using the Human Body Model, making the MAX3340E ideal for applications where a robust transmitter is required.

V_{CC}

In most applications V_{CC} is derived from the USB +5V output. If supplying V_{CC} with an alternative power supply, the input range is 4.0V to 5.5V. Bypass V_{CC} to GND with a 10µF and a 0.1µF capacitor. Place the 0.1µF capacitor closest to the MAX3340E.

External Components

External Resistors

Two external resistors are required for USB connection, each of them 24.3Ω, ±1%, 1/8W (or greater). Place one resistor in series between D+ of the MAX3340E and D+ of the USB connector. Place the other resistor in series between D- of the MAX3340E and D- of the USB connector. The *Typical Operating Circuit* shows these connections.

External Capacitors

Four external capacitors are recommended for proper operation. Use a 0.1µF ceramic for decoupling V_L, a 0.1µF ceramic and a 10µF electrolytic for decoupling V_{CC}, and a 1.0µF (or greater) ceramic or plastic filter capacitor on VTRM. Return all capacitors to GND.

Powering External Components with VTRM

VTRM is the output of the internal 3.3V linear regulator, and requires an external ceramic capacitor, as detailed in the *VTRM* section above. VTRM can source up to 15mA at 3.3V for powering external devices. Note that the source of power for the internal regulator is usually

the USB provided 5V; if so, any devices powered from VTRM will lose power if the USB connection is broken. If D+ or D- is shorted to +5V (a fault condition), VTRM follows a diode drop below. If any external circuitry is powered from VTRM, it is recommended that the circuitry be either +5V tolerant, or that an external protection zener is used.

Data Transfer

Receiving Data from the USB

Data received from the USB are output to VP/VM in either of two ways, differentially or single-ended. To receive data from the USB, force MODE high or let it float, force OE/ENUMERATE and RENB high, and force SUSP low. Differential data arriving at D+/D- will appear as differential logic signals at VP/VM, and as a single-ended logic signal at RCV. If both D+ and D- are low, then VP and VM are low, signaling an SE0 condition on the bus; RCV is undefined. See Table 1.

Transmitting Data to the USB

The MAX3340E outputs data to the USB differentially on D+ and D-. The logic driving signals may be either differential or single-ended. For sending differential logic, force MODE high or let it float, force OE/ENUMERATE, RENB and SUSP low, and apply data to VP and VM. If sending single-ended logic, force MODE low, force RENB, SUSP, OE/ENUMERATE, and VM low, and apply data to VP. With VP low, D+ is low and D- high, resulting in a Logic 0. With VP high, D+ is high and D- low resulting in a Logic 1 state. See Table 1.

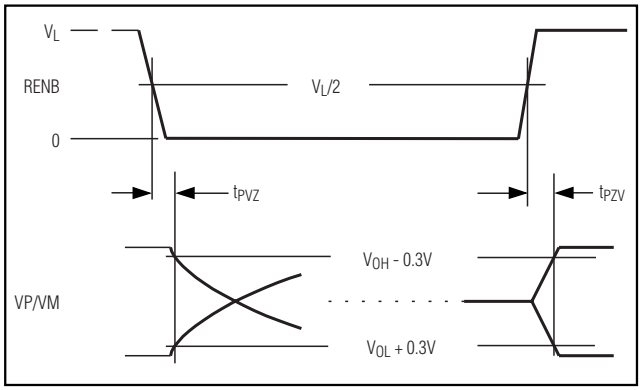


Figure 1a. Enable and Disable Timing, Receiver

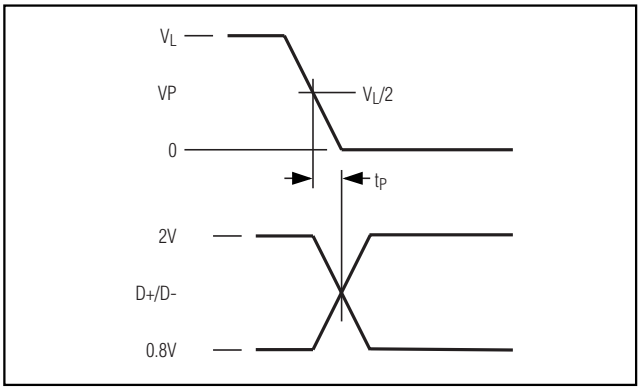


Figure 2. Mode 0 Timing

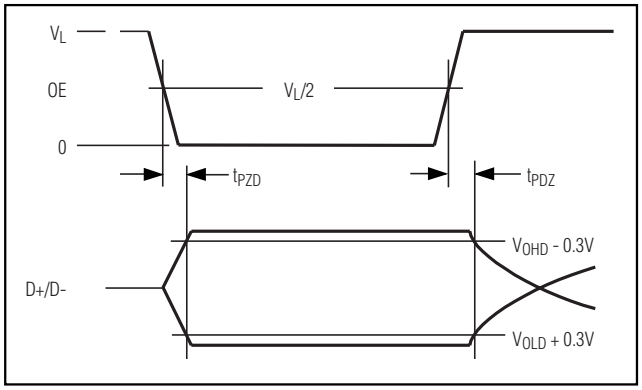


Figure 1b. Enable and Disable Timing, Transmitter

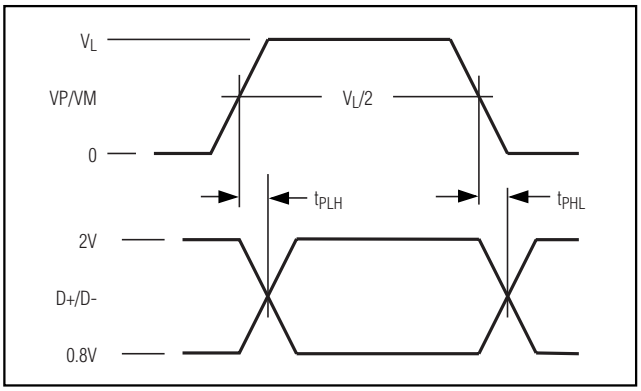


Figure 3. Mode 1 Timing

±15kV ESD-Protected USB Level Translator in UCSP

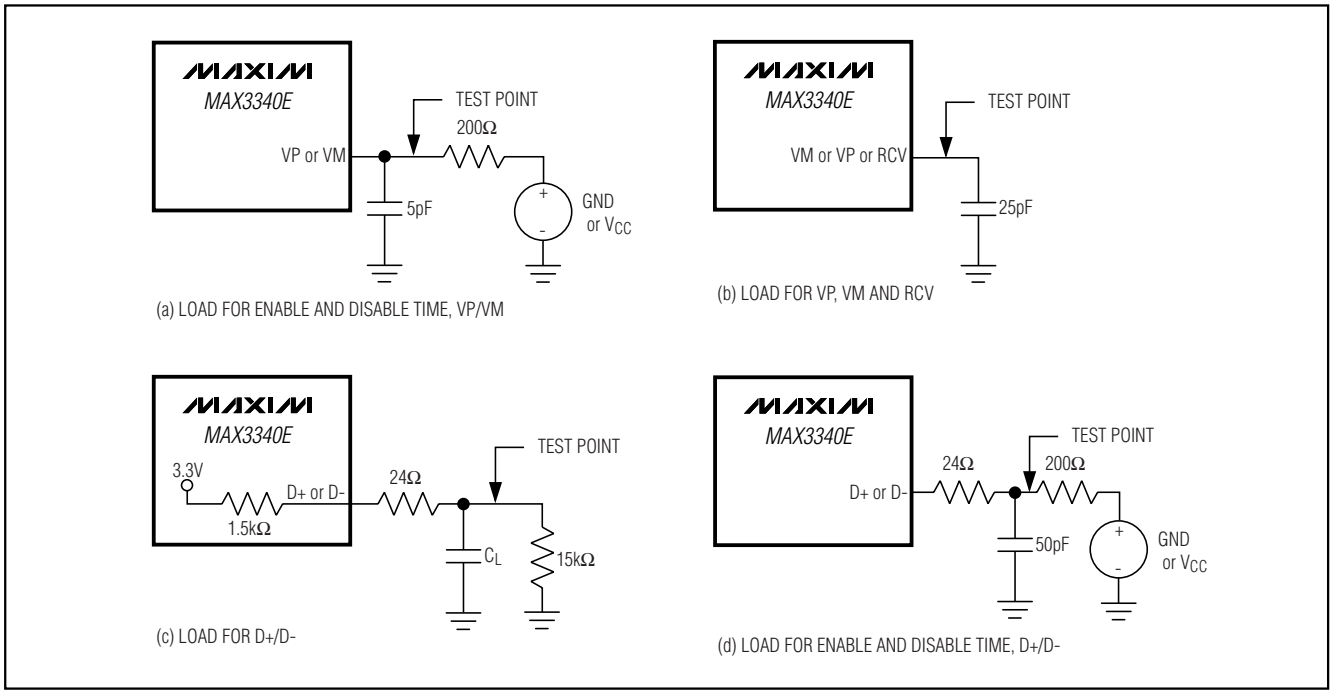


Figure 4. Test Circuits

Table 1a. Truth Table Transmit (MODE = 0)

OE/ENUMERATE = 0 (TRANSMIT), RENB = 0					
INPUT		OUTPUT			RESULT
VP	VM	D+	D-	RCV	
0	0	0	1	0	Logic 0
0	1	0	0	X	SEO
1	0	1	0	1	Logic 1
1	1	0	0	X	SEO

Table 1b. Truth Table Transmit (MODE = 1)

OE/ENUMERATE = 0 (TRANSMIT), RENB = 0					
INPUT		OUTPUT			RESULT
VP	VM	D+	D-	RCV	
0	0	0	0	X	SEO
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined

Table 1c. Truth Table Receive

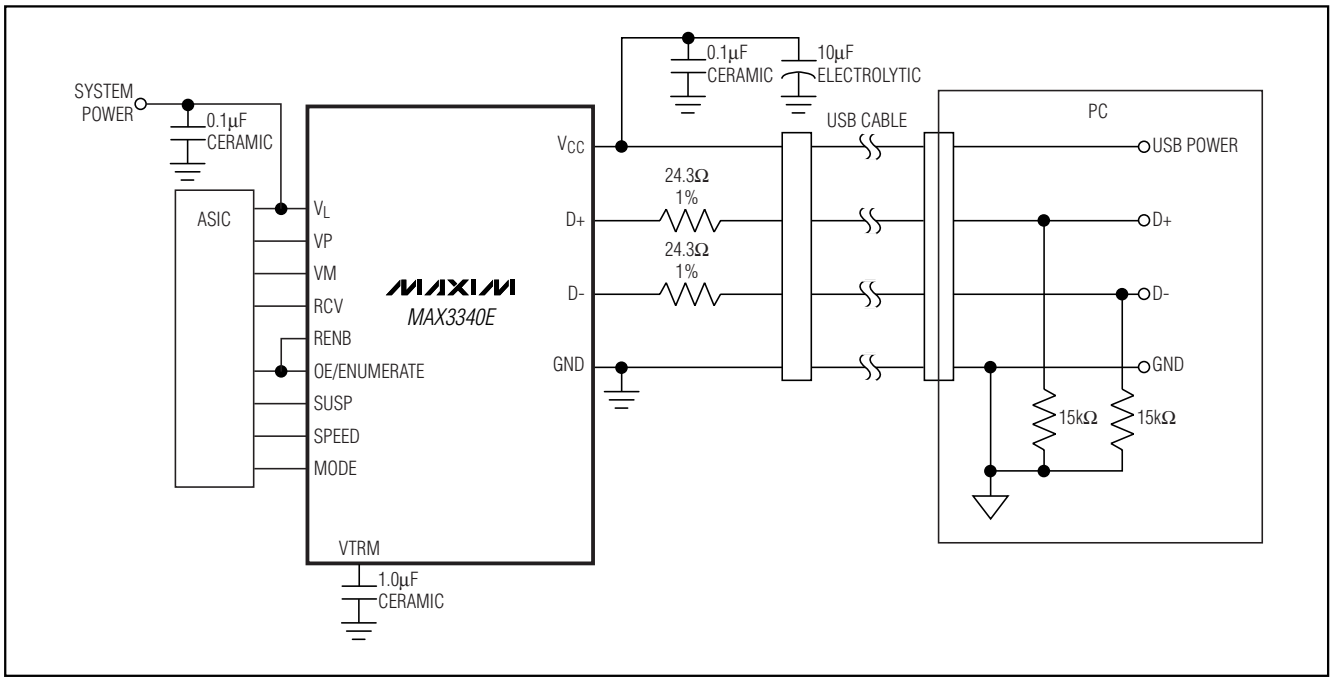
OE/ENUMERATE = 0 (RECEIVE), RENB = 1					
INPUT		OUTPUT			RESULT
D+	D-	VP	VM	RCV	
0	0	0	0	X	SEO
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined

Table 1d. Function Select

SUSP	OE/ENUMERATE	RENB	D+/D-	RCV	VP/VM	FUNCTION
0	0	0	Driving	Active	High-Z	Normal driving (differential receiver active)
0	0	1	Driving	Active	Active	Conflict state: not permitted
0	1	0	High-Z	Active	High-Z	R_{PULLUP} connected
0	1	1	High-Z	Active	Active	Receiving
1	0 or 1	0 or 1	High-Z	0	Active	Low-power state
0	Float	0 or 1	High-Z	Active	High-Z	R_{PULLUP} disconnected
1	Float	0 or 1	High-Z	0	Active	R_{PULLUP} disconnected

±15kV ESD-Protected USB Level Translator in UCSP

Typical Operating Circuit



UCSP Reliability

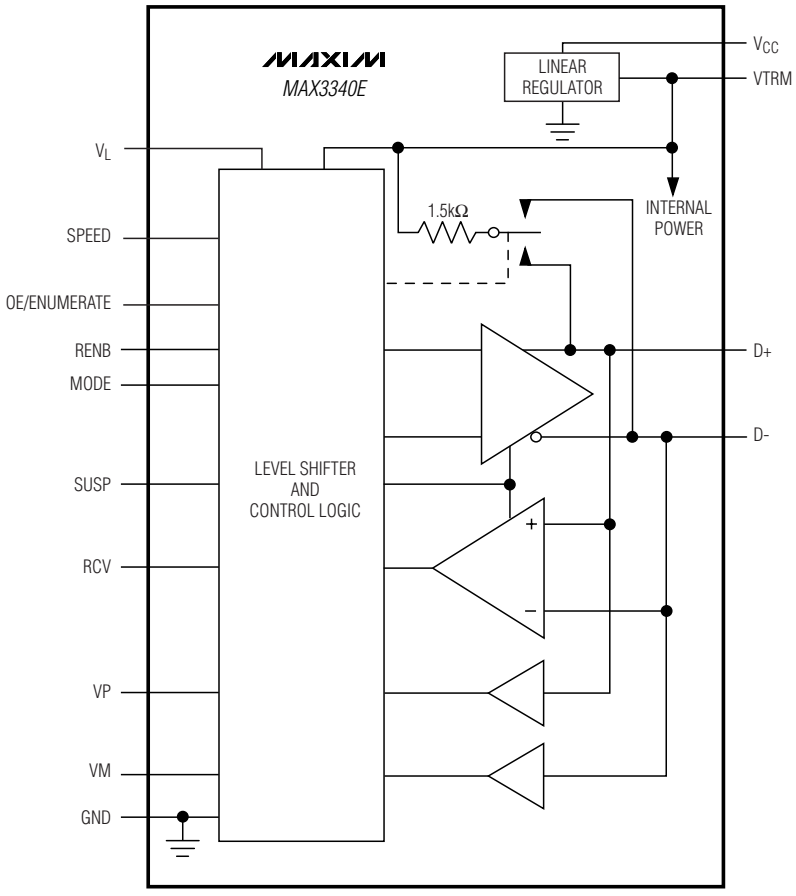
The UCSP represents a unique packaging form factor that may not perform equally to a packaged product through traditional mechanical reliability tests. CSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a CSP package. Performance through Operating Life Test and Moisture Resistance remains uncompromised as it is primarily determined by the wafer-fabrication process.

Mechanical stress performance is a greater consideration for a CSP package. CSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged product lead frame. Solder joint contact integrity must be considered. Table 2 shows the testing done to characterize the CSP reliability performance. In conclusion, the UCSP is capable of performing reliably through environmental stresses as indicated by the results in the table. Additional usage data and recommendations are detailed in the UCSP application note, which can be found on Maxim's website at www.maxim-ic.com.

Table 2. Reliability Test Data

TEST	CONDITIONS	DURATION	NO. OF FAILURES PER SAMPLE SIZE
Temperature Cycle	-35°C to +85°C, -40°C to +100°C	150 cycles, 900 cycles	0/10, 0/200
Operating Life	T_A = +70°C	240hr	0/10
Moisture Resistance	+20°C to +60°C, 90% RH	240hr	0/10
Low-Temperature Storage	-20°C	240hr	0/10
Low-Temperature Operational	-10°C	24hr	0/10
Solderability	8hr steam age	—	0/15
ESD	±2000V, Human Body Model	—	0/5
High-Temperature Operating Life	T_J = +150°C	168hr	0/45

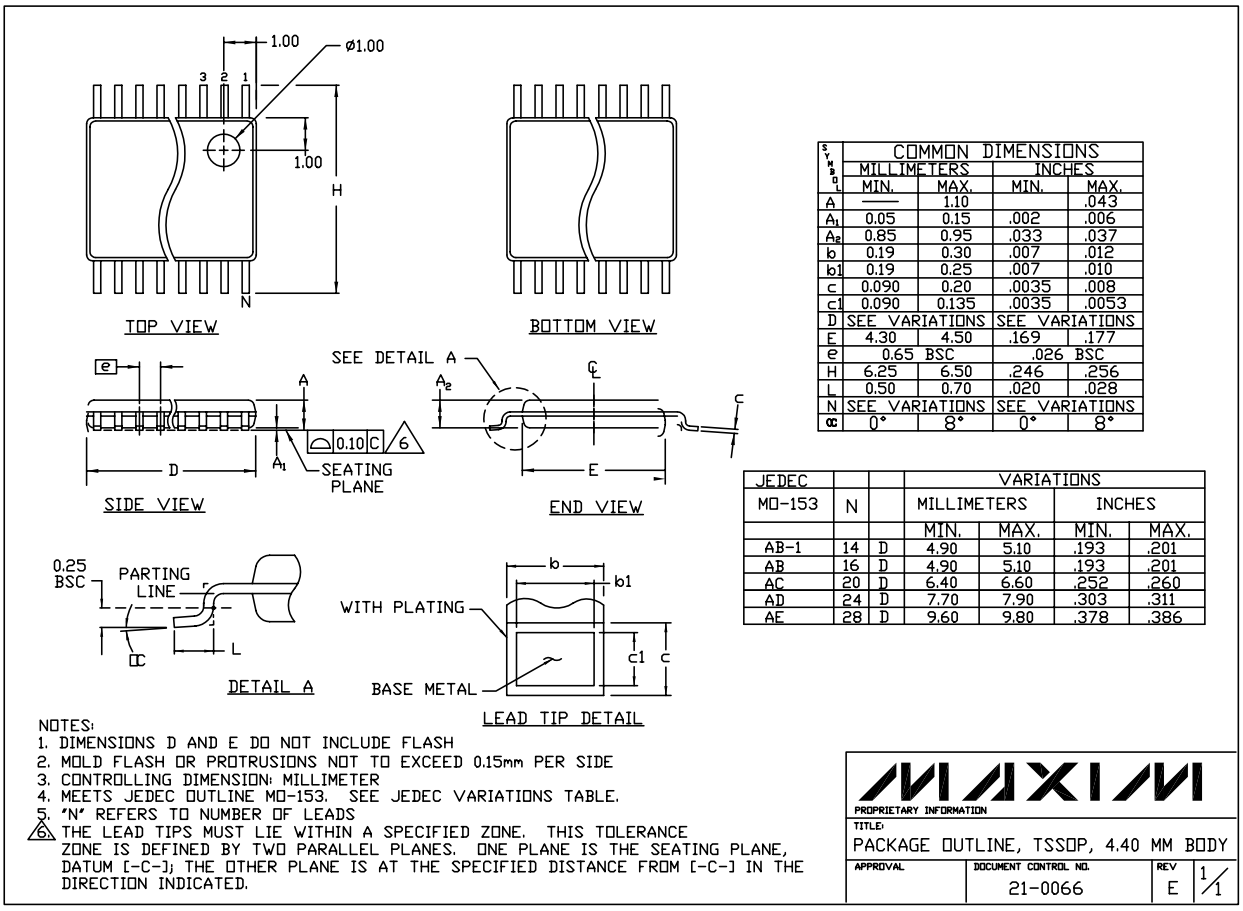
Functional Diagram



±15kV ESD-Protected USB Level Translator in UCSP

Package Information

TSSOP,NO PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

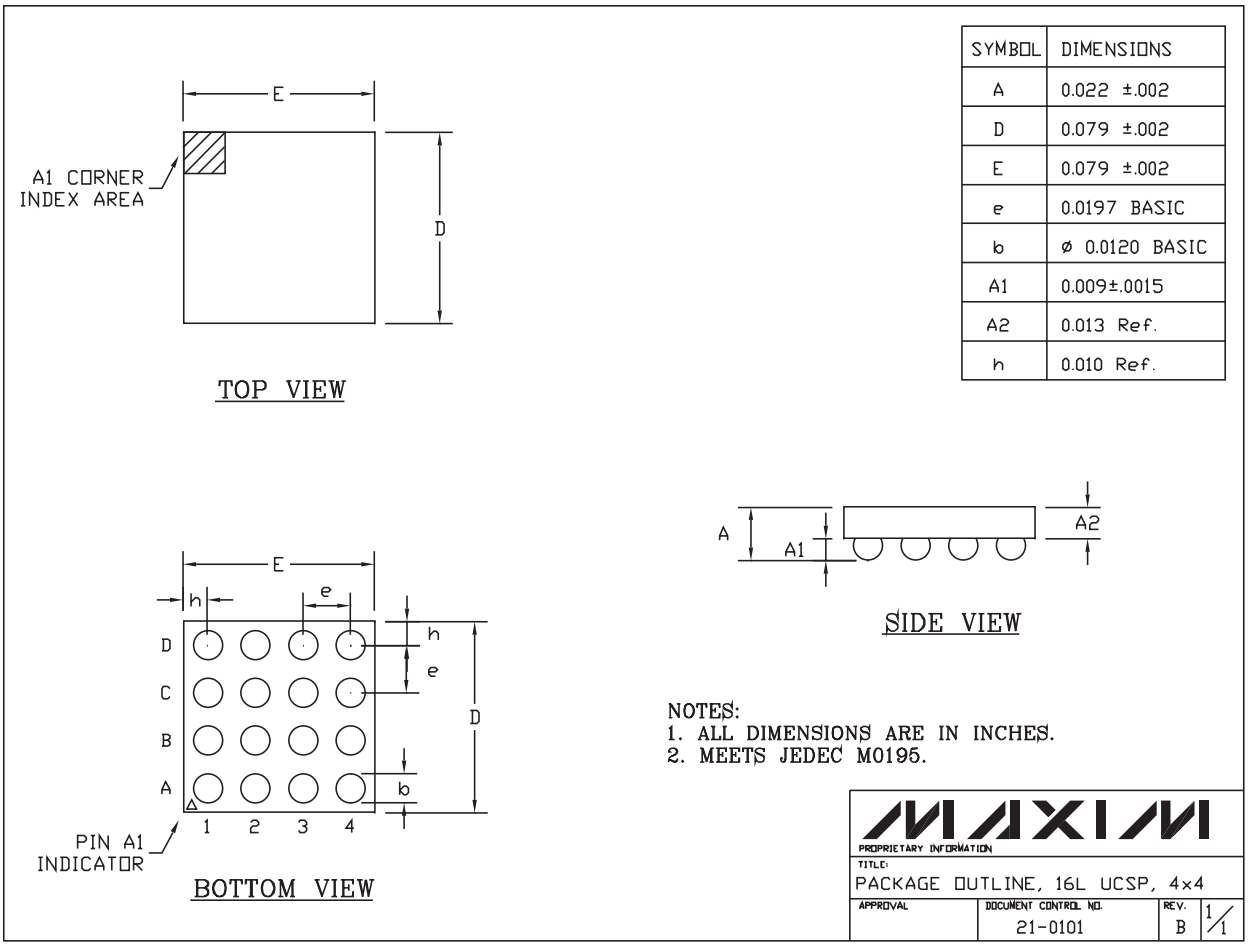
NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	E	1/1

Package Information (continued)



SYMBOL	DIMENSIONS
A	0.022 ±.002
D	0.079 ±.002
E	0.079 ±.002
e	0.0197 BASIC
b	ø 0.0120 BASIC
A1	0.009±.0015
A2	0.013 Ref.
h	0.010 Ref.