

# NLSV4T244E

## 4-Bit Dual-Supply Non-Inverting Level Translator

The NLSV4T244E is a 4-bit configurable dual-supply voltage level translator. The input  $A_n$  and output  $B_n$  ports are designed to track two different power supply rails,  $V_{CCA}$  and  $V_{CCB}$  respectively. Both supply rails are configurable from 0.9 V to 4.5 V allowing universal low-voltage translation from the input  $A_n$  to the output  $B_n$  port.

### Features

- Wide  $V_{CCA}$  and  $V_{CCB}$  Operating Range: 0.9 V to 4.5 V
- High-Speed w/ Balanced Propagation Delay
- Inputs and Outputs have OVT Protection to 4.5 V
- Non-preferential  $V_{CCA}$  and  $V_{CCB}$  Sequencing
- Outputs at 3-State until Active  $V_{CC}$  is Reached
- Power-Off Protection
- Outputs Switch to 3-State with  $V_{CCB}$  at GND
- Data Rate > 200 Mbps @  $V_{CCA} = 1.8$  V,  $V_{CCB} = 3.3$  V,  $R_L = 2$  k $\Omega$ ,  $C_L = 15$  pF
- Ultra-Small Packaging: 1.7 mm x 2.0 mm UQFN12
- These are Pb-Free Devices

### Typical Applications

- Mobile Phones, PDAs, Other Portable Devices

### Important Information

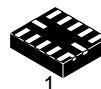
- ESD Protection for All Pins:  
 HBM (Human Body Model) > 2000 V  
 MM (Machine Model) > 400 V



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### MARKING DIAGRAMS

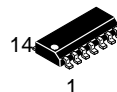


UQFN12  
MU SUFFIX  
CASE 523AE

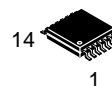
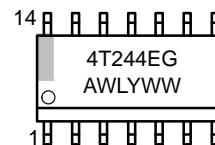


AF = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

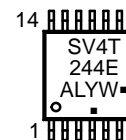
(Note: Microdot may be in either location)



SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ▪ = Pb-Free Package  
(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NLSV4T244EMUTAG	UQFN12 (Pb-Free)	3000/Tape & Reel
NLSV4T244EDR2G	SO-14 (Pb-Free)	2500/Tape & Reel
NLSV4T244EDTR2G	TSSOP14 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NLSV4T244E

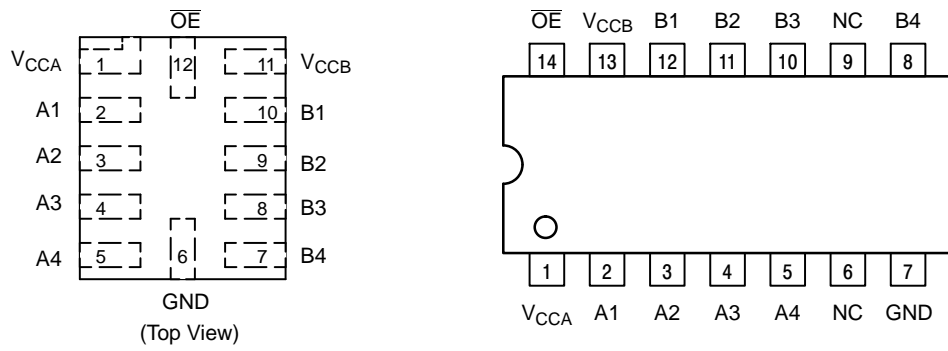


Figure 1. Pin Assignments

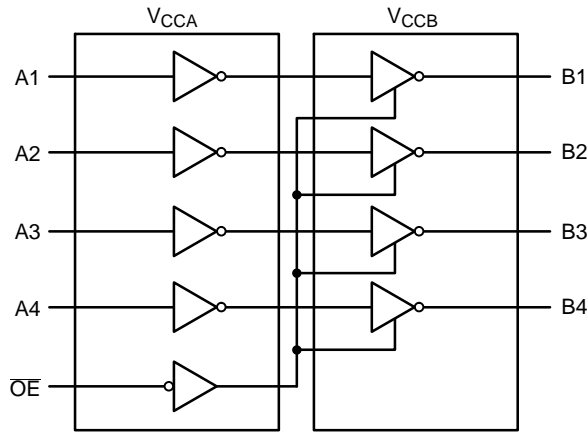


Figure 2. Logic Diagram

## PIN ASSIGNMENT

PIN	FUNCTION
V <sub>CCA</sub>	Input Port DC Power Supply
V <sub>CCB</sub>	Output Port DC Power Supply
GND	Ground
A <sub>n</sub>	Input Port
B <sub>n</sub>	Output Port
OE	Output Enable

## TRUTH TABLE

Inputs		Outputs
OE	A <sub>n</sub>	B <sub>n</sub>
L	L	L
L	H	H
H	X	3-State

# NLSV4T244E

## MAXIMUM RATINGS

Symbol	Rating	Condition	Value	Unit	
$V_{CCA}, V_{CCB}$	DC Supply Voltage		-0.5 to +5.5	V	
$V_I$	DC Input Voltage	$A_n$	-0.5 to +5.5	V	
$V_C$	Control Input	$\overline{OE}$	-0.5 to +5.5	V	
$V_O$	DC Output Voltage (Power Down)	$B_n$	$V_{CCA} = V_{CCB} = 0$	-0.5 to +5.5	V
	(Active Mode)	$B_n$		-0.5 to +5.5	V
	(Tri-State Mode)	$B_n$		-0.5 to +5.5	V
$I_{IK}$	DC Input Diode Current	$V_I < GND$	-20	mA	
$I_{OK}$	DC Output Diode Current	$V_O < GND$	-50	mA	
$I_O$	DC Output Source/Sink Current		$\pm 50$	mA	
$I_{CCA}, I_{CCB}$	DC Supply Current Per Supply Pin		$\pm 100$	mA	
$I_{GND}$	DC Ground Current per Ground Pin		$\pm 100$	mA	
$T_{STG}$	Storage Temperature Range		-65 to +150	$^{\circ}C$	
$T_J$	Junction Temperature		+125	$^{\circ}C$	
$\theta_{JA}$	Junction-to-Ambient Thermal Resistance		53	$^{\circ}C/W$	
$\Psi_{JC(top)}$	Junction-to-Case (Top) Thermal Resistance		10	$^{\circ}C/W$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CCA}, V_{CCB}$	Positive DC Supply Voltage	0.9	4.5	V	
$V_I$	Bus Input Voltage	GND	4.5	V	
$V_C$	Control Input	$\overline{OE}$	4.5	V	
$V_{IO}$	Bus Output Voltage (Power Down Mode)	$B_n$	GND	4.5	V
	(Active Mode)	$B_n$	GND	$V_{CCB}$	V
	(Tri-State Mode)	$B_n$	GND	4.5	V
$T_A$	Operating Temperature Range	-40	+85	$^{\circ}C$	
$\Delta t / \Delta V$	Input Transition Rise or Rate $V_I$ , from 30% to 70% of $V_{CC}$ ; $V_{CC} = 3.3 V \pm 0.3 V$	0	10	nS	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# NLSV4T244E

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	-40°C to +85°C		Unit
					Min	Max	
V <sub>IH</sub>	Input HIGH Voltage (An, OE)		3.6 – 4.5	0.9 – 4.5	2.2	–	V
			2.7 – 3.6		2.0	–	
			2.3 – 2.7		1.6	–	
			1.4 – 2.3		0.65 * V <sub>CCA</sub>	–	
			0.9 – 1.4		0.9 * V <sub>CCA</sub>	–	
V <sub>IL</sub>	Input LOW Voltage (An, OE)		3.6 – 4.5	0.9 – 4.5	–	0.8	V
			2.7 – 3.6		–	0.8	
			2.3 – 2.7		–	0.7	
			1.4 – 2.3		–	0.35 * V <sub>CCA</sub>	
			0.9 – 1.4		–	0.1 * V <sub>CCA</sub>	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = –100 μA; V <sub>I</sub> = V <sub>IH</sub>	0.9 – 4.5	0.9 – 4.5	V <sub>CCB</sub> – 0.2	–	V
		I <sub>OH</sub> = –0.5 mA; V <sub>I</sub> = V <sub>IH</sub>	0.9	0.9	0.75 * V <sub>CCB</sub>	–	
		I <sub>OH</sub> = –2 mA; V <sub>I</sub> = V <sub>IH</sub>	1.4	1.4	1.05	–	
		I <sub>OH</sub> = –6 mA; V <sub>I</sub> = V <sub>IH</sub>	1.65	1.65	1.25	–	
			2.3	2.3	2.0	–	
		I <sub>OH</sub> = –12 mA; V <sub>I</sub> = V <sub>IH</sub>	2.3	2.3	1.8	–	
			2.7	2.7	2.2	–	
		I <sub>OH</sub> = –18 mA; V <sub>I</sub> = V <sub>IH</sub>	2.3	2.3	1.7	–	
			3.0	3.0	2.4	–	
I <sub>OH</sub> = –24 mA; V <sub>I</sub> = V <sub>IH</sub>	3.0	3.0	2.2	–			
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 100 μA; V <sub>I</sub> = V <sub>IL</sub>	0.9 – 4.5	0.9 – 4.5	–	0.2	V
		I <sub>OL</sub> = 0.5 mA; V <sub>I</sub> = V <sub>IH</sub>	1.1	1.1	–	0.3	
		I <sub>OL</sub> = 2 mA; V <sub>I</sub> = V <sub>IH</sub>	1.4	1.4	–	0.35	
		I <sub>OL</sub> = 6 mA; V <sub>I</sub> = V <sub>IL</sub>	1.65	1.65	–	0.3	
			2.3	2.3	–	0.4	
		I <sub>OL</sub> = 12 mA; V <sub>I</sub> = V <sub>IL</sub>	2.7	2.7	–	0.4	
			2.3	2.3	–	0.6	
		I <sub>OL</sub> = 18 mA; V <sub>I</sub> = V <sub>IL</sub>	3.0	3.0	–	0.45	
I <sub>OL</sub> = 24 mA; V <sub>I</sub> = V <sub>IL</sub>	3.0	3.0	–	0.6			
I <sub>I</sub>	Input Leakage Current	V <sub>I</sub> = V <sub>CCA</sub> or GND	0.9 – 4.5	0.9 – 4.5	–1.0	1.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	OE = 0 V	0 0.9 – 4.5	0.9 – 4.5 0	–1.0 –1.0	1.0 1.0	μA
I <sub>CCA</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CCA</sub> or GND; I <sub>O</sub> = 0, V <sub>CCA</sub> = V <sub>CCB</sub>	0.9 – 4.5	0.9 – 4.5	–	2.0	μA
I <sub>CCB</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CCA</sub> or GND; I <sub>O</sub> = 0, V <sub>CCA</sub> = V <sub>CCB</sub>	0.9 – 4.5	0.9 – 4.5	–	2.0	μA
I <sub>CCA</sub> + I <sub>CCB</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CCA</sub> or GND; I <sub>O</sub> = 0, V <sub>CCA</sub> = V <sub>CCB</sub>	0.9 – 4.5	0.9 – 4.5	–	4.0	μA
ΔI <sub>CCA</sub>	Increase in I <sub>CC</sub> per Input Voltage, Other Inputs at V <sub>CCA</sub> or GND	V <sub>I</sub> = V <sub>CCA</sub> – 0.6 V; V <sub>I</sub> = V <sub>CCA</sub> or GND	4.5	4.5	–	10	μA
			3.6	3.6		5.0	
ΔI <sub>CCB</sub>	Increase in I <sub>CC</sub> per Input Voltage, Other Inputs at V <sub>CCA</sub> or GND	V <sub>I</sub> = V <sub>CCA</sub> – 0.6 V; V <sub>I</sub> = V <sub>CCA</sub> or GND	4.5	4.5	–	10	μA
			3.6	3.6		5.0	
I <sub>OZ</sub>	I/O Tri-State Output Leakage Current	T <sub>A</sub> = 25°C, OE = 0V <sub>CCA</sub> , V <sub>O</sub> = 0 to V <sub>CCB</sub> + 0.5 V	0.9 – 4.5	0.9 – 4.5	–	1.0	μA
		T <sub>A</sub> = 25°C, OE = 0V <sub>CCA</sub> , V <sub>O</sub> = 0 to 4.5 V			–	75	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# NLSV4T244E

## TOTAL STATIC POWER CONSUMPTION ( $I_{CCA} + I_{CCB}$ )

$V_{CCA}$ (V)	-40°C to +85°C										Unit
	$V_{CCB}$ (V)										
	4.5		3.3		2.8		1.8		0.9		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
4.5		2		2		2		2		< 1.5	$\mu$ A
3.3		2		2		2		2		< 1.5	$\mu$ A
2.8		< 2		< 1		< 1		< 0.5		< 0.5	$\mu$ A
1.8		< 1		< 1		< 0.5		< 0.5		< 0.5	$\mu$ A
0.9		< 0.5		< 0.5		< 0.5		< 0.5		< 0.5	$\mu$ A

NOTE: Connect ground before applying supply voltage  $V_{CCA}$  or  $V_{CCB}$ . This device is designed with the feature that the power-up sequence of  $V_{CCA}$  and  $V_{CCB}$  will not damage the IC.

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	$V_{CCA}$ (V)	-40°C to +85°C										Unit
			$V_{CCB}$ (V)										
			4.5		3.3		2.8		1.8		1.5		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$ (Note 1)	Propagation Delay, $A_n$ to $B_n$	4.5		3.0		3.2		3.4		3.7		4.0	nS
		3.6		3.3		3.5		3.7		4.0		4.3	
		2.8		3.5		3.7		3.9		4.2		4.5	
		1.8		3.8		4.0		4.2		4.5		4.8	
		1.5		4.1		4.3		4.5		4.8		5.0	
$t_{PZH}$ , $t_{PZL}$ (Note 1)	Output Enable, $\overline{OE}$ to $B_n$	4.5		4.4		4.8		5.2		5.7		6.2	nS
		3.3		4.7		5.1		5.5		6.0		6.5	
		2.8		4.9		5.3		5.7		6.2		6.7	
		1.8		5.2		5.6		6.0		6.5		7.0	
		1.5		5.5		5.9		6.3		6.8		7.3	
$t_{PHZ}$ , $t_{PLZ}$ (Note 1)	Output Disable, $\overline{OE}$ to $B_n$	4.5		4.4		4.8		5.2		5.7		6.2	nS
		3.3		4.7		5.1		5.5		6.0		6.5	
		2.8		4.9		5.3		5.7		6.2		6.7	
		1.8		5.2		5.6		6.0		6.5		7.0	
		1.5		5.5		5.9		6.3		6.8		7.3	
$t_{OSHL}$ , $t_{OSLH}$ (Note 1)	Output to Output Skew, Data to Output	4.1		0.15		0.15		0.15		0.15		0.15	nS
		3.6		0.15		0.15		0.15		0.15		0.15	
		2.8		0.15		0.15		0.15		0.15		0.15	
		1.8		0.15		0.15		0.15		0.15		0.15	
		1.2		0.15		0.15		0.15		0.15		0.15	

1. Propagation delays defined per Figures 3 and 4.

## CAPACITANCE

Symbol	Parameter	Test Conditions	Typ (Note 2)	Unit
$C_{IN}$	Control Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$	3.5	pF
$C_{I/O}$	I/O Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$	5.0	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA}$ , $f = 10$ MHz	20	pF

2. Typical values are at  $T_A = +25^\circ\text{C}$ .

3.  $C_{PD}$  is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from:  
 $I_{CC(\text{operating})} \cong C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$  where  $I_{CC} = I_{CCA} + I_{CCB}$  and  $N_{SW}$  = total number of outputs switching.

# NLSV4T244E

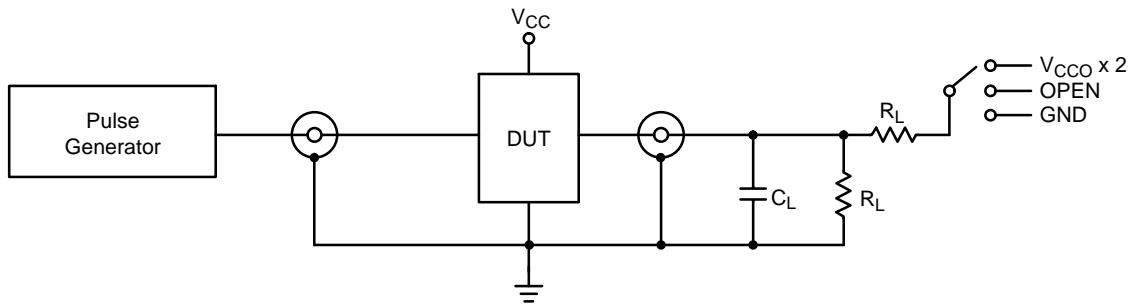
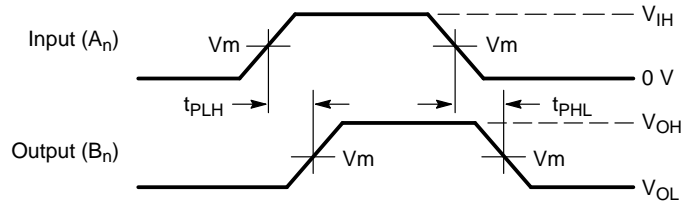


Figure 3. AC (Propagation Delay) Test Circuit

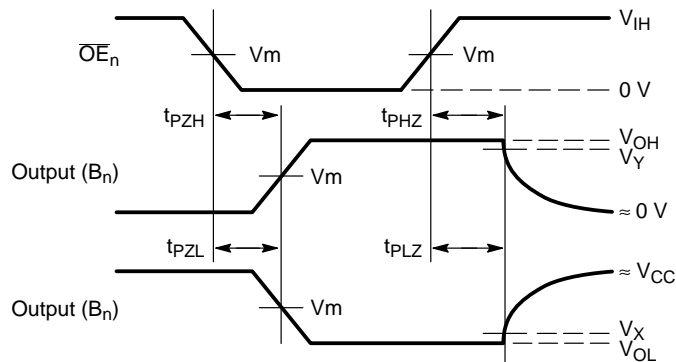
Test	Switch
$t_{PLH}$ , $t_{PHL}$	OPEN
$t_{PLZ}$ , $t_{PZL}$	$V_{CCO} \times 2$
$t_{PHZ}$ , $t_{PZH}$	GND

$C_L = 15 \text{ pF}$  or equivalent (includes probe and jig capacitance)  
 $R_L = 2 \text{ k}\Omega$  or equivalent  
 $Z_{OUT}$  of pulse generator =  $50 \Omega$



Waveform 1 – Propagation Delays

$t_R = t_F = 2.0 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$



Waveform 2 – Output Enable and Disable Times

$t_R = t_F = 2.0 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$

Figure 4. AC (Propagation Delay) Test Circuit Waveforms

Symbol	$V_{CC}$				
	3.0 V – 4.5 V	2.3 V – 2.7 V	1.65 V – 1.95 V	1.4 V – 1.6 V	0.9 V – 1.3 V
$V_{mA}$	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$
$V_{mB}$	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$
$V_X$	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$
$V_Y$	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

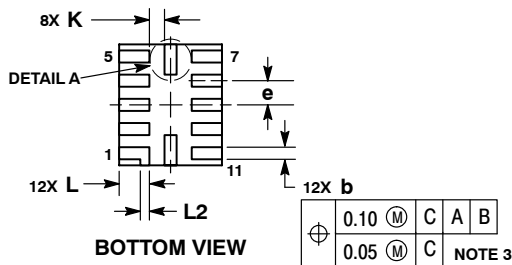
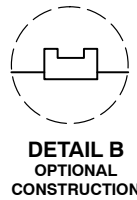
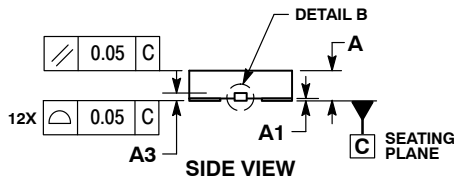
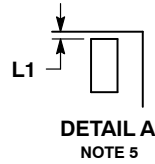
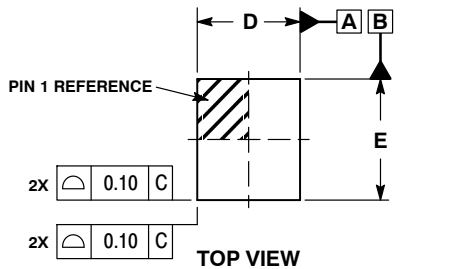
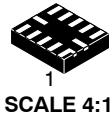
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### UQFN12 1.7x2.0, 0.4P

CASE 523AE-01  
ISSUE A

DATE 11 JUN 2007

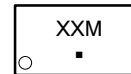


NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS
- DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
- MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH 0.03 MAX ON BOTTOM SURFACE OF TERMINALS.
- DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.70 BSC	
E	2.00 BSC	
e	0.40 BSC	
K	0.20	---
L	0.45	0.55
L1	0.00	0.03
L2	0.15 REF	

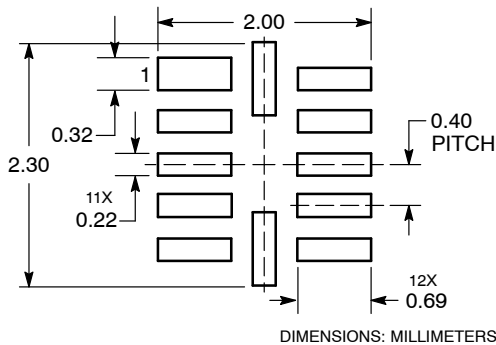
### GENERIC MARKING DIAGRAM\*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### MOUNTING FOOTPRINT SOLDERMASK DEFINED



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DESCRIPTION:	UQFN12 1.7 X 2.0, 0.4P	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

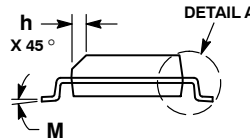
ON Semiconductor®



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

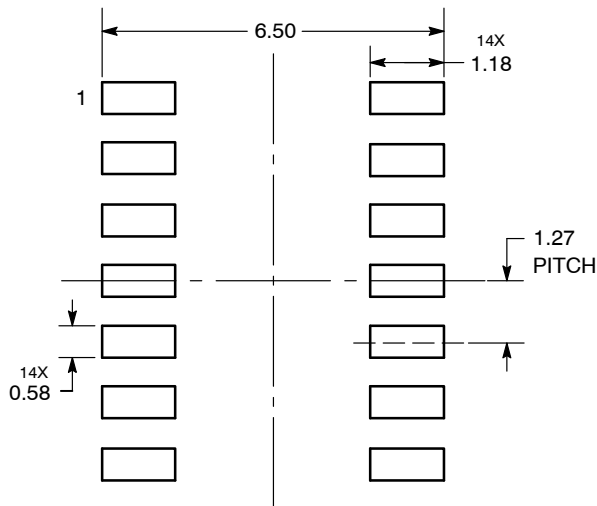
DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
  5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### STYLES ON PAGE 2

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DESCRIPTION:	SOIC-14 NB	PAGE 1 OF 2

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
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 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

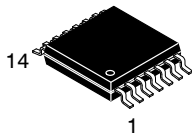
STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

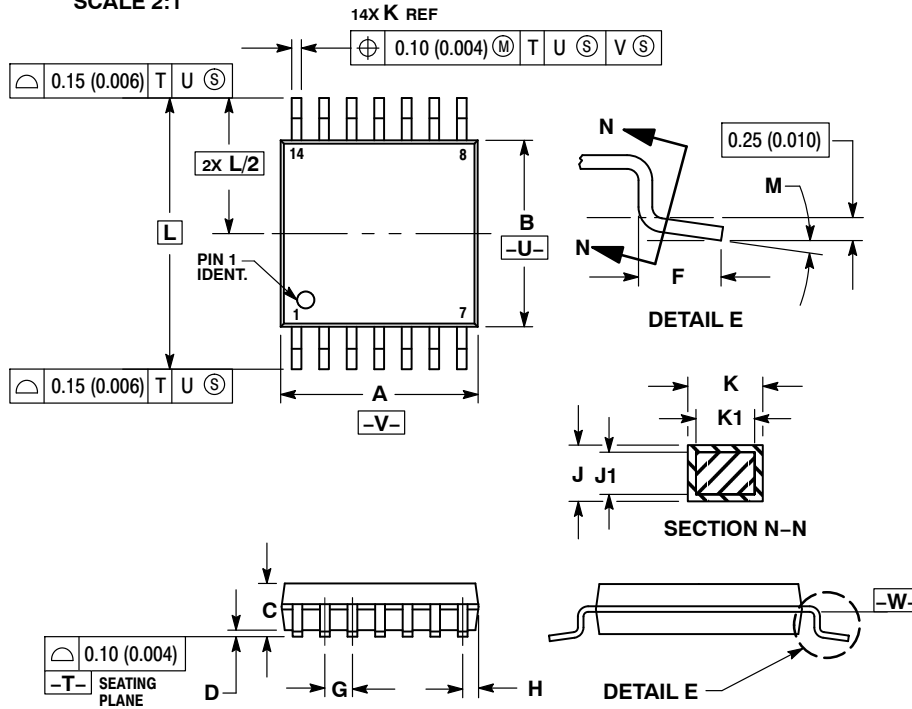
ON Semiconductor®



**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

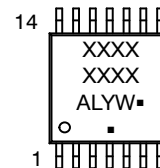


**NOTES:**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**GENERIC MARKING DIAGRAM\***

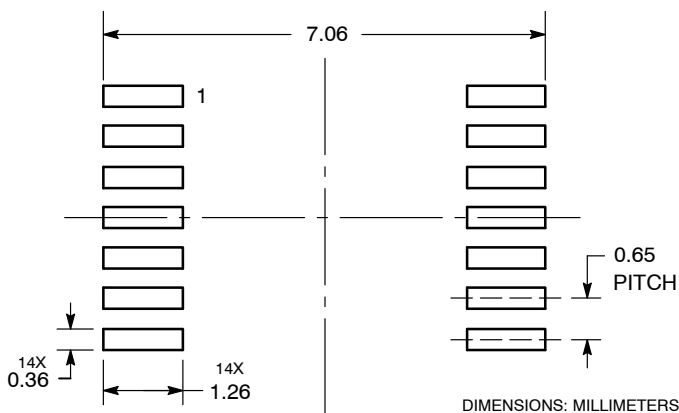


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT**



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